VX-160/180U Circuit Description

1. Receive Signal Path

Incoming RF from the antenna jack is delivered to the RF Unit and passes through a low-pass filter consisting of coils L1003, L1006 and L1007, capacitors C1002, C1007, C1013, C1017, C1022, C1025, C1029 and C1169, and antenna switching diode D1007 (RLS135).

Signals within the frequency range of the transceiver enter a varactor-tuned band-pass filter consisting of coils L1014 and L1015, capacitors C1057, C1058, C1064, C1071 and C1073, and diodes D1012 (HVC355B), D1013 (HVC355B), D1016 (HVC355B) and D1017 (HVC355B), then amplified by Q1015 (2SC5006) and enter a varactor-tuned band-pass filter consisting of coils L1021 and L1024, capacitors C1084, C1088, C1095 and C1097, and diodes D1022 (HVC355B), D1023 (HVC355B), D1024 (HVC355B), D1025 (HVC355B), D1026 (HVC355B) and D1027 (HVC355B), before first mixing by Q1025 (SGM2016AM).

Buffered output from the VCO is amplified by Q1009 (2SC5005) to provide a pure first local signal between 355.75 and 385.75 MHz for injection to the first mixer Q1025. The 44.25 MHz first mixer product then passes through monolithic crystal filter XF1002 (HDF0028, 5.5 kHz BW) to strip away all but the desired signal, which is then amplified by Q1032 (2SC4215Y).

The amplified first IF signal is applied to FM IF subsystem IC Q1036 (TA31136FN), which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and RSSI amplifier.

A second local signal is produced from the PLL reference/second local oscillator of 14.60 MHz crystal X1001. The 14.60 MHz reference signal is tripled by Q1036 and capacitor C1123, Coil L1005, then resulting the 43.8 MHz second local signal delivered to mixer section of Q1036 which produce the 450 kHz second IF mixed with the first IF signal.

The second IF then passes through the ceramic filter CF1001 (ALFYM450F=K: only on “Wide” channels) or CF1002 (ALFYM450G=K: only on “Narrow” channels) to strip away unwanted mixer products, and is then applied to the limiter amplifier in Q1036, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001 (CDBC450CX24).

Detected audio from Q1036 is applied to the audio high-pass filter, and then passed via the volume control to the audio amplifier Q1039 (NJM2070M), which provides up to 0.5 Watts to the optional headphone jack or a 4-Ω loudspeaker.

Squelch Control

The squelch circuitry consists of a noise amplifier and band-pass filter within Q1036, and noise detector D1030 (1SS355).

When no carrier received, noise at the output of the detector stage in Q1036 is amplified and band-pass filtered by the noise amplifier section of Q1036 and the network between pins 7 and 8, and then rectified by D1030.

The resulting DC squelch control voltage is passed to pin 37 of the microprocessor Q1014 (M37516E6HP). If no carrier is received, this signal causes pin 24 of Q1014 to go high and pin 20 to go high. Pin 24 signals Q1056 (RT1P441U) to disable the supply

voltage to the audio amplifier Q1039, while pin 20 hold the green (Busy) half of the LED off, when pin 24 is high and pin 20 is high.

Thus, the microprocessor blocks output from the audio amplifier, and silences the receiver, while no signal is being received (and during transmission, as well).

When a carrier appears at the discriminator, noise is removed from the output, causing pin 37 of Q1014 to go low and the microprocessor to activate the "Busy" LED via Q1014.

The microprocessor then checks for CTCSS or CDCSS code squelch information, if enabled. If not transmitting and CTCSS or CDCSS is not activated, or if the received tone or code matches that programmed, allows audio to pass through the audio amplifier Q1039 (NJM2070M) to the loudspeaker by enabling the supply voltage to it via Q1037.

Transmit Signal Path

Speech input from the microphone is amplified by Q1017 (NJM2902V), after pre-emphasis by C1059 and R1045, the audio passes another section of Q1017.

The processed audio may then be mixed with a CTCSS tone generated by Q1014 (M37516E6HP) for frequency modulation of the PLL carrier (up to ±5kHz from the unmodulated carrier) at the transmitting frequency.

If a CDCSS code is enabled for transmission, the code is generated by microprocessor Q1014 (M37516E6HP) and delivered to D1004 (HVC350B) for CDCSS modulating.

The modulated signal from the VCO Q1005 (2SK508-K52) is buffered by Q1008 (2SC5005). The low-level transmit signal is then passes through the T/R switching diode D1014 (DAN235E) to the amplifier Q1009 (2SC5005), driver amplifier Q1012 (2SC3357) and Q1016 (2SK2973), then amplified transmit signal is applied to the final amplifier Q1021 (2SK2974) up to 5 watts output power.

The transmit signal then passes through the antenna switch D1007 (RLS135) and is low-pass filtered to suppress harmonic spurious radiation before delivery to the antenna.

3-1 Automatic Transmit Power Control

Current from the final amplifier is sampled by R1110, R1124 and R1132, and is rectified by Q1033 (IMZ2A). The resulting DC is fed back through Q1027 (FMW1) to the drive amplifier Q1016 and final amplifier Q1021, for control of the power output.

The microprocessor selects "High" or "Low" power levels.

3-2 Transmit Inhibit

When the transmit PLL is unlocked, pin 14 of PLL chip Q1004 goes to a logic "Low", and unlock detector Q1054 (2SA1586Y) goes to a logic "High". The resulting DC unlock control voltage is passed to pin 14 of the microprocessor Q1014. While the transmit PLL is unlocked, pin 22 of Q1014 remains high, which then turns off Q1031 (CPH6102) and the Automatic Power Controller Q1027 (FMW1) to disable the supply voltage to the drive amplifier Q1012, Q1016 and final amplifier Q1021, thereby disabling the transmitter.

3-3 Spurious Suppression

Generation of spurious products by the transmitter is minimized by the fundamental

carrier frequency being equal to final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of Coils L1003, L1006 and L1007 plus Capacitors C1002, C1007, C1013, C1017, C1022, C1029, C1169 and C1196, resulting in more than 60 dB of harmonic suppression prior to delivery to the antenna.

4. PLL Frequency Synthesizer

The PLL circuitry on the Main Unit consists of VCO Q1005 (2SK508-K52), VCO buffer Q1008 (2SC5005), and PLL subsystem IC Q1004 (MB15A02PFV1), which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and charge pump.

Frequency stability is maintained by temperature compensating thermistor TH1001. The output from TH1001 is applied to pin 39 of Q1014. Q1014 output thermal data to D/A converter Q1052 (M62364FP) which produce the DC voltage according with the thermal data. The resulting DC voltage is applied to varactor diode D1004 (HVC350B) to stabilize the 14.60MHz Reference Frequency.

While receiving, VCO Q1005 oscillates between 405.75 and 440.75 MHz according to the transceiver version and the programmed receiving frequency. The VCO output is buffered by Q1008, then applied to the prescaler section of Q1004. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1004, before being sent to the programmable divider section of Q1004.

The data latch section of Q1004 also receives serial dividing data from the microprocessor Q1014, which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 5 kHz or 6.25 kHz derivative of the current VCO frequency.

Meanwhile, the reference dividers section of Q1005 divides the 14.60 MHz crystal reference from the reference oscillator Q1022, by 2920 (or 2336) to produce the 5 kHz (or 6.25 kHz) loops reference (respectively).

The 5 kHz (or 6.25 kHz) signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1004, which produces a pulsed output with pulse duration depending on the phase difference between the input signals.

This pulse train is filtered to DC and returned to the varactor D1001 (HVC355B) and D1002 (HVC355B). Changes in the level of the DC voltage applied to the varactor, affecting the reference in the tank circuit of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator.

The VCO is thus phase-locked to the crystal reference oscillator. The output of the VCO Q1005, after buffering by Q1008, is applied to the first mixer as described previously.

For transmission, the VCO Q1005 oscillates between 400 and 430 MHz according to the model version and programmed transmit frequency. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the receiving case). Also, the VCO is modulated by the speech audio applied to D1005 (HVC350B), as described previously.

Receive and transmit buses select which VCO is made active by Q1002 (RT1N441U).

5. Miscellaneous Circuits

5-1 Push-To-Talk Transmit Activation

The PTT switch on the microphone is connected to pin 48 of microprocessor Q1014, so that when the PTT switch is closed, pin 23 of Q1014 goes low. This signal disables the receiver by disabling the 5 V supply bus at Q1035 (DTB123EK) to the front-end, FM IF subsystem IC Q1036 and receiver VCO circuitry.

At the same time, Q1026 (FMW1) and Q1031 (CPH6102) activate the transmit 5V supply line to enable the transmitter.