VX-1210 Circuit Description

Receive Signal Path

Incoming RF signal from the ANT jack is delivered to J3005 on the PA Unit, and passes through the ANT relay RL3014 and TX/RX relay RL3013 to the low-pass filter consists of the coils L3016 & L3017 and capacitors C3050, C3051, & C3052 which cut-off frequency is 30 MHz.

The RF signal is then applied to J1001 on the MAIN Unit, and passed through the limitter circuit consist of **D1001**, **D1002**, **D1003**, and **D1004** (all **1SS244**) to prevent the distortion from the high RF input and one of six band-pass filters which strip away unwanted signals to the RF amplifier **Q1001** and **Q1002** (both **2SK520-K41**).

The amplified RF signal is applied to the double balanced mixer **D1009** (**HSB88WS**) where the RF signal is mixed with 1st local signal delivered from buffer **Q1005** (**2SC2954**), resulting in a 47.055 MHz 1st IF signal.

The 47.055 MHz 1st IF signal is fed through the monolithic crystal filter **XF1001** (**47M15AU**) which strip away unwanted mixer products, and then the 1st IF signal is applied to the 2nd mixer **Q1006** (**3SK151GR**), where it is mixed with the 36.355 MHz 2nd local signal delivered from buffer amplifier **Q2038** (**2SC2714Y**) on the Control Unit, resulting in a 10.7 MHz 2nd IF signal.

The 10.7 MHz 2nd IF signal is fed through the Noise Blanker Gate **D1014** & **D1015** (both **1SS302**) and 2nd IF filter **XF1002** (**10M2.4D**) to the 2nd IF amplifier **Q1007**, **Q1008**, & **Q1009** (all **3SK151GR**).

A portion of the 2nd IF signal is amplified by **Q1011** & **Q1012** (both **3SK151GR**), and then detected (with twofold voltage amplitude) by diode **D1016** (**HSM198S**). This detected output controls the gain of above-mentioned FET by an average AGC voltage responsible for AGC amplifier **Q1013** (**2SK2812**). Also, noise pulse contained in the detected output is amplified by the **Q1014** (**2SC2812**) to be utilized for controlling Noise Blanker Gate **D1014** & **D1015**.

In SSB, CW and FSK modes, the amplified 2nd IF signal from **Q1009** is applied to the product detector diode **D1024** & **D1025** (both **HSM198S**).

In AM mode, the amplified 2nd IF signal from **Q1009** is fed through the buffer amplifier **Q1015** (**2SC2812**) and AM detector diodes **D1021** & **D1022** (both **HSM198S**), then applied to the buffer amplifier **Q1019** (**2SC2812**).

The audio signal from the selected detector is fed through the low-pass filter **Q1020** (**2SC2812**), which eliminates high-pitched noise on the audio signal, and amplified by AF preamplifier **Q1023** (**M5218AFP**). The audio signal is then fed through the AF mute gate **Q1025** (**TC4S66F**) and front panel AF potentiometer **VR4001**, then back to audio amplifier **Q1027** (**TDA2822D**) and **Q1058** (**TDA7235**).

A portion of the output of AM detector diodes **D1021** & **D1022** is amplified by AGC amplifier **Q1016** (**2SC2812**). The amplified DC voltage is fed through the buffer amplifier **Q1018** (**2SC2812**) to the RF amplifier **Q1001** & **Q1002** and also the amplified DC voltage is fed to the 2nd gates of the IF amplifiers **Q1007**, **Q1008**, & **Q1009**, to reduce their gain when strong signals are present in the receiver passband.

When pulse type noise is received, a sample of the 2nd IF signal from **Q1006** is amplified by **Q1011** & **Q1012** (both **3SK151GR**) before application to pulse detector **D1016** (**HSM198S**). The resulting DC pulse switches noise blanker gate controller **Q1014** (**2SC2812**), which interrupts the 2nd IF signal at noise blanker gate **D1014** & **D1015** during the length of the noise pulse.

The DC voltage from the pulse detector is also amplified by **Q1013** (**2SC2812**) and fed back to 2nd gates of the AGC amplifier **Q1011** & **Q1012** as noise blanker AGC.

Transmit Signal Path

The speech audio from the microphone is delivered to J8001 on the MIC-CONN Unit, then applied to the J2002 on the CNTL Unit.

The speech audio is amplified by **Q2046** (**NJM4558V**), then passed though the MIC gain potentiometer VR1001, and further amplified by **Q1043** (**2SC2812**) before application to balanced modulator **D1036** (**HSB88WS**). The modulator also receives 10.7 MHz carrier signal from buffer amplifier **Q1022** (**2SC2812**).

The modulated signal is delivered to the crystal filter **XF1002** where is stripped unwanted sideband. The resulting 10.7 MHz single sideband signal is buffered by **Q1045** (**3SK151GR**) and then applied to single balanced mixer **Q1046** (**3SK151GR**) which receives 36.355 MHz local signal from buffer amplifier **Q2038** on the CNTL Unit. In AM mode, the single balanced mixer **Q1046** also receivers 10.7 MHz carrier signal from buffer amplifier **Q1022** to resulting the double sideband (AM) signal.

The resulting the 47.055 MHz IF signal is fed through the monolithic crystal filter **XF1001** which strip away unwanted mixer products, and then amplified by **Q1048** (**3SK151GR**). The amplified IF signal is delivered to double balanced mixer **D1009**, where it is mixed with the PLL local signal from the buffer amplifier **Q1005** (**2SC2954**).

The resulting the RF signal at the transmit frequency is fed through the TX amplifier **Q1049** (**2SC2714Y**) and buffer amplifier **Q1050** (**2SC3357**), and then filtered by one of six bandpass filters to suppress out-of-band mixer products. The RF signal is then amplified by **Q1051** (**2SK2954**) and delivered to PA Unit.

On the PA Unit, the low-level RF signal from the Main Unit is amplified by pre-drive **Q3501** (**2SC2166**), push-pull driver **Q3502/Q3503** (both **2SC2166**), and then push-pull final amplifier **Q3504/Q3505** (both **2SC3133**), which provides approximately 20 watts RF output power.

The RF output from the final amplifier is fed through the one of six low-pass filters, sampling directional coupler T3001, and TX/RX relay RL3014 before delivery to the antenna jack.

The sampling directional coupler senses forward and reverse power output, which is rectified by **D3001/D3005** & **D3002/D3006** (all **1SS106**) respectively for return to the ALC and SWR sensing circuitry on the Main Unit. The DC voltages derived from forward and reverse power are applied in combination to op-amp **Q1053** (**M5218AFP**), the output which is buffered by **Q1055** (**2SC2812**), then fed back to the 2nd gate of the 10.7 MHz IF amplifier **Q1045** and the 2nd gate of the 47.055 MHz IF amplifier **Q1048**, so that transmitter IF gain is regulated by relative power output, thus preventing overdrive or transmission into an excessive impedance mismatch at the antenna. In the AM mode, A portion of the output of forward power from the PA Unit is fed through the integral circuit consist of R1321 & C1252 which is equalized forward power, then applied to **Q1054** (**M5218AFP**), which is compared with the reference voltage from **Q2039** (**M62354FP**) on the CNTL Unit. The output from **Q1054** fed back to the 2nd gate of the 47.055 MHz IF amplifier **Q1048**, so that the AM carrier power is regulated.

PLL Circuit

The PLL local signal for the receiver 1st local and the transmitter final local is generated by one of three VCOs: **Q2017**, **Q2018**, & **Q2019** (all **2SK210GR**) in conjunction with varactor diodes **D2008**, **D2009**, & **D2010** (all **HVU359**) on the CNTL Unit. The oscillating frequency is determined primarily by the level of DC voltage applied to the varactor diodes. The VCO output is buffered by **Q2011** (**2SK302Y**), amplified by **Q2025** (**2SC535B**) and bandpass filtered by capacitor C2088, C2091, C2093, C2095, C2096, & C2099 and coils L2012, L2013, L2015, & L2016. The filtered PLL local signal is applied to the J1002 on the Main Unit, then fed through the buffer amplifiers **Q1003** (**2SC2714Y**), **Q1004** (**2SC3356**), and **Q1005** (**2SC2954**) to the TX final mixer/RX 1st

mixer **D1009**.

A portion of the output of buffer amplifier **Q2011** is further amplified by **Q2006** (**2SC2714Y**) and delivered to the PLL subsystem IC **Q2001** (**LM7001JUM**), which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. The sample VCO signal is divided by the programmable divider section of the **Q2001**. Meanwhile, the 36.355 MHz crystal reference oscillator X2002 and **Q2037** (**2SC2714Y**) amplified by **Q2036** & **Q2033** (both **2SC2714Y**) and divides by the DDS IC **Q2024** (**AD9850BRS**) accordance with the PLL dividing data from the main CPU **Q2030** (**HD64F2132RF**), then applied to the low-pass filter consist of capacitors C2034, C2036, C2037, C2038, C2041, C2046, C2047, C2051, & C2053 and coils L2002, L2003, L2004, & L2006. The divided and filtered reference signal is applied to the reference divider section of the PLL subsystem IC **Q2001**, where divide by 72 to produce the loop reference.

The divided signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of the PLL subsystem IC **Q2001**, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is low-pass filtered by **Q2003** (**2SK208Y**) & **Q2004** (**2SC2812**), then fed back to the VCO varactor diodes **D2008**, **D2009**, & **D2010**.

Changes in the DC voltage applied to the varactor diodes **D2008**, **D2009**, and **D2010** affect the reactance in the tank circuit VCO **Q2017**, **Q2018**, and **Q2019**, changing the oscillating frequency according to the phase difference between the signals derived from the VCO and the crystal reference oscillator. The VCO is thus phase-locked to the reference frequency standard.

A portion of the output of reference signal from **Q2037** is buffered by **Q2038** (**2SC2714Y**), then applied to the low-pass filter consist of capacitors C2155 ~ C2159 and coils L2024 & L2025. The filtered reference signal delivered to J1003 on the Main Unit, then applied to the 2nd gate of the TX 1st mixer Q1045 and 2nd gate of the RX 2nd mixer **Q1006**.

A portion of the output of reference signal from **Q2033** is applied to further DDS IC **Q2032** (**AD9835BRU**) where is divided reference signal to 10.7 MHz carrier signal accordance with the PLL dividing data from the main CPU **Q2030**, then fed through the low-pass filter consist of capacitors C2117, C2119, & C2122 ~ C2126 and coils L2020 ~ L2022. The filtered carrier signal is buffed by **Q2035** (**2SC2812**) and delivered to J1005 on the Main Unit, then fed through the carrier amplifier **Q1022** (**2SC2812**) to the detector diode **D1024** & **D1025** and balanced modulator **D1036**.

Control Circuit

Major frequency control functions such as memory selecting, display, and PLL divider control are preformed by main CPU **Q2030** (**HD64F2132RF**) on the CNTL Unit, at the command of the user via the tuning knob and function switches on the front panel.

The programmable divider data for the PLL from main CPU **Q2030** is applied directly to DDS IC **Q2024** (**AD9850BRS**) & **Q2032** (**AD9835BRU**) and PLL subsystem IC **Q2001** (**LM7001JUM**).

The Mode selection data from the main CPU **Q2030** is level shifted by **Q2007** ~ **Q2010** (all **FMC3**) to control the various circuit required for the selected mode.

The Band selection binary data from the main CPU **Q2030** is BCD-to Decimal decoded by **Q2021** (**TC4028BF**). The resulting decimal outputs are level shifted by **Q2015** (**TD62083F**) to select the active band-pass filter on the Main Unit required for the operating frequency. Also, the decimal outputs from **Q2021** are delivered to PA Unit, then level shifted by **Q3001** ~ **Q3006** (all **FMC5A**) to select the active low-pass filter required for the operating frequency.

TX/RX Control

When press the PTT switch, **Q2002** (**IMZ2**) on the CNTL Unit goes low, thus pin 22 of main CPU **Q2030** (**HD64F2132RF**) goes low. This signal disable the receiver 12 V bus at **Q2022** (**2SA1179**). At the same time, activate the transmit 12 V bus at **Q2016** (**2SA1365**).

Power Supply & Regulation

The +5 V bus for the main CPU is derived from the 13.5 V bus via regulator **Q2050** (**NJM78L05UA**) on the CNTL Unit.

The +5 V bus is derived the from the 13.5 V bus by switching regulator **Q2043** (**IR3M03A**) and rectified **D2016** (**11EQS04**) and L2028. A portion of the +5 V is switched by **Q2044** (**2SC4047**) & **Q2047** (**2SA1365**) on the CNTL Unit, under control of the main CPU **Q2030** via pin 58.

The +8 V bus is derived from the 13.5 V bus via regulator **Q2048** (**KIA7808API**) on the CNTL Unit.

The –8 V bus for the op amps is derived from the +5 V bus to **Q2042** (**2SC4154E**) where it is switched by clock signal of PLL IC **Q2001** (**LM7001JUM**) the to converted to AC 5 V, then twofold rectified by **D2017** (**DA221**) to provide –8 V.