Theory of Operation

YAESU MUSEN CO., LTD.
FCC ID: K66RP80U
EXHIBIT #: 9A

3. THEORY OF OPERATIONS

3.1 RX Unit

3.1.1 PLL circuit

The PLL circuit consists of three blocks: PLL IC QR20; charge pump QR18 and QR19 and low pass filter RR45 CR68, RR40, CR67, RR43 and CR66. The XR02 TCXO is used to generate the 12.6 MHz reference oscillation frequency. Either 1/64 or 1/65 can be selected as the frequency division ratio for operation at a reference frequency of approximately 196 kHz at 1/64 or approximately 193 kHz at 1/65.

3.1.2 Front end

The RF signals supplied from JR01 pins 16 and 32 pass through helical coil LR04 to RF amplifier QR03. The RF amplifier QR03 amplifies these signals by 15 dB, outputs them from its collector, and then they are again input to helical coil LR07. RF amplifier QR03 provides class-B amplification to improve the secondary and tertiary distortion characteristics. The RF signals output from LR07 are supplied to the double balanced mixer (DBM) and matching attenuator (ATT). The attenuator is composed of resistors RR63, RR64 and RR65, and it provides a 1 dB attenuation.

3.1.3 1st mixer circuit and IF amplifier circuit

The first mixer circuit is a double balanced mixer (DBM) type. DBM is configured as a unit and composed of LR21, LR22 and QR04. The local signal is amplified to 10 dBμ more than the output by QR05 and supplied to DBM. The RF signal, which has been switched by the local signal, gives rise to a difference from the local signal, and this difference is output as the IF signal (44.95 MHz) from DBM. The IF signal output is supplied to the 2-stage 44.95 MHz MCF (crystal filter) FR01 and FR02 via DBM matching attenuators RR60, RR67 and RR68. After the converted spurious emissions have been filtered out by the 2-stage MCF, the IF signal is converted into the 455 kHz second IF signal by the second mixer. The second local signal is generated by XR01, and its frequency is 44.495 MHz. It is supplied from QR12 pins 1 and 2. After conversion to 455 kHz, the 2nd IF signal is output from QR12 pin 4, passes through the FR03 and FR04 ceramic filters, and is again supplied from pin 6. It is then subject to a 1/4 π phase delay by quadrature coil LR17, converted into the audio signal by the internal phase comparator, and output from QR12 pin 11. The audio signal is now divided into two: one signal is output to the control unit from JR01 pin 7 and the other is supplied to the QR11 noise amplifier where it is squelched.

3.1.4 Squelch circuit

The noise amplified by QR11 is detected by QR10, and two signals are output. One signal is output as the squelch control to pin 5 of JD50 on the volume P.C.B from JR01 pin 8. This is then output from JR01 pin 5 to JD01 pin 4 of the display unit. The other signal is supplied to pin 15 of squelch ON/OFF circuit QR12 is converted into an ON/OFF signal by the internal comparator and output from QR12 pin 16. The signal passes through JR01 pin 5 and is supplied to JD01 pin 4 of display unit.

3.2 TX Unit

3.2.1 PLL circuit

The PLL circuit consists of three blocks: PLL IC QT14; charge pump QT12 and QT13; and low-pass filter RT52, CT54, RT51, CT53, RT50 and CT52. The XT01 TCXO is used to generate the 12.6 MHz reference oscillation frequency. Either 1/64 or 1/65 can be selected as the frequency division ratio for operation at a reference frequency of approximately 196 kHz at 1/64 or approximately 193 kHz at 1/65.

3.2.2 RF amplifier circuit

The VCO QT06 RF output is supplied to buffer amplifier QT05 and then to RF amplifier QT04. After amplification by QT04 to 20 mW the signal is supplied to RF amplifier QT03 where it is amplified to between about 50 and 60 mW and further supplied to final-stage RF amplifier QT01. The maximum output of QT01 is approximately 1.5 W. The QT01 output is supplied to the low-pass filter to remove harmonic spurious emissions. Its output is supplied to booster unit JW01 via JT01 pins 16 and 32.

3.2.3 APC (auto power control) circuit

The detected signals from the booster unit are supplied from JT01 pin 20 to the base of QT20. By the fluctuation of the voltage supplied to QT20, the QT19 base voltage is shifted, the resistance between the collector and emitter of QT19 is varied and the APC amplifier QT09 base voltage is controlled. By controlling this base voltage the voltage drop between the collector and emitter of QT09 is controlled, the QT03 collector voltage is adjusted, and automatic power control is achieved.

3.2.4 TX low

The signal for the voltage which was thermally detected inside the booster is supplied to TX unit JT01 pin 21 via the control unit. The input voltage is supplied through QT19 to the same circuit as the APC circuit. In the TX low mode, the QT20 base voltage is controlled by a constant voltage so that the output signal of the booster will be –3 dB.

3.3 Booster Unit

The RF signal (approx. 1.5 W) supplied by JW01 is amplified by RF power amplifier QW01 to about 8 W. It is then further amplified to 15 W by RF power amplifier QW02 and supplied to final-stage RF power amplifier QW03. The 15 W RF signal is amplified to between 55 and 60 W by QW03 and output from JW04 via the 3-stage low-pass filter which provides an attenuation of 0.8 dB. The RF signal for APC is detected by the directional coupler composed of the pattern from between QW03 and its output, is detected by RF detector QW04 and output from JW02 pin 3 as a DC signal. Two posistors are provided for temperature compensation. One, QW05, is controlled by the control unit so that the output power is reduced by 3 dB when the heat sink temperature exceeds 85 °C or so. The other, QW06, is controlled by the control unit so that fan motor MG01 is automatically activated when the heat sink temperature exceeds 65 °C.

3.4 Control Unit

3.4.1 RX audio circuit

The RX audio signal which is input to JL01 pin 7 (RX Audio) is supplied to CTCSS IC QL06 and analog switch QL03 (2/4, 3/4). While the repeater is operating, the level of the audio signal is first adjusted by RL33. QL03 (4/4) is turned ON, and the audio signal is mixed in TX unit JT01 pin 23 via JL03 pin 23. After having passed through QL03 (3/4), the audio signal passes through the high-pass filter contained in CTCSS IC QL06 which thoroughly filters out the unnecessary audio signals below 300 Hz. De-emphasis circuit QL05 then de-emphasizes the amplified audio signal with a 6 dB/oct frequency response over a frequency range of 300 to 3000 Hz, and amplifies the audio level. After passing through preamplifier circuit QL04, the level of the signal is then adjusted by volume control RD51. The signal is applied to audio amplifier QL01 and amplified to a level sufficient to drive speaker NG01.

3.4.2 TX audio circuit

The TX audio signal, which is supplied to microphone jack JD61 pin 1, is input to JL01 pin 8 (Mic Audio). It is adjusted to a level for standard modulation by RL29 and then supplied to microphone amplifier QL09. After being amplified by QL09, the audio signal passes through analog switch QL10 for microphone muting, and mixer amplifier QL11 (1/4) and the pre-emphasis circuit QL11 (2/4) pre-emphasize the amplified audio signal with a 6 dB/oct frequency response over a frequency range of 300 to 3000 Hz, and amplify the audio level. The audio signal is then supplied to limiter amplifier QL11 (3/4) and low-pass filter QL11 (4/4) and its maximum modulation level is adjusted by mic deviation RL50 in order to prevent overmodulation. It is mixed with the RX audio signal when the repeater is operating and sent.

3.4.3 TX LED driver

The RF power detection signal, which is input to JL01 pin 10 (TX RF DET), turns on the TX indicators (QD30, QD34) on the front panel by means of RF detector amplifier QL12. Its level is adjusted by APC volume control RL54, and the signal is fed back to the APC circuit in the TX unit.

3.4.4 Fan driver

The temperature detection signal, which has been input to JL01 pin 9 (TEMP FAN), drives fan motor MG01 which is mounted on the heat sink of the booster unit by means of fan switches QL13 and QL14. When the temperature of the booster unit has risen above a specific level, fan motor MG01 is rotated in order to air-cool the unit.

3.4.5 Low power

The temperature detection signal, which has been input to JL01 pin 24 (TEMP LOW), is stored in the memory by flip-flop circuit QL15, QL16 and QL17. A 3 dB reduction in the low power level is produced by low power volume control RL66. When the temperature of the booster unit has risen above a specific level, the RF power is reduced during continuous transmission in order to prevent the booster being destroyed by heat. When RX mode is restored from the TX mode by the JL01 pin 22 (SET PTT) input signal, the flip-flop circuit is reset.

3.4.6 Code guard (CTCSS)

CTCSS IC QL06 provides encoding and decoding in accordance with the tone codes supplied by 3 signals (DATA, CLOCK and STB) from microprocessor QD01.

- Encoding -

When the microphone (CMP820E) PTT switch is pressed (JD61 pin 2 and ground are shorted), sub-audio signals corresponding to the tone codes supplied from microprocessor QD01 are output from CTCSS IC QL06 pin 16 (TONE OUT) as sine waves. Their level is first adjusted by RL23, and then the signals are mixed with the TX audio signals and sent.

- Decoding -

When the sub-audio signals contained in the RX audio signals input to CTCSS IC QL06 pin 24 (DEC IN) match the tone codes supplied from microprocessor QD01, CTCSS IC QL06 pin 13 (DET) outputs a low-level (0 V) signal. Conversely, if they do not match, it outputs a high-level (5 V) signal. This DET signal is supplied to microprocessor QD01 and used as the code guard function.

3.5 Display Unit

3.5.1 Microprocessor

The functions of the microprocessor (QD01) ports are described in the table below.

In/Out Port Descriptions

Table 3-1

Pin No.	In/Out	Name	Description
1	O	DAT	I²C bus line data output.
2	O	CLK	I²C bus line clock output.
3	–	VCC	Connect to power supply (+5 V).
4	I	MD0	Mode setting input; connect to VCC.
5	I	MD1	Mode setting input; connect to VCC.
6	I	MD2	Mode setting input; connect to VCC.
7	I	RES	Microprocessor reset input.
8	I	NMI	Non-maskable interrupt input; connect to VSS.
9	–	VSS	Connect to ground.
10	O	DB0	Data bus output for LCD, key matrix.
11	O	DB1	Data bus output for LCD, key matrix.
12	O	DB2	Data bus output for LCD, key matrix.
13	O	DB3	Data bus output for LCD, key matrix.
14	O	DB4	Data bus output for LCD, key matrix.
15	O	DB5	Data bus output for LCD, key matrix.
16	O	DB6	Data bus output for LCD, key matrix.
17	O	DB7	Data bus output for LCD, key matrix.
18	O	P30	Data bus output for LCD contrast.
19	O	P31	Data bus output for LCD contrast.
20	O	P32	Data bus output for LCD contrast.
21	O	P33	Data bus output for LCD contrast.
22	O	RS	LCD register selection output.
23	O	R/W	LCD read/write output.
24	O	E	LCD data read/write drive output.
25	O	SET PTT	TX power control output. Low : TX+B on High : TX+B off
26	I	P40	Data bus input for key matrix.
27	I	P41	Data bus input for key matrix.
28	I	P42	Data bus input for key matrix.
29	I	P43	Data bus input for key matrix.
30	I	CH SW1	No connection.
31	I	CH SW2	No connection.
32	I	CH SW3	No connection.
33	I	CH SW4	No connection.
34	–	VCC	Connect to power supply (+5 V).
35	O	PLL DATA	PLL IC, CTCSS IC data output.
36	O	PLL CLOCK	PLL IC, CTCSS IC clock output.
37	O	RX PLL STB	RX PLL IC strobe output.
38	O	BEEP	1000/350 Hz square wave output.
39	O	TX PLL STB	TX PLL IC strobe output.
40	O	CTCSS STB A	Tone A (CTCSS IC) strobe output.
41	O	CTCSS STB B	Tone B (CTCSS IC) strobe output.
42	O	DCS STB A	Not used.
43	–	VSS	Connect to ground.
44	–	AVSS	Connect to ground.
45	I	MIC PTT	PTT SW input. Low : PTT SW on High : PTT SW off

Pin No.	I/O	Name	Description
46	I	PROGRAM INHI	Program and clone mode inhibit input. Low : Program and clone mode enable High : Program and clone mode inhibit
47	I	COR	RX signal detection input. Low : No RX signal High : RX signal available
48	I	PLL UNLOCK	PLL loop circuit status detection input. Low : Locked High : Unlocked
49	–	AVCC	Connect to power supply (+5 V).
50	O	SEROP	Cloning data output.
51	I	SERIP	Cloning data input.
52	O	AF MUTE2	Repeater TX audio signal mute output. Low : Muting on High : Muting off
53	O	AF MUTE1	RX audio signal mute output. Low : Muting on High : Muting off
54	O	MIC MUTE	Microphone audio signal mute output. Low : Muting on High : Muting off
55	O	BUSY LED	Busy indicator ON output. Low : Busy indicator OFF High : Busy indicator ON
56	–	VSS	Connect to ground.
57	I	EXTAL	Connect reference crystal oscillator.
58	O	XTAL	Connect reference crystal oscillator.
59	O	DCS STB B	Not used.
60	I	TONE DET B	Tone B (CTCSS IC) decode result detection input. Low : Tone code matched High : Tone code not matched
61	I	TONE DET A	Tone A (CTCSS IC) decode result detection input. Low : Tone code matched High : Tone code not matched
62	I	I^2C INT	I^2C bus line interrupt input. Low : Interrupt available High : No interrupt
63	O	T.O.T TRIG	TX timer time-out output.
64	O	PWR CONT	Not used.

3.5.2 EEPROM

The EEPROM (QD02) is an electrically erasable programmable, read-out memory whose data can be changed. Data is transferred with the microprocessor (QD01) via the I^2C bus.

3.5.3 Reset

The SWED +5 V output from the 5 V regulator (QD05) is supplied to the reset IC (QD07). When the input voltage is less than 4.0 to 4.4 V, the output voltage is set to 0 V, setting the microprocessor (QD01) pin 7 level low and resetting the unit.

3.6 Power Supply Circuit

The power supply unit in the RP80V is as shown below.

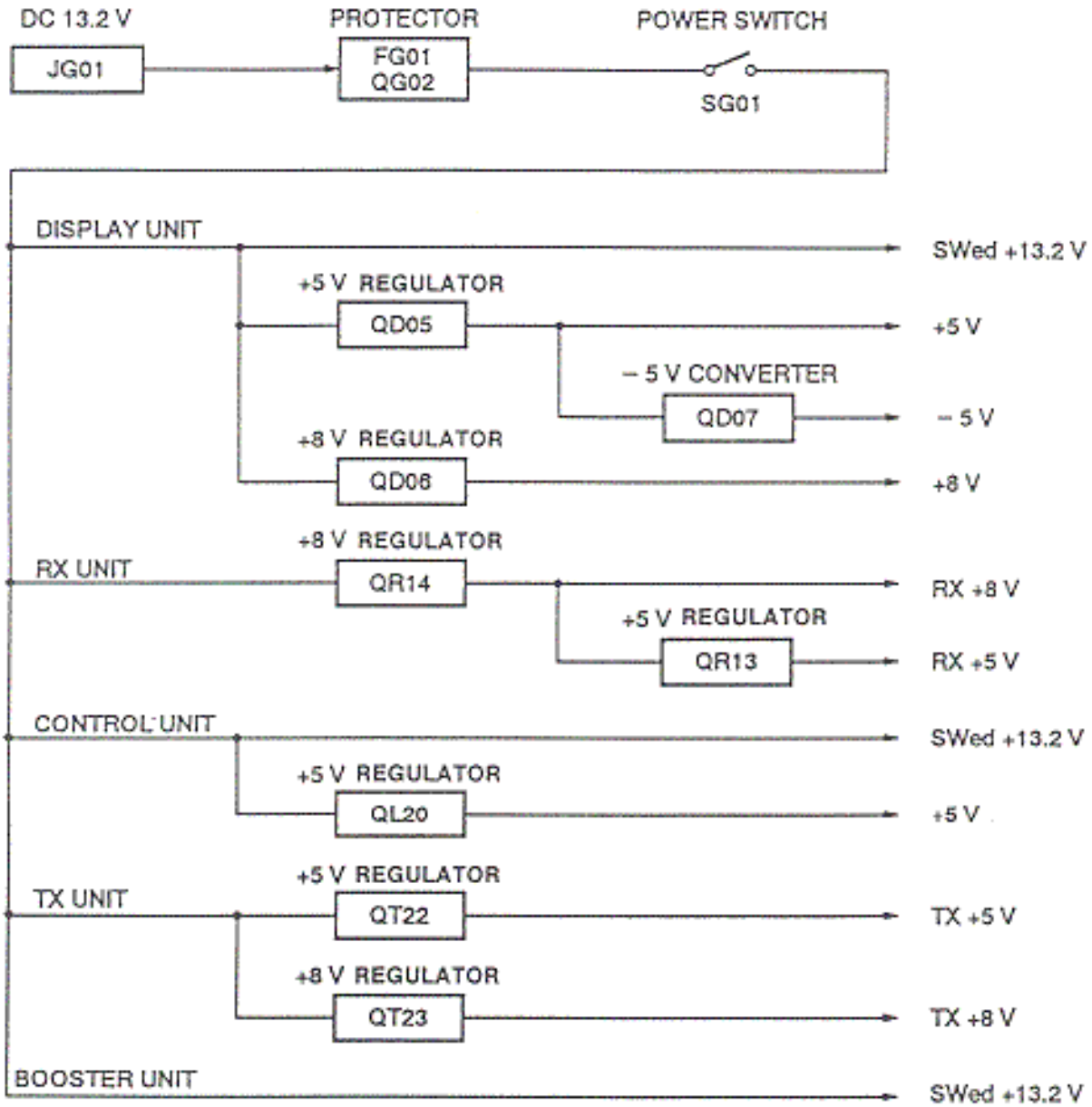

Figure 3-1 Block diagram of power supply circuit