CIRCUIT DESCRIPTION of RP80U

Oscillator and Frequency Stability Circuits

A. Receiver Section

1: Oscillator Circuits

A PLL is used to control the receiver 1st local oscillator circuits. QR20 is an IC containing a reference frequency divider, a programmable counter, a phase detector and a dual modular pre-scalar which forms a pulse swallow counter. The output of the phase detector passes through the active low pass filter(QR18, QR19), is converted to DC voltage, and on to control the oscillation frequency Voltage Controlled Oscillator consists of QR16.

The reference oscillator consists of XP02 produces a reference frequency of 12.6MHz. XR02 and QR20 divides the frequency to produce a reference signal of 12.5KHz. The VCO output is divided by the QR20 pulse swallow counter and is compared to the reference 12.5KHz signal by the phase detector. The VCO output is supplied to the 1st RX mixer to heterodyne the RF signal.

2: Frequency Stability Circuit

PLL frequency stability is determined by the inherent design of oscillator(XP02). This oscillator circuit uses a highly stabilized, temperature controlled crystal oscillator which prevents the maximum frequency variation from exceeding ±2.5ppm.

B. Transmitter Section

1: Oscillator Circuits

A PLL is used to control the receiver 1st local oscillator circuits. QT14 is an IC containing a reference frequency divider, a programmable counter, a phase detector and a dual modular pre-scalar which forms a pulse swallow counter. The output of the phase detector passes through the active low pass filter(QT12, QT13), is converted to DC voltage, and on to control the oscillation frequency Voltage Controlled Oscillator consists of QT06.

The reference oscillator consists of XT01 produces a reference frequency of 12.6MHz. XT01 and QT14 divides the frequency to produce a reference signal of 12.5KHz. The VCO output is divided by the QT14 pulse swallow counter and is compared to the reference 12.5KHz signal by the phase detector. The VCO output is supplied to the TX input where it initializes the transmitter circuit.

2: Frequency Stability Circuit

PLL frequency stability is determined by the inherent design of oscillator(XT01). This oscillator circuit uses a highly stabilized, temperature controlled crystal oscillator which prevents the maximum frequency variation from exceeding ±2.5ppm.

3: Modulation Limiting Circuit

Audio from the microphone passes through the pre-emphasis circuit of audio processor(QL09, QL10, QL11). This limiting circuit controls the amplitude to a level below system deviation. The roll-off filter reduces the high frequency ranges by 18dB/OCT.

4: Spurious Radiation Suppression

Harmonic and spurious signals are initially attenuated by about 50dB in the TX final output circuit (QW03). They are further attenuated by more than 60dB by the low pass filter consists of [LW12 to 15, CW20, CW23, CW26, CW27, CW38].