2. THEORY OF OPERATIONS

Note : Refer to the block diagrams (figure 2-1 through 2-8) in the text for the operations of the circuits.

2.1 PLL Block

The PLL block comprises a VCO, TCXO, PLL IC, and PLL loop filter.

The VCO circuit generates the transmission signal and first local signal directly.

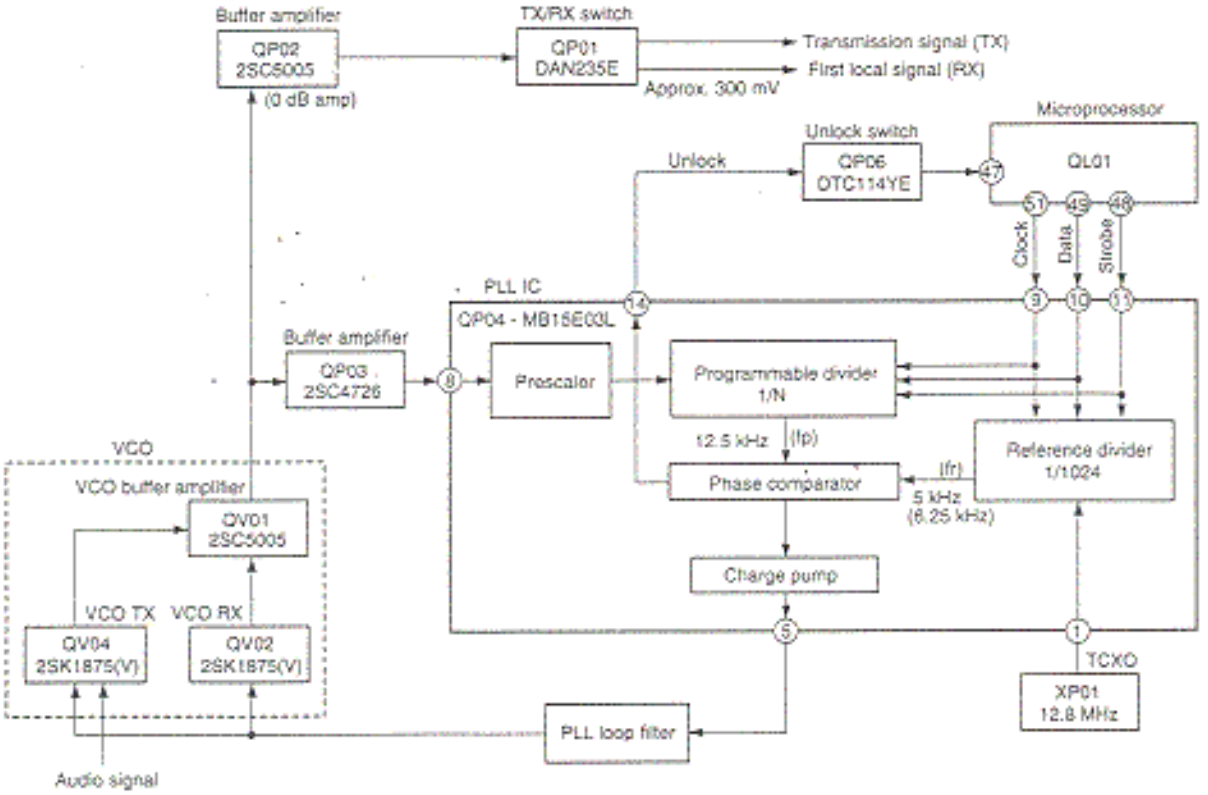

Figure 2-1 PLL block diagram

2.1.1 Programmable Divider

The input oscillation signal is frequency divided by the prescaler using a determined division ratio (1/64 or 1/65). After this, the oscillation signal is input to a programmable divider built into the PLL IC. Based on the data from microprocessor QL01, the programmable divider frequency divides the oscillation signal from the VCO to 1/N to generate a comparison frequency (fp) of 12.5 kHz.

2.1.2 Reference Divider

The reference divider is a circuit that generates a reference frequency (fr) of 12.5 kHz based on data from microprocessor QL01. The 12.8 MHz reference oscillation signal from the TCXO XP01 passes through pin 1 of PLL IC QP04 and is input to the reference divider built into the PLL IC. The 12.8 MHz reference oscillation signal is frequency divided to 1/1,024 to generate a reference frequency of 12.5 kHz.

2.1.3 Frequency Stability Circuit

The PLL frequency stability is determined by the inherent design of oscillator TCXO XP01. This oscillator circuit uses a highly stabilized, temperature controlled crystal oscillator which prevents the maximum frequency variation from exceeding ± 2.5ppm.

2.1.4 Phase Comparator

The phase comparator compares the comparison frequency (fp) and the reference frequency (fr) to determine the phase difference.

2.1.5 Charge Pump

The charge pump circuit charges and discharges the electrical charge accumulated in the PLL loop filter.

2.1.6 PLL loop Filter

The PLL loop filter CR integrates the level signal (square wave) output from the charge pump, converting it into a DC voltage.

2.1.7 VCO Circuit

The DC voltage output by the PLL loop filter is input to a variable capacitance diode built into the VCO. This DC voltage changes the capacitance between the electrodes of the variable capacitance diode, thereby controlling the oscillation signal of the VCO.

2.1.8 Unlock Detect Circuit

The microprocessor QL01 (pin 47) determines whether the status of the PLL circuitry is lock or unlock according to the output level (high or low) from pin 14 of the PLL IC.

If the phase comparator built into the PLL IC detects no phase difference (PLL circuit locked), it produces a high level output. This high level output signal is input to an unlock switch QP06, causing it to turn on. When the unlock switch is on, a low level output signal is input to pin 47 of microprocessor QL01. The low level input causes microprocessor QL02 to determine that the PLL circuit is locked.

If there is a phase difference (PLL circuit unlocked), the phase comparator produces a low level output. This low level output signal is input the unlock switch QP06, causing it to turn off. When the unlock switch is off, a high level output signal is input to pin 47 of microprocessor QL01. The high level input causes microprocessor QL01 to determine that the PLL circuit is unlocked.

2.2 Receiver Block

The reception method is double-conversion superheterodyne with a first IF frequency of 44.95 MHz (Lower) and a second IF frequency of 455 kHz (Lower). The receiver block comprises an RF amplifier circuit, first mixer circuit, first IF amplifier circuit, second IF circuit, and audio circuit.

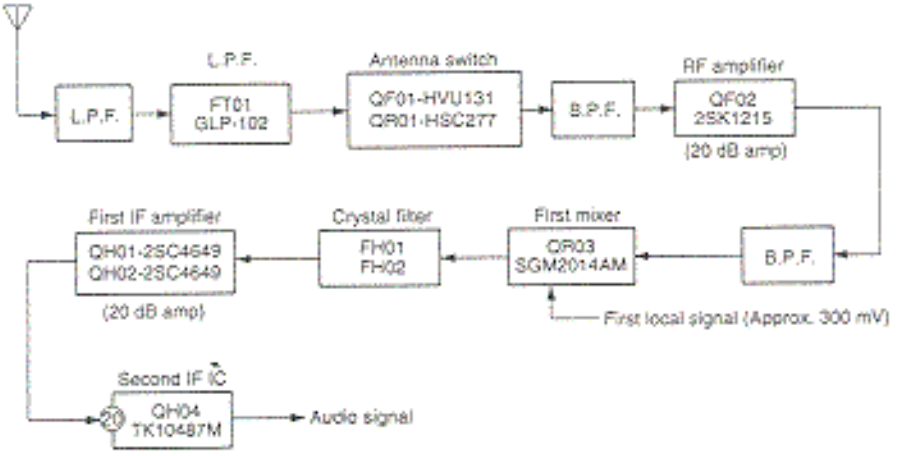

Figure 2-2 Receiver block diagram

2.2.1 RF Amplifier Circuit

The reception frequency amplified by approximately 20 dB by RF amplifier QR02, after which it is input to a band-pass filter consisting of LF04, CF10, LF05, CF12, CF13, LF06, CF14, CF15 CF16 and LF07. At this point, unwanted frequency elements removed by the band-pass filter.

2.2.2 First Mixer Circuit

The reception frequency (frx) is mixed with the first local signal (fvco) from the VCO by first mixer QF03, and first IF signals consisting of their difference are generated.

frx - fvco = 44.95 (MHz)

frx : Reception frequency

fvco : First local signal

2.2.3 First IF Amplifier Circuit

The First IF signal is applied to crystal filters FH01 and FH02 to improve the selectivity and attenuate undesired heterodyne products.

After being amplified by approximately 20 dB by first IF amplifier QH01 and QH02, the 44.95 MHz first IF signal is input to pin 20 of second IF IC QH04.

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2.2.4 Second IF Circuit

The second IF IC comprises a second local oscillator, second mixer, second IF amplifier, wave detector, noise amplifier, and noise wave detector.

The first IF signal passes through pin 20 of second IF IC QH04 and is input to the second mixer built into QH04. The first IF signal and second local signal are mixed, and the first IF signal is converted into a 455 kHz second IF signal. After having adjacent signal elements eliminated by ceramic filter FH03 and FH04 (6 dB bandwidth ±6.0 kHz or greater), the second IF signal is converted into an audio signal by the second IF amplifier and a quadrature wave detector.

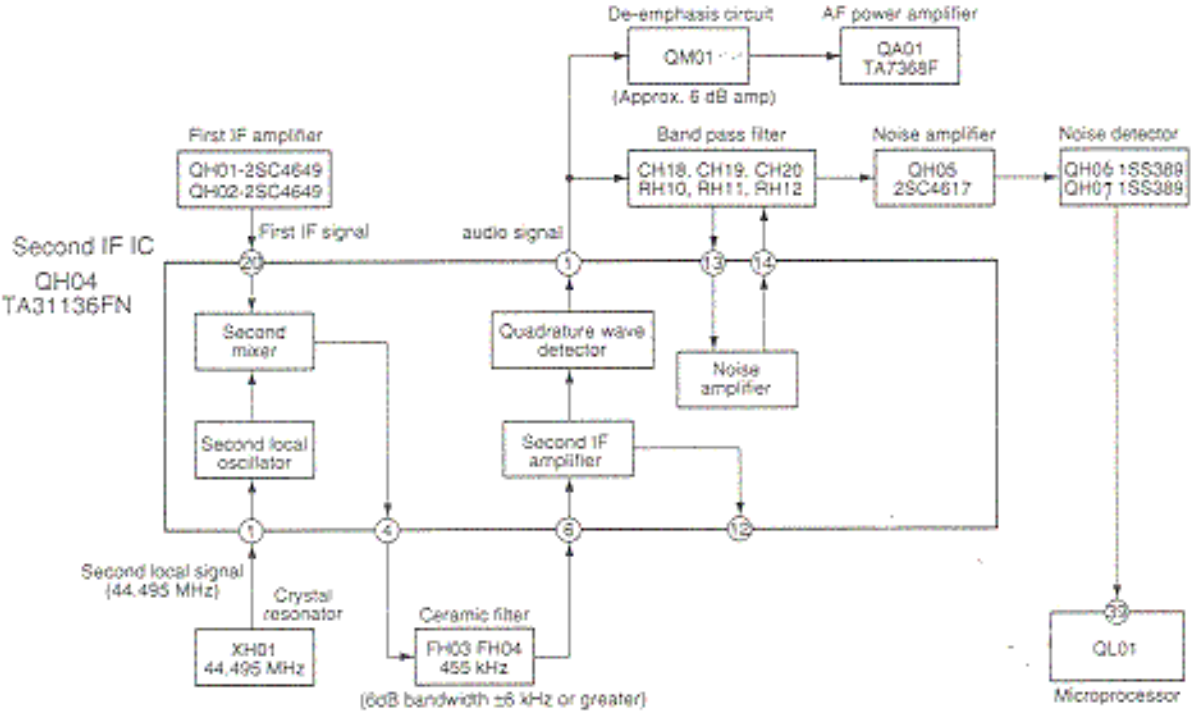

Figure 2-3 Second IF circuit block diagram

2.2.5 Audio Filter/Volume Control

The audio signal detected by the second IF stage passes through a 300 Hz high-pass filter in sub audio IC QS01, which removes any CTCSS and low speed control tones from the recovered audio, and is then presented to pin 7 of main audio IC QM01. Inside QM01, the received signal passes through a de-emphasis circuit and then through an electronic variable resistor to control received audio volume level. A voltage generated by AF volume control SW20 is applied to microprocessor QL01 pin 40. Based on this voltage, QL01 controls the settings of electronic variable resistor in QM01. The received audio signal is output from pin 21 of QM01.

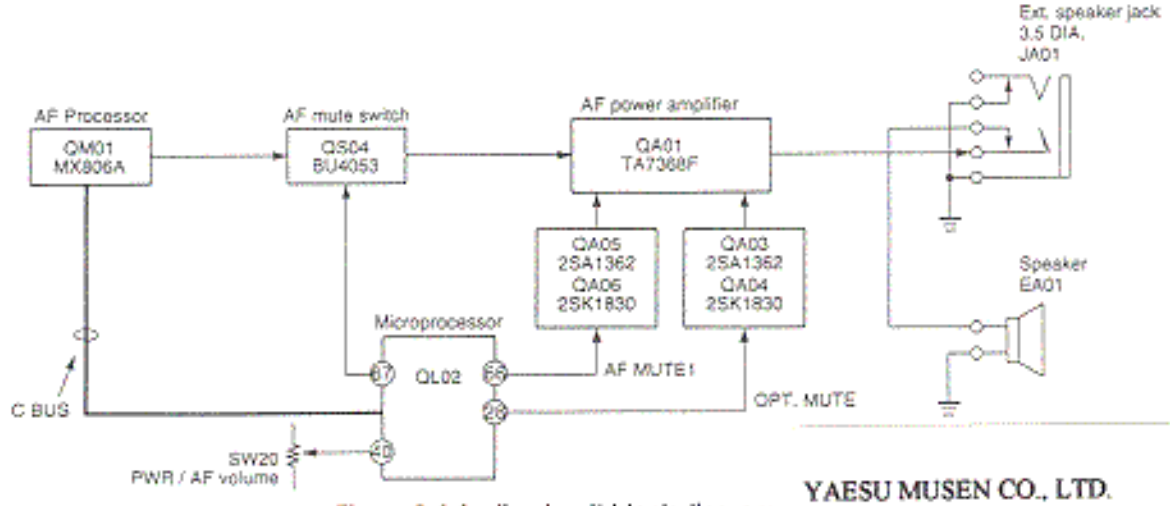

Figure 2-4 Audio circuit block diagram

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2.2.6 Squelch Circuit

A portion of the audio signal output from pin 11 of second IF IC QH04 is input to a band-pass filter consisting of CH18, CH19, CH20, RH10, RH11 and RH12. Noise elements are extracted from the audio signal by the band-pass filter. The noise signal has approximately 40 kHz elements only amplified by a noise amplifier built into QH05 to generate the squelch signal. This squelch signal is converted into a DC signal by the noise wave detector built into QH05, QH06 and then output to pin 39 of QL01.

2.3 Transmitter Block

2.3.1 Microphone Amplifier (Modulation limiting and Roll-Off filter circuit)

Audio signals from the microphone are presented on QS03(pin 3). When the MIC mute signal from QL01 pin 29 output Logic High, the Microphone audio is routed to main audio IC QM01. QM01 contains an amplifier, pre-emphasis circuit, limiter and roll off filter and Modulator driver to both VCO and PLL reference oscillator. The incoming signal is first amplified and then applied to a pre-emphasis circuit which boosts the frequency response between 300 Hz and 3 kHz by 6 dB per octave. And next, the limiter maintains the audio level such that the deviation will not exceed the maximum deviation (±5.0 kHz or ±2.5kHz). Finally, the roll off filter attenuates frequencies above the 3 kHz limit. The audio is then output from QM01 pin 22 to the VCO and pin 23 to the PLL reference oscillator(XP01).

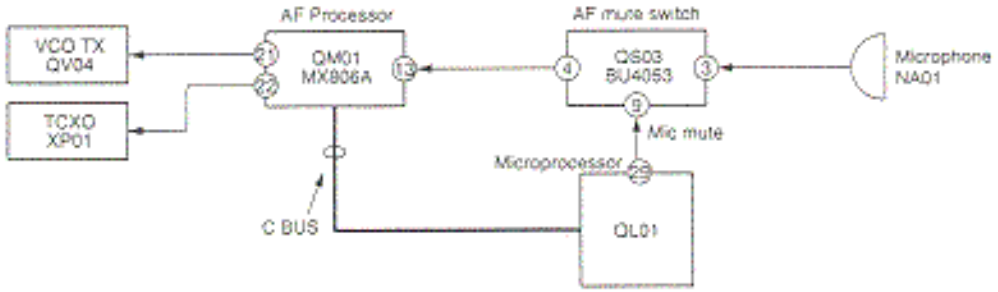


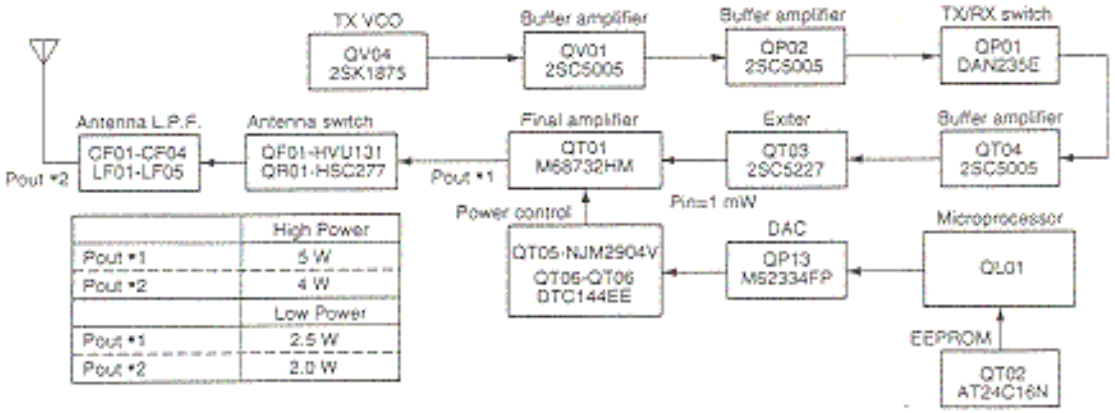
Figure 2-5 Microphone amplifier circuit block diagram

2.3.2 RF Power Amplifier

The output of the VCO is presented to buffer amp QP02 and then to RF switch QP01. Diodes in QP01 act as a TX/RX switch, so that during transmit mode the VCO output is the RF carrier frequency and during receive mode it is the 1st IF injection frequency. From the TX/RX switch, the RF signal is amplified to approximately 1.0 mW by the RF amplifier QT03. And the RF signal is amplified to approximately 5.0 W (High Power), 2.5W(Low Power) by RF power module QT01. The output of QT01 is presented to low-pass filter consisting of [CF01 toCF04, LF01 to LF05], which attenuates unwanted harmonics and spurious radiation. The RF output to the antenna at this point is approximately 4.0 (High Power), 2.0W(Low Power).

2.3.3 Automatic Power Control (APC)

The automatic power control is composed of QT05,QT06, QT07, QT08 and associated components. A portion of the transmitted RF output is sampled by RT12. The result signal is input to QT05 Pin 2 and causes the Power control signal of the QT01 by controlling the Power setting signal from the Analogue to Digital Converter QP13 Pin4 which controlled by Microprocessor QL01 with the stored data at EEPROM QL02. The Power control signal is out from QT05 Pin7 and amplified by QT06 and then input to QT01 as the Power control signal.



	High Power
Pout *1	5 W
Pout *2	4 W
	Low Power
Pout *1	2.5 W
Pout *2	2.0 W

Figure 2-6 Transmission circuit block diagram

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CONTROL CIRCUITS

Microprocessor

The system microprocessor, QL01, processes or controls all functions of radio.

Key Assignment

Key assignment refers to the method by which microprocessor QL01 determines which external key on the radio was pressed.

Keys monitored by the microprocessor, the microprocessor pin monitoring the line, and name of the monitor line, are shown below:

Fixed functional Keys

QL01 Pin #	#20	#41	#42	(*1)
	SHIFT	F1	F2	Key Pad (*2)

(*1) : Key matrix operation QL01 #76 to #79 and #72 to #75
(*2) : Optional Keypad CKP290

Programmable Keys by PPS

QL01 Pin #	#21	#21	#79, #72	#79, #72	#79, #73	#79, #73
	AUX	AUX In Shift mode	H	H In Shift mode	S	S In Shift mode
A/D	–	–	Fixed HOME	Y	Fixed SCAN	Y
TA	–	–		Y		Y
TRANSPOND	–	–		Y		Y
PHONE	Y	Y		Y		Y
MONITOR	Y	Y		Y		Y
H/L	Y	Y		Y		Y
NET	Y	Y		Y		Y

Reset

Switched +7.2Vdc is applied to QC03(which produces ALL+5V), and ALL +5V is applied to reset IC QL03. A logic low reset pulse generated by QL03 is applied to microprocessor QL01 pin #1.

Memory

(1) EEPROM QL02 has 16k bytes of memory, and stores adjustment and backup data, such as SCAN list.
(2) FLASH Memory included QL01 stores the radio control software, channel and operation feature data programmed by PPS. These information can be easily written into memory by external equipment.

LCD (Liquid-Crystal Display)

LCD driver QD01 is controlled by microprocessor QL01. Data controlling the LCD consist of 12 signals: DB0 to DB7, Reset, RS(resister select), R/W (read or write) and E(Enable). The pin connections are shown below:

	DB0 to 7	Reset	RS	R/W	E
QL01	#57, #58 #68, #69 #80, #81 #90, #91	#56	#53	#54	#55
QD01	#44 to #51	#40	#41	#42	#43

LCD Contrast

The LCD contrast circuit includes QL01(microprocessor),QP13(1/4) (ADC: Digital to Analog Converter) and QD01 (LCD driver). Microprocessor QL01 controls the DC output level of QP13 ADC pin #4 via serial data bus (QL01 pin #12, pin #16). And the controlled DC signal is supplied to QD01 pin #38 as the contrast control signal.

SIGNALING

DTMF(encoding)

DTMF signals are produced by microprocessor QL01 (#44, #45). The DTMF signals pass through the amplifier QM02(1/2) and are then supplied to the filter and amplifier circuits of audio processor IC QM01. The signals are supplied to the modulation circuits of both VCO and TCXO. (Refer to description of transmitter)

DTMF(decoding)

DTMF signals are demodulated by QH04 from the received signal. And the received DTMF signals are supplied to QS07 (DTMF receiver) pin #1. The QS07 detects the number of the DTMF signal and communicates with microprocessor QL01 as shown below:

	STD signal detect	SD serial data	ACK acknowledge	PD Power down
QL01	#32	#33	#34	#35
QS07	#9	#10	#7	#2

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CTCSS Eencode

CTCSS tones are produced by signaling audio processor IC QS01. Type of signal is determined by the serial data form microprocessor QL01. After level adjustment and removal of higher harmonics components by signal audio processor IS QS01. CTCSS tones pass through the LPF in QS01 and QS01 pin #9 and are applied to audio processor QM01 pin #18. The CTCSS tone then passes through the amplifier in QM01, and exits on pin 22 and 23. From there, the tones are applied to the modulation circuits of boih VCO and TCXO. (Refer to description of transmitter)

CTCSS Decode

A voice signal(received audio) containing CTCSS tones passes through amplifier QS06 and is supplied to QS01 pin #10 and #16. The voice signal containing CTCSS tones and is passed through a 180/260Hz LPF(Low Pass Filter) in QS01 to allow QS01 pin #17 to output only CTCSS tones.

The CTCSS tone output from QS01 pin #17 is applied to the multiplexer QS04 pin #12. Then output form QS04 pin #14 and is again applied to QS01 pin #14. The tones are amplified, exit at pin #15 and re-enter at pins #19 and #20. At this time, the tones are analyzed for frequency components. Any such detected frequency components are converted into serial data in QS01. Any such detected frequency components are converted into serial data in QS01, and output on pins 4,5,6,7 and 8 to microprocessor QL01. When receives correct CTCSS tones from the antenna, QL01 clears the audio mute mode by controlling AF mute..

DCS Encode

The DCS signal is out from signaling processor QS01 pin #9 after level adjustment. The type of signal output is determined by data output from microprocessor QL01. Any optional DCS produces a DCS signal inside QS01.

The signal from QS01 pin #9 is applied to audio processor QM01 pin #18. The DCS signal is amplified in IC QM01, and exits on pins #22 and #23. From there, the tones are applied to the modulation circuits of both VCO and TCXO. (Refer to description of transmitter)

DCS Decode

A voice signal(received audio) containing DCS signal passes through amplifier QS06 and is supplied to QS01 pin #10 and #16. The voice signal containing DCS signal and is passed through a 180Hz LPF(Low Pass Filter) in QS01 to allow QS01 pin #17 to output only DCS signal.

The DCS signal output from QS01 pin #17 is applied to the multiplexer QS04 pin #12. Then output form QS04 pin #14 and is again applied to QS01 pin #14. The signal is amplified, exit at pin #15 and re-enter at pins #19 and #20. At this time, the signal are analyzed for DCS code. Any such detected frequency components are converted into serial data in QS01. Any such detected frequency components are converted into serial data in QS01, and output on pins 4,5,6,7 and 8 to microprocessor QL01. When receives correct DCS signal from the antenna, QL01 clears the audio mute mode by controlling AF mute.

LTR Data Control

The LTR system is trunking method designed by E.F.Johnson Inc. The signaling rate is 300bps.The signals pass through the same circuits as the DCS signal described previously.

2-TONE Decode

The received 2-tone signal passes through amplifier QS06 and is supplied to QS01 pin #10 and #16. The received audio is passed through a 300Hz HPF(High Pass Filter) in QS01 to allow QS01 pin #11 to output only 2-tone signal.

The 2-tone output from QS01 pin #11 is applied to the multiplexer QS04 pin #13. Then output form QS04 pin #14 and is again applied to QS01 pin #14. The tones are amplified, exit at pin #15 and re-enter at pins #19 and #20. 2-tone signal is output from QS01 pin #21 after converting Logic signal (Square wave) by an amplifier in QS01. The square wave is applied to microprocessor QL01 pin #23. Microprocessor measure the 2 tone frequency and detects the kind of 2-tone code. When receives correct 2-tone from the antenna, QL01 clears the audio mute mode by controlling AF mute or ringing.

HX292UT Microprocessor QL01 PIN Discription

PIN #	SIGNAL NAME	I/O	ACTIVE	Function
1	RES	I	LO	Power on reset
2	XTAL	I	-	System clock oscillator (4.032MHz)
3	EXTAL	I	-	System clock oscillator (4.032MHz)
4	Vcc	I	-	Microprocessor positive supply (+5V)
5	MD1	I	HI	Specified MPU operation mode
6	MD0	I	LO	Specified MPU operation mode
7	NMI	I	LO	Not used
8	STBY	I	LO	Not used
9	Vcc	I	-	Microprocessor positive supply (+5V)
10	X_SHIFT	O	HI	Clock (XL01) shift control output
11	----	O	HI	Not used
12	IIC_SCL	O	-	Serial clock output to EEPROM (QL02) / DAC (QP13)
13	BB_PWR	O	LO	Control output to Power supply of Base band circuit (II BUS clock)
14	PTT_SW	I	LO	PTT input
15	Vss	I	-	Negative ground
16	IIC_SDA	I/O	-	Serial data Input /Output to EEPROM (QL02) / DAC (QP13)
17	CLK_OUT	O	-	Clock output to Base band circuit (QM01)
18	OPT_SEN1	I	LO	Not used
19	WIDE/NALLOW	O	-	Channel space Wide or Narrow selection output
20	KEY_AUX2	I	-	SHIFT key input
21	KEY_AUX1	I	-	AUX key input
22	2TONE_SW	O	-	2-tone decoding control output
23	DET_2TONE	I	-	Reception signal [2TONE/DCS/LTR] input
24	PWR_SW	I	-	Not used
25	TRD/RX NRZ	I	-	Not used
26	TXPOWBCONT	O	HI	Transmitter power supply control output
27	LAMP_CONT	O	HI	LCD, KEYPAD backlight control output
28	OPT_MUTE	O	LO	Optional AF mute output
29	MIC_MUTE	O	LO	Microphone mute control output
30	PLLPOWBCONT	O	HI	PLL power supply control output
31	RXPOWBCONT	O	LO	Receiver power supply control output
32	DTMF_STD	I	HI	DTMF receiver signal detect input
33	DTMF_SD	I	-	DTMF reception 4bit serial data input
34	DTMF_ACK	O	-	DTMF receiver control (4 bit serial clock) output
35	DTMF_PD	O	HI	DTMF receiver power down control output
36	AVref	I	-	ADC (Analog to Digital Converter) reference input
37	AVcc	I	-	ADC positive supply input
38	BATT_CHK	A/D	-	Battery level input (ADC)
39	SQL_WS	A/D	-	Noise squelch level input (ADC)
40	VOL_AF	A/D	-	AF volume level input (ADC)
41	F1 KEY	I	-	F1 key input
42	F2 KEY	I	-	F2 key input
43	INT_CBS	I	-	C-BUS control input (Interrupt request from QS01)
44	DTMF_ENCH	D/A	-	DTMF encoding HI TONE output
45	DTMF_ENCL	D/A	-	DTMF encoding LO TONE output
46	AVss	I	-	Analog ground
47	UNLOCK	I	LO	PLL unlock input
48	PLL_STB	0	I	PLL IC (QP04) control output (strobe)
49	PLL_DATA	0	-	PLL IC (QP04) control output (serial data)
50	BEEP	O	-	BEEP output

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HX292UT Microprocessor QL01 PIN Discription

PIN #	SIGNAL NAME	I/O	ACTIVE	Function
51	PLL_CLK	O	↑	PLL IC (QP04) control output (serial clock)
52	LCD_POWB	O	LO	LCD driver power supply control output
53	LCD_RS	O	–	LCD driver control output (register select)
54	LCD_R/W	O	–	LCD driver control output (HI =read : LO =write)
55	LCD_E	O	HI	LCD driver control output (HI : enable)
56	LCD_RES	O	LO	LCD driver control output(Reset)
57	LCD_DB7	I/O	–	LCD driver DATA #7 input/output
58	LCD_DB6	I/O	–	LCD driver DATA #6 input/output
59	Vcc	I	–	Microprocessor positive supply (+5V)
60	ROT_SW4	I	–	Rotary selector switch (SW17) input #4
61	ROT_SW3	I	–	Rotary selector switch (SW17) input #3
62	ROT_SW2	I	–	Rotary selector switch (SW17) input #2
63	ROT_SW1	I	–	Rotary selector switch (SW17) input #1
64	LED_TX	O	HI	TX LED control output
65	LED_BUSY	O	HI	BUSY LED control output
66	AF_MUTE1	O	LO	AF mute control #1 output (AF main amp. QA01)
67	AF_MUTE2	O	LO	AF mute control #2 output (AF Pre-mute)
68	LCD_DB5	I/O	–	LCD driver DATA #5 input/output
69	LCD_DB4	I/O	–	LCD driver DATA #4 input/output
70	Vss	I	–	Negative ground
71	Vss	I	–	Negative ground
72	KEY_SCN3	O	HI	Key matrix output #3
73	KEY_SCN2	O	HI	Key matrix output #2
74	KEY_SCN1	O	HI	Key matrix output #1
75	KEY_SCN0	O	HI	Key matrix output #0
76	KEY_RET3	I	–	Key matrix input #3
77	KEY_RET2	I	–	Key matrix input #2
78	KEY_RET1	I	–	Key matrix input #1
79	KEY_RET0	I	–	Key matrix input #0
80	LCD_DB3	I/O	–	LCD driver DATA #3 input/output
81	LCD_DB2	I/O	–	LCD driver DATA #2 input/output
82	PLLS/TX NRZ	O	–	Not used
83	PDB/FLT CNT	O	–	Not used
84	TD/NRZ TR	O	–	Not used
85	MSKE	O	–	Not used
86	PRE	O	–	Not used
87	RTM	I	–	Not used
88	RDT	I	–	Not used
89	OPT_SEN2	I	–	Not used
90	LCD_DB1	I/O	–	LCD driver DATA #1 input/output
91	LCD_DB0	I/O	–	LCD driver DATA #0 input/output
92	Vss	I	–	Negative ground
93	CLK_CBS	O	–	C-BUS control output (clock)
94	CMD_CBS	O	–	C-BUS control output (command)
95	CS_CBS	O	LO	C-BUS control output (chip select)
96	RPL_CBS	I	HI	C-BUS control input (reply)
97	TXD	O	–	UART - Serial data output (send)
98	RXD	I	–	UART- Serial data input (receive)
99	BOOT	O	–	System control (enable BOOT mode)
100	RESO	O	–	No connection

Binary input

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HX292UT Power Supply Circuit

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