3. THEORY OF OPERATION

3.1 PLL Block

Refer to Figure 3-1.

The Phase-Locked Loop (PLL) is comprised of a VCO circuit (QV02, QV04, QV05, QV06, and QV07), reference oscillator XP01, PLL IC QP01 and PLL loop filter. Oscillation from the VCO circuit is output from the collector of buffer amplifier QV07, QV09.

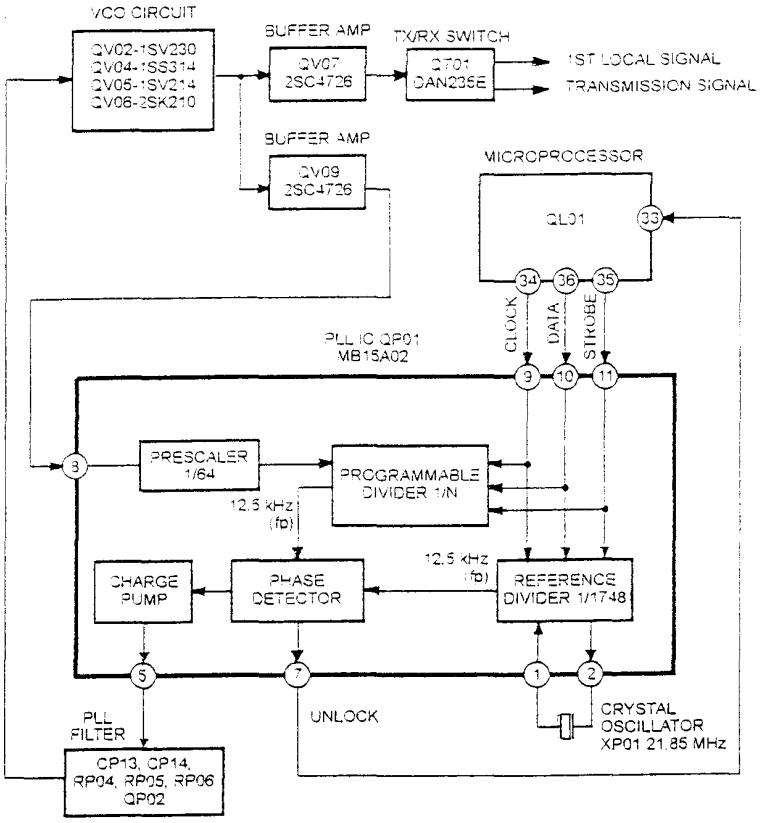

Figure 3-1

3.1.1 Programmable Divider

The microprocessor QL01 determines a divide-by number (N) which is sent to pins 9, 10 and 11 of PLL IC QP01. Inside QP01, the programmable divider divides the VCO frequency by the N number after being supplied to the divide-by-64 prescaler to produce a 12.5 kHz signal. Changing the operating frequency will cause the N number from microprocessor QL01 and the frequency from the prescaler to the programmable divider to change so that the programmable divider is consistently providing a 12.5 kHz signal to the phase detector inside QP01.

3.1.2 Phase Detector

The phase detector compares the phase relationship between the frequency from the programmable divider (fp) and the reference frequency (fr). Based on this phase difference, square wave signals are output from pin 5 of PLL IC QP01 and applied to the PLL filter.

3.1.3 Reference Divider

The 21.850 MHz frequency produced by the crystal oscillator XP01 passes through pin 1 of PLL IC QP01 and is applied to the reference divider inside QP01. The reference frequency (12.5 kHz) is produced by dividing the reference oscillator frequency by 1748. It is then applied to the phase detector in QP01.

3.1.4 PLL Filter

The PLL filter is compose a lag-lead filter and a lag-filter. The PLL filter converts the square wave signal output from pin 5 of QP01 to a DC voltage. This voltage is applied to varactor diode QV02 in the VCO circuit.

3.1.5 Voltage-Controlled Oscillator (VCO)

The VCO circuit is comprised of QV02, QV04, QV05 and QV07 are varactor diode which change capacitance with different bias levels applied (determined by the error voltage from the PLL filter). The change in capacitance causes QV06 to change oscillation frequency. QV04 switches the VCO output between the first local signal during receive (LO = RX frequency -21.4 MHz) and the transmission frequency during transmit. QV05 in conjunction with CV05, LV02, and CV03 controls the deviation during transmit. QV07 is used as the output for the VCO circuit. During receive, pin 16 of microprocessor QL01 outputs a high voltage (5 V) which turns on RX switch QV08. When turned on, the 5V regulator circuit which is comprised of QA12, supplies 5 V to the RX/TX switch circuit which is comprised of QV04, QV01 and QV08, allowing the first LO signal from buffer amplifier QV07 to be applied to first mixer QR02. During transmit, pin 15 of microprocessor QL01 outputs a low voltage (0 V) which turns on RX/TX switch QA08. When turned on, QA08 supplies 5 V to RX/TX switch QT01. The diode inside QT01, that is biased during receive, no longer has voltage applied to it and therefore is no longer active. The other diode inside QT01, which is now receiving 5V from QA08, is conducting. This allows the signal from buffer amplifier QV07 to be applied to the transmitter circuit for amplification. Also during transmit, audio from the microphone is supplied to microphone amplifier QA06 (3/4) and low pass filter QA06 (1/4), applied to potentiometer RA50 for deviation adjustment, then to varactor diode QV05 where the signal is frequency modulated. The modulated signal is applied to QV06 then output from buffer amplifier QV07.

3.1.6 Unlock Detector Circuit

The PLL circuit is locked or unlocked (operational/not operational) depending on the output of pin 7 of PLL IC QP01. When there is no phase difference between the reference and programmable frequencies in the phase detector of PLL IC QP01, the PLL is locked and a hi voltage (5 V) is output from pin 7 of QP01. This voltage is applied to pin 33 of microprocessor PL01, which will stop supplying the N number to PLL IC QP01. When there is a phase difference between the reference and programmable frequencies in QP01, the PLL is unlocked and a low voltage (0 V) is output from pin 7 of PLL IC QP01. Then this low voltage is applied to pin 33 of microprocessor QL01 that will supply the N number to PLL IC QP01.

3.1.7 Weather Alert

QA01 is Weather alert band-pass filter and comparator. In order for QA01 to operate a weather channel needs to be present in the scan memory. This causes a low voltage (0V) to be output from pin 17 of microprocessor QL01 (WA CONT). This voltage is applied to WA switch QA02 which turns it on and applies +5V to pin 8 of Weather Alert band-pass filter QA01.

The Weather alert tone signal is applied to pin 2 of band-pass filter QA01 (1/2) and unwanted signals are eliminated by this circuit. Then the Weather alert tone signal is applied to pin 6 of comparator circuit QA01 (2/2). The weather alert tone signal is passed through the comparator circuit QA01 (2/2) to create a square wave , and is supplied to pin 11 of microprocessor QL01.

When the proper frequency (1050 Hz) is detected by microprocessor QL01, a high voltage (5 V) is output from pin 22 (AF MUTE). Microprocessor QL01 also outputs Weather alert beep from pin 10 (BEEP) which is applied to AF amplifier QA05. This causes a beep tone to be emitted from internal speaker EA01.

3.2 Receiver Block

The receiver is a double-conversion super-heterodyne with a first intermediate frequency (IF) of 21.4 MHz and a second IF frequency of 450 kHz. The receiver consists of RF amplifier QR01, first mixer QR02, first IF amplifier QF01, second IF IC QF02, and AF power amplifier QA05

3.2.1 RF Amplifier Circuit

The incoming signal through the antenna socket JT01 passes through the low-pass filter consisting of LT11, CT29, CT28, LT10, CT27, LT09, CT26, CT25, CT24 and CT23. It then passes through antenna switch QT06 and is applied to the band pass filter LR01. The signal from LR01 is applied to RF amplifier QR01 where it is amplified then applied to the first mixer QR02. The front-end test point may be used to balance the band pass filters or used to check the RF amplifier and associated circuitry.

3.2.2 First Mixer Circuit

The first local signal is applied to the gate of first mixer QR02. The receive frequency and the first local signal are mixed in QR02 and produce four frequencies: the sum, the difference, receive, and first LO (the first LO is equal to the RX frequency – 21.4 MHz.) These signals are applied to the crystal filter, comprised of FF01 and FF02, where the 21.4 MHz signal is filtered. The first IF signal of 21.4 MHz is then applied to first IF amplifier QF01.

3.2.3 First IF Amplifier Circuit

The 21.4 MHz first IF signal is amplified by IF amplifier QF01 and then applied to pin 16 of second IF IC QF02.

3.2.4 Second IF Circuit

In the second mixer, the first IF (21.4 MHz) and second LO (21.850 MHz from XP01) are mixed to produce a 450 kHz second IF signal. The signal passes through pin 3 of QF02 and applied to ceramic filter FF03 to eliminate adjacent signals. It is then applied to pin 5 of QF02 where it is amplified by a second IF amplifier and fed to a quadrature detector where it is converted to audio and output from pin 9.

3.2.5 Audio Circuit

A portion of the audio signal output from second IF IC QF02 is applied to AF pin 6 of high-pass filter QA06 (2/4) and the audio signal is output from pin 7 of QA06. The audio signal passes through pin 12 of AF control switch QA07 and applied to pin 3 of AF low-pass filter QA06(1/4).The audio signal output from pin 1 of AF low-pass filter QA06 (1/4) is applied pin 1 of AF control switch QA07, then input to the de-emphasis circuits RA19 and CA15.The de-emphasis circuits RA19 and CA15 are compensated the frequency of the audio signal and then applied to potentiometer RB01. The audio signal level is adjusted by potentiometer RB01, then input to pin 2 of AF power amplifier QA05. The amplified signal is output from pin 6 of QA05, passes through socket JF02 and drives internal speaker EA01.

3.2.6 Noise Squelch Circuit

A portion of the audio signal output from pin 9 of second IF IC QF02 is applied to the band-pass filter consists of CF08, CF09, RF06, RF07, RF08, RF09 and RF10. The audio signal is then applied to pin 7 of QF02. The noise component of the signal is output from pin 7 of QF02. It is rectified into a DC voltage in noise detector in IF IC QF02 to produce a squelch signal. The voltage of the squelch signal output pin 14 of IF IC QF02, and is applied to pin 5 of microprocessor QL01. The voltage is compared with the adjusted squelch level. Then be controlled pin 21(AF AMP CONT) and pin 22(AF MUTE). When the voltage output from pin 4 of IF IC QF02, is more high than the adjusted squelch level, squelch is in operation (no sound is emitted from the transceiver.). When the voltage output from pin 14 of IF IC QF02, is more low than squelch level, squelch is off (noise is emitted from the transceiver.)

3.3 Transmitter Block

3.3.1 Microphone Amplifier

When the push-to-talk switch (PTT) SL03 is pressed, a low voltage (0V) is applied to pin 8 of microprocessor QL01 (PTT). When this happens, pin 14 of microprocessor QL01 (TX PO CONT) outputs a low voltage (0 V) which turns on TX+B switch QA08 to supply TX +B to the transmit circuits. Microphone audio is applied to the microphone amplifier/limiting QA06 (3/4) then to pin 13 of AF control switch QA07. The limited signal is applied to pin 3 of low-pass filter QA06 (1/4). QA06 contains a low-pass filter that attenuates audio signals higher than 3 kHz by 18 dB/oct. The frequency of the microphone audio is compensated and then the signal level is adjusted by Deviation Adjustment RA50 and applied to varactor diode QV05 to modulate the VCO.

3.3.2 Buffer Amplifier / Driver / Exciter

Refer to Figure 3-2.

The modulated transmit signal is output from QV06 of the VCO circuit and applied to buffer amplifier QV07. The amplified signal passes through TX/RX switch QT01 and is applied to amplifier comprised of driver QT02 and exciter QT03 which will amplify the signal from 1 mW to 1000 mW. The amplified signal is then applied to the final power amplifier QT04.

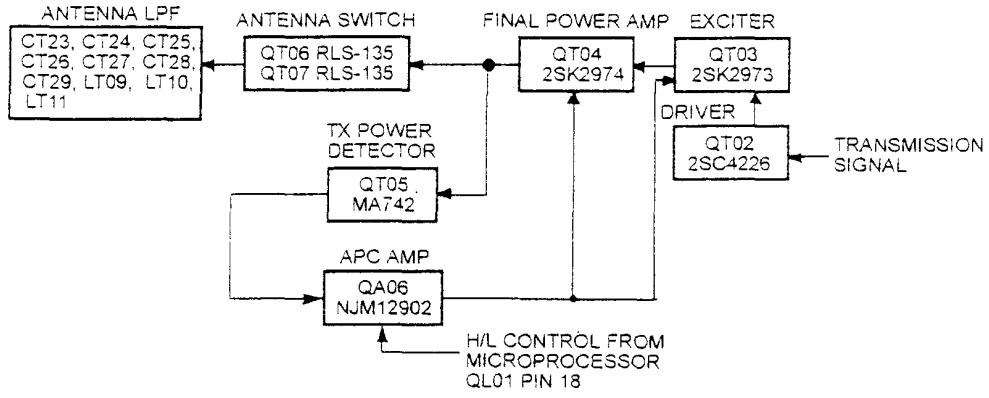

Figure 3-2

3.3.3 Final Power Amplifier

The transmit signal supplied by QT03 is further amplified to the desired level by final power amplifier QT04. The transmit signal output from QT04 passes through a low pass filter comprised of CT23 – CT29 and LT09 – LT11 to eliminate harmonics and spurious signals. The signal then passes through antenna socket JT01 and is output through the antenna.

3.3.4 High/Low Power

The RF power can be set to either 1 watt (LOW POWER) or 5 watts (HIGH POWER) by the H/L key on the front of the transceiver. If 1 watt is selected, a low voltage (0 V) is output from pin 18 of microprocessor QL01 (HI/LO CONT), and applied to pin 13 of APC amplifier QA06 (4/4) pass though QT09. This causes the automatic power control (APC) circuit to supply a lower signal level to the final power amplifier QT04 so that the output is 1 watt. When 5 watts is selected, a high voltage (5 V) is output from pin 18 of microprocessor QL01 (HI/LO CONT), and applied to pin 13 of APC amplifier QA06 (4/4). This causes the APC circuit to stop operating and final power amplifier QT04 will have an output of 5 watts.

3.3.5 APC (Automatic Power Control) Circuit

When the transceiver is TX mode, a portion of the transmit signal output from final amplifier QT04 is applied to TX power detector QT05 which converts it to a DC voltage. The APC amp QA06 (4/4) compare with an applied DC voltage from pin 18 of microprocessor QL01 (HI/LO CONT) and an applied DC voltage from TX power detector QT05. Then the compare voltage output from pin14 of APC amplifier QA06 (4/4), and applied to the final power amplifier QT04 and exciter QT03.

3.4 Control Circuit Block

3.4.1 Microprocessor

The microprocessor QL01 controls all the functions of the transceiver.

The functions of QL01 are listed below. Table 3-1

Pin No.	I / O	Port name	Active	Initial	Pull up/Pull down	Function
1	I	KEY1	— —	— —	— —	Front key input 1
2	I	KEY2	— —	— —	— —	Front key input 2
3	I	KEY3	— —	— —	— —	Front key input 3
4	I	BATT CHK	— —	— —	— —	Battery voltage input
5	I	SQL DET	— —	— —	— —	SQL input terminal
6	I	TX DET	— —	— —	— —	TX DET input terminal
7	O	NC	— —	L	EXT UP	Not used
8	I	PTT SW	L	H	EXT UP	PTT input terminal
9	O	WA BEEP CONT	H	L	EXT UP	BEEP control terminal
10	O	BEEP OUT	— —	L	— —	BEEP output terminal
11	I	WA DET	— —	— —	INT UP	WA detector input terminal
12	I	NC	L	H	INT UP	Not used
13	I	TEST SW	L	H	INT UP	TEST mode on / off switching
14	O	TX PO CONT	L	H	EXT UP	TX+B power supply control
15	O	SAVE CONT	H	L	EXT UP	SAVE+B power supply control
16	O	TX/RX CONT	L	H	— —	TX+B/SAVE+B power supply control
17	O	WA CONT	L	H	— —	WA power supply control
18	O	H/L CONT	H	H	— —	TX hi / low power control
19	O	TXD	— —	L	— —	UART DATA output
20	I	RXD	— —	— —	INT UP	UART DATA input
21	O	AF AMP CONT	H	L	EXT DN	AF AMP power supply control
22	O	AF MUTE	L	L	EXT DN	AF mute control
23	O	NC	— —	L	— —	Not used
24	I	NC	— —	— —	EXT DN	Not used
25	I	RESET	— —	— —	— —	Reset signal input
26	O	NC	— —	L	— —	Not used
27	O	NC	— —	L	— —	Not used
28	I	XIN	— —	— —	— —	4.19MHz crystal oscillator input
29	O	XOUT	— —	— —	— —	4.19MHz crystal oscillator output
30	I	Vss	— —	— —	— —	Ground terminal
31	O	NC	— —	L	— —	Not used
32	O	NC	— —	L	— —	Not used
33	I	PLL_UL	L	— —	EXT DN	Lock : Hi Unlock : Low
34	O	PLL_CLK	— —	L	— —	PLL CLK output terminal
35	O	PLL_STB	H	L	— —	PLL STB output terminal
36	O	PLL_DATA	— —	L	— —	PLL DATA output terminal
37	I	DO	— —	— —	INT UP	Serial data input terminal
38	O	DI	— —	L	— —	Serial data output terminal
39	O	SK	— —	L	— —	Serial clock output terminal

40	O	CS	H	L	EXT DN	Chip select output terminal

Pin No.	I / O	Port name	Active	Initial	Pull up/Pull down	Function
41	O	NC	H	H	— —	Not used
42	O	NC	H	H	— —	Not used
43	O	NC	H	H	— —	Not used
44	O	NC	H	H	— —	Not used
45	O	LAMP CONT	H	L	EXT DN	LAMP control
46	O	NC	H	H	— —	Not used
47	O	SEG 0	— —	— —	— —	Segment 0 output terminal
48	O	SEG 1	— —	— —	— —	Segment 1 output terminal
49	O	SEG 2	— —	— —	— —	Segment 2 output terminal
50	O	SEG 3	— —	— —	— —	Segment 3 output terminal
51	O	SEG 4	— —	— —	— —	Segment 4 output terminal
52	O	SEG 5	— —	— —	— —	Segment 5 output terminal
53	O	SEG 6	— —	— —	— —	Segment 6 output terminal
54	O	SEG 7	— —	— —	— —	Segment 7 output terminal
55	O	SEG 8	— —	— —	— —	Segment 8 output terminal
56	O	SEG 9	— —	— —	— —	Segment 9 output terminal
57	O	SEG 10	— —	— —	— —	Segment 10 output terminal
58	O	SEG 11	— —	— —	— —	Segment 11 output terminal
59	O	SEG 12	— —	— —	— —	Segment 12 output terminal
60	O	SEG 13	— —	— —	— —	Segment 13 output terminal
61	O	SEG 14	— —	— —	— —	Segment 14 output terminal
62	O	SEG 15	— —	— —	— —	Segment 15 output terminal
63	O	SEG 16	— —	— —	— —	Segment 16 output terminal
64	O	SEG 17	— —	— —	— —	Segment 17 output terminal
65	O	SEG 18	— —	— —	— —	Segment 18 output terminal
66	O	SEG 19	— —	— —	— —	Segment 19 output terminal
67	O	SEG 20	— —	— —	— —	Segment 20 output terminal
68	O	SEG 21	— —	— —	— —	Segment 21 output terminal
69	O	SEG 22	— —	— —	— —	Segment 22 output terminal
70	— —	SEG 23	— —	— —	— —	Segment 23 output terminal
71	— —	VCC	— —	— —	— —	Power supply terminal
72	— —	VREF	— —	— —	— —	A/D power supply terminal(connected to Vcc)
73	— —	Avss	— —	— —	— —	Ground terminal
74	— —	NC	— —	— —	— —	Not used
75	— —	NC	— —	— —	— —	Not used
76	O	COM2	— —	— —	— —	Common 2 output terminal
77	O	COM1	— —	— —	— —	Common 1 output terminal
78	I	VL3	— —	— —	— —	LCD drive voltage (connected to Vcc)
79	O	VL2	— —	— —	— —	LCD drive voltage (connected to VL1)
80	O	VL1	— —	— —	— —	LCD drive voltage (connected to VL2)

3.4.2 EEPROM

EEPROM QL02 stores the data supplied by microprocessor QL01 that control channels placed into scan memory, the channel that the transceiver was set to when it was turned off. And stores the initial data that is the TX H/L power data, the squelch level data. QL02 will store this data even when no voltage is supplied to it.

3.4.3 Lamp Control

When the LAMP/KEYLOCK key is pressed, a high voltage (5 V) is output from pin 45 of microprocessor QL01 (LAMP CONT). This causes lamp switch QL09 to turn on and the lamp to light. After 5 seconds, the output of pin 45 of microprocessor QL01 (LAMP CONT) will return to a low voltage level (0 V). This will cause lamp switch QL04 to turn off and the lamp will also turn off.

3.5 Power Supply Block

7.2V DC is supplied to the transceiver through battery terminal. This voltage is applied to various circuits in the transceiver after passing through power switch RB01.

3.5.1 +B Power Supply

Once the +7.2 V (DC) has passed through power switch RB10, it is supplied to AF amplifier QA05, final power amplifier QT04, the +5 V regulator of QA12 and the +5 V regulator of QL06.

3.5.2 +5V Regulator

+5V Regulator QL06 of the control P.C.B supply the +5 V to operate microprocessor QL01, reset IC QL05, EEPROM QL02. +5V Regulator QA12 of the main P.C.B supply the +5 V to PLL IC PL01, VCO QV06, buffer amplifiers QV07/QV09, microphone amplifier/LPF/HPF/APC amplifier QA06 RX/TX switch QT01, AF control switch QA07, WA switch QA02.