FTA-250 Circuit Description

Receive Signal Path

Incoming RF from the antenna jack is passed through a low-pass filter and high-pass filter consisting of coils L1025, L1026, L1027, L1030, L1031 & L1032, capacitors C1266, C1268, C1269, C1270, C1271, C1272, C1273, C1276, C1277, C1280,C1281, C1282, C1283 & C1284 and antenna switching diodes D1038 and D1039 to the receiver front end section.

Signals within the frequency range of the transceiver is applied to the receiver front end which contains RF amplifier Q1054 and varactor-tuned band-pass filter consisting of coils L1018, L1021, L1022, L1028 & L1029, capacitors C1233, C1234, C1235, C1237, C1244, C1245,C1247, C1249, C1255, C1261, & C1264, and diodes D1035, D1036, D1037 & D1041, then applied to the 1st mixer Q1050.

Buffered output from the VCO is amplified by Q1039 to provide a pure 1st local signal between 165.25 and 210.525 MHz for injection to the 1st mixer. The 47.25 MHz 1st mixer product then passes through monolithic crystal filter XF1001 (4.0 kHz BW) or XF1002 (7.5 kHz BW) which strips away all but the desired signal, which is then amplified by mixer post-amp Q1043.

The amplified 1st IF signal is applied to the AM/FM IF subsystem IC Q1040, which contains the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier and AM/FM detector.

A 2nd local signal is generated by 11.7 MHz TCXO X1001 .The11.7MHz signal mixed with the 1st IF signal within Q1040. The 2nd IF then passes through the ceramic filter CF1001(2.0 kHz BW) or CF1002(7.5 kHz BW) to strip away unwanted mixer products.

In the FM mode, a 2nd IF signal from the ceramic filter CF1002 applied to the limiter amplifier section of Q1040, which removes amplitude variations in the 450 kHz IF before detection of the speech by the ceramic discriminator CD1001. Detected audio from Q1040 is passed through the de-emphasis, consisting of the resistors R1115, capacitors C1115.

In the AM mode, detected audio from Q1040 is passed through the audio amplifier Q1042-2 and ANL circuit, then applied to the Digital signal processor Q1045. When impulse noise received, a portion of the AM detector output signal from the AM/FM IF subsystem Q1040, including pulse noise is rectified by D1032. The resulting DC is applied to the ANL MUTE gate Q1040, thus reducing the pulse noises.

The processed audio signal from Q1045 is passed through the volume control IC Q1024, AF amplifier Q1021 and audio power amplifier Q1006, providing up to 0.7 Watts to 16ohm loudspeaker.

A portion of the AF signal from the AM/FM IF subsystem Q1040 converted into DC voltage within the IC, and provide to the inversion amplifiers Q1052 and Q1055. These amplifier reduce the amplifier gain of the RF amplifier Q1054 while receiving a strong signal.

Squelch Control

When signal is received, appear the DC squelch control voltage at pin 16 of AM/FM IF subsystem Q1040 according to the receiving signal strength. This DC is applied to pin 68 of microprocessor Q1020.

The DC squelch control voltage is compared with the SQL threshold level by the microprocessor Q1020. If the DC squelch control voltage is lower, microprocessor Q1020 control the volume control IC Q1024. and pin24 of Q1024 goes low. thus disabling the AF audio.

Also, the microprocessor stops scanning, if active, and allows audio to pass through the the volume control IC Q1024.

Transmit Signal Path

Speech input from the microphone applied to the Digital signal processor Q1045, process ALC, high-pass filter, low-pass filter. The processed speech signal adjust the modulation level, then fed to the AM modulator Q1051.

When using the optional headset, the SIDETONE signal from J1001 becomes “HIGH”, turning Pin58 of Q1020 on; pin 59 of Q1020 therefore a portion of the speech signal applied to the AF power amplifier Q1006 as a monitor signal.

The carrier signal from the VCO Q1036 passes through the buffer amplifier Q1039 and TX/RX switch D1029.

The signal from D1029 is amplified by Q1046 and Q1049, and ultimately applied to the final amplifier Q1051 which increases the signal level up to 5 watts output power. The transmit signal then passes through the antenna switch D1038, and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

Automatic Transmit Power Control

RF power output from the final amplifier is sampled by C1260/C1265 and is rectified by D1040. The resulting DC is fed through the Automatic Power Controller Q1053, thus allowing control of the power output.

Transmit Inhibit

When the transmit PLL is unlocked, pin 7 of PLL chip Q1023 goes to a logic low. The resulting DC “unlock” control voltage is switches off TX inhibit switches Q1010, to disable the supply voltage to transmitter RF amplifiers Q1046, disabling the transmitter.

Spurious Suppression

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency. Additional harmonic suppression is provided by a low-pass filter consisting of L1026, L1027 & L1031 and C1266, C1268, C1271, C1273 and C1278, resulting in more than 60 dB of harmonic suppression prior to delivery of the RF signal to the antenna.

PLL Frequency Synthesizer

PLL circuitry consists of VCO Q1030 and Q1036, VCO buffer Q1039, and PLL subsystem IC Q1023, which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and charge pump.

Stability is maintained by the 11.7 MHz frequency reference TCXO X1001.

In the receive mode, VCO Q1030 oscillates between 165.25 and 210.525 MHz. The VCO output is buffered by Q1039, and applied to the prescaler section of Q1023. There the VCO signal is divided by 32 or 33, according to a control signal from the data latch section of Q1023, before being applied to the programmable divider section of Q1023. The data latch section of Q1023 also receives serial dividing data from the microprocessor Q1020, which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 12.5 kHz derivative of the current VCO frequency.

Meanwhile, the reference divider section of Q1023 divides the 11.7 MHz crystal reference from the reference oscillator section by 936 to produce the 12.5 kHz loop reference. The 12.5 kHz signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1023, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is filtered to DC and returned to the varactor D1011 and D1012.

Changes in the level of the DC voltage applied to the varactors affect the reactance in the tank circuit of the VCO, changing the oscillating frequency of the VCO according to the

phase difference between the signals derived from the VCO and the crystal reference oscillator. The VCO is thus phase-locked to the crystal reference oscillator.

The output of the VCO Q1030 is buffered by Q1039 before application to the 1st mixer, as described previously.

For transmission, the VCO Q1036 oscillates between 118 and 137 MHz. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the receiving case).

Receive and transmit buses select which VCO is made active by Q1028 (RX) or Q1035 (TX).

When the power saving feature is active, the microprocessor periodically signals to the PLL IC Q1023 to conserve power, and to shorten lock-up time.

Push-To-Talk Transmit Activation

The PTT switch on the microphone is control to pin 44 and 52 of microprocessor Q1020, so that when the PTT switch is closed, pin 55 of Q1020 goes high, pin 56 of Q1020 gose low. This signals cut off the receiver by disabling the 5 V supply bus at Q1011 which feeds the front-end, FM/AM IF subsystem IC Q1040, and receiver VCO circuitry. At the same time, Q1010 activates the transmit 5 V supply line to enable the transmitter.