GX2000 / GX2100 Circuit Description

Reception and transmission are switched the MPU IC **Q2004** on the CNTL Unit. The receiver uses double-conversion superheterodyne circuitry, with a 21.7 MHz 1st IF and 450 kHz 2nd IF. The 1st local is produced by a PLL synthesizer, yielding the 21.7 MHz 1st IF. The 2nd local uses a 21.250 MHz crystal oscillator, yielding the 450 kHz 2nd IF. The 2nd mixer and other circuits use a custom IC to convert and amplify the 2nd IF and detect FM to obtain demodulated signals. During transmit, the PLL synthesizer oscillates at the desired frequency directly, for amplification to obtain RF power output. During transmit, voice modulation is applied to this synthesizer. Transceiver functions, such as TX/RX control, PLL synthesizer settings, and channel programming, are controlled using the MPU.

RECEIVER

Incoming RF signals from the antenna connector are delivered to the RF Unit, and pass through a low-pass filter (LPF) consisting of coils L1001 & L1002 and capacitors C1002,C1008,C1022&C1023, and antenna switching diode **D1003・D1004** for delivery to the receiver front end.

Signals within the frequency range of the transceiver are then passed through a SAW filter **XF1001**, before RF amplification by **Q1020**.

The amplified RF is then passed through a SAW filter **XF1001**, the pure in-band input signal is delivered to 1st DBM mixer consisting of **D1016** & T1001 & T1002.

Buffered output from the VCO is amplified by **Q1023** and low-pass filtered by coils L1012 and capacitors C1099, C1105,C1091 & C1109 to provide a pure 1st local signal between 134.35MHz and 141.575 MHz for delivery to the 1st DBM mixer consisting of **D1016(HSB88WS)** & T1001 & T1002.

The 21.7 MHz 1st mixer product then passes through monolithic crystal filters **XF1004 & XF1005** , and is amplified by **Q1040** and delivered to the input of the FM IF subsystem IC **Q1042**. This IC contains the 2nd mixer, 2nd local oscillator, limiter amplifier, FM detector, noise amplifier, and squelch gates.

The 2nd local in the FM IF subsystem IC is produced from TCXO **X1001** (21.250 MHz), and the 1st IF is converted to 450 kHz by the 2nd mixer and stripped of unwanted components by ceramic filter **CF1001**.

After passing through a limiter amplifier, the signal is demodulated by the FM detector. Demodulated receive audio from the FM IF subsystem IC is amplified by **Q1004**.

The audio signal is passed through the AF Mute switch **Q1036** & amplifier **Q1002** & the Electoric Volume **Q1045** , to the AF power amplifier **Q1049**, the audio signal is

delivered to the 16 Ohm internal loudspeaker and external Speaker terminal in the accessory cable.

PLL SYNTHESIZER

The 1st Local signal maintains stability from the PLL synthesizer by using a 21.250 MHz reference signal from TCXO **X1001**. PLL synthesizer IC **Q1035** consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data, a phase comparator, and a charge pump.

The PLL synthesizer IC divides the 21.250 MHz reference signal by 1700 using the reference counter (12.5 kHz comparison frequency). The reference oscillator feeds to the PLL synthesizer IC **Q1035**. for the 2nd local signal.

The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator, and applied to the charge pump.

A voltage proportional to their phase difference is delivered to the low-pass filter circuit, then fed back to the VCO as a voltage with phase error, controlling and stabilizing the oscillating frequency. This synthesizer also operates as a modulator during transmit.

The VCO is consisted of **Q1029** and varactor diodes **D1013**, **D1015**, which oscillates at 21.7 MHz below from the receiving frequency. The VCO output passes through buffer amplifier **Q1026,Q1023** to obtain stable output, then applied to the 1st DBM mixer consisting of **D1016** & T1001 & T1002. The DC supply for the VCO is regulated by **Q1022** .

TRANSMITTER

Voice audio from the microphone is delivered via the **MIC** connector to the MAIN Unit. After passing through microphone amplifier **Q1003** , a pre-emphasis network, limiter (IDC: instantaneous deviation control), and low-pass filter network **Q1003** , the audio is adjusted for optimum deviation level and delivered to the next stage.

Voice or DSC (Digital Selective Calling) encode signal inputs from the low-pass filter network **Q1003** is by the VCO **Q1029** and varactor diode **D1013**, **D1015**, which oscillates the fundamental transmit frequency with direct frequency-modulation using varactor diode **D1014**. The modulated signal passes through buffer amplifier **Q1026** and **Q1023** , diode switch **D1007** to drive amplifiers **Q1016** and RF power amplifier module **Q1014** .

The RF energy then passes through antenna switch **D1003** and low-pass filter (LPF) consisting of coils L1001 & L1002 and capacitors C1002, C1008, C1022 & C1023 and finally to the antenna connector.

RF output power from the RF power amplifier module **Q1014** is sampled by C1013 and C1019 and is rectified by **D1002** . The resulting DC is fed through Automatic Power Controllers **Q1001** to RF power amplifier module **Q1014** , thus providing positive control of the power output.

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of coils and capacitors, resulting in more than 70 dB of harmonic suppression prior to delivery of the RF energy to the antenna.

DSC Encoder/ Decoder

Encoder

The DCS (Digital Selective Calling) encode signal which D/A converted in the MPU IC **Q2004** on the CNTL Unit is fed through the low-pass filter **Q1003** on the MAIN Unit to the VCO **Q1029** .

Decoder

The receiving DCS code is demodulated by the FM IC **Q1046**, then fed through the low-pass filter **Q1052** to the DCS Decoder IC **Q1043** which the receiving DCS code is decoded. The decoded DCS signal delivered to the MPU IC **Q2004**

1050 Hz Weather Alert Decoder

1050 Hz Weather Alert signal from the FM IF subsystem IC **Q1042** is demodulated by **Q1004** then is applied to the 8-bit MPU IC **Q2004** on the CNTL Unit. AIS-Receiver Description

MPU

Operation is controlled by 8-bit MPU IC **Q2004** . The system clock uses a 9.8304 MHz crystal for a time base.

EEPROM

The EE-PROM **Q2005** retains TX and RX data for all memory channels, prescaler dividing, IF frequency, local oscillator injection side, and reference oscillator data

AIS-Receiver Description (GX2100)

The RF signal via J4001 from the MAIN-UNIT is supplied to AIS-UNIT, and it is amplified in LNA **Q4011** through the SAW FILTER **XF4001**. The amplified signal goes through the SAW FILTER **XF4002**, and it is divided in RX (CH1) and RX (CH2).
The 1st local signal (229.625MHz) from VCO1 **Q4006** and the RF signal (161.975MHz) divided in RX (CH1) are delivered to the 1st mixer **Q4019** to generate the 1st IF signal (67.65MHz). The 1st IF signal is amplified in the IF amplifier **Q4023** after unwanted signals were filtered in CF **XF4004**. In the FM IF IC **Q4025**, the 1st IF signal and the 2nd local signal (67.20MHz) from the TCXO **X4001** are delivered to the 2nd mixer to generate the 2nd IF signal (450kHz). The 2nd IF signal is amplified with the limiter amplifier after unwanted signals were filtered in the ceramic filter **CF4001**, and it is demodulated at the quadrature detector with the ceramic discriminator **CD4001**. The demodulated signal is delivered to the AIS IC **Q4020** to decode the AIS signal (CH1).

Similarly, the 1st local signal (200.875MHz) from VCO2 **Q4007** and the RF signal (162.025MHz) divided in RX (CH2) are delivered to the 1st mixer **Q4018** to generate the 1st IF signal (38.85MHz). The 1st IF signal is amplified in the IF amplifier **Q4022** after unwanted signals were filtered in MCF **XF4003**. In the FM IF IC **Q4026**, the 1st IF signal and the 2nd local signal (38.40MHz) from the TCXO **X4002** are delivered to the 2nd mixer to generate the 2nd IF signal (450kHz). The 2nd IF signal is amplified with the limiter amplifier after unwanted signals were filtered in the ceramic filter **CF4002**, and it is demodulated at the quadrature detector with the ceramic discriminator **CD4002**. The demodulated signal is delivered to the AIS IC **Q4020** to decode the AIS signal (CH2).

2. PLL Frequency Synthesizer

The AIS IC **Q4020** has two PLL synthesizers, and each consists of a programmable divider, a phase comparator and a charge pump. The reference clock (19.2MHz) is common with a system clock of the AIS IC **Q4020** and is supplied from the TCXO **X4002**. This TCXO has a stability of ±5ppm (-20 to +60℃).

VCO1 **Q4006** oscillates at 229.625MHz, and this local signal is amplified with a buffer amplifier **Q4003**. The amplified local signal is fed back to the AIS IC **Q4020** and divided by a programmable divider. In the AIS IC, a reference divider divides the reference signal (19.2MHz) by 1,536 to generate the comparison frequency of 12.5 kHz. The divided local signal is compared with the comparison frequency with a phase comparator, and a charge pump is controlled to make the control voltage VCV1. The

PLL loop is formed by controlling VCO1 by VCV1.

VCO2 **Q4007** oscillates at 200.875MHz, and this local signal is amplified with a buffer amplifier **Q4004**. The amplified local signal is fed back for the AIS IC **Q4020** and divided by a programmable divider. The divided local signal is compared with the comparison frequency with a phase comparator, and a charge pump is controlled to make the control voltage VCV2. The PLL loop is formed by controlling VCO2 by VCV2.

3. AIS Decoder IC

The AIS IC **Q4020** can watch two channels simultaneously because it has two GMSK decoder and two PLL blocks. The AIS IC outputs the decoded AIS signal from its serial port to the CNTL-UNIT.