HX400 Circuit Description

1. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 67.65 MHz and a second IF of 450 kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 67.65 MHz.

This is then mixed with the 67.2MHz second local oscillator output to produce the 450 kHz second IF. This is detected to give the demodulated signal.

The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. FRONT-END RF AMPLIFIER

Incoming RF signal from the antenna is delivered to the Main Unit and passes through Low-pass filter, high-pass filter and removed undesired frequencies by varactor diode (tuned band-pass filter) **D1012** and **D1013** (both **1SV325**).

The radio signal is supplied to the RF amplifier **Q1025** (**2SC5006**) amplified, applied to a tuned band pass filter. The signal is then applied to the first mixer.

2-2. FIRST MIXER

The 1st mixer consists of the **Q1036** (**3SK293**). Buffered output from the RX VCO **Q1040** (**2SK508**) is amplified by **Q1038** (**2SC5005**) to provide a pure first local signal between 223.675 and 230.925 MHz (Marine Band) or 201.650 and 241.650 MHz (LMR Band) for injection to the first mixer.

The IF signal then passes through monolithic crystal filter **XF1001** (±7.5 kHz BW) to strip away all but the desired signal.

2-3. IF AMPLIFIER

The first IF signal is amplified by **Q1041** (**2SC4215Y**). The amplified first IF signal is applied to FM IF subsystem IC **Q1046** (**BA4116FV**) which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and RSSI amplifier.

The signal from reference oscillator X1003 is applied to FM IF subsystem IC **Q1046** (**BA4116FV**) which increase the frequency by 4 times, mixes with the First IF signal to become the Second IF 450kHz.

The second IF then passes through the ceramic filter **CF1001** (**LTM450GW** for Wide band) or **CF1002** (**LTM450FW** for Narrow band) to strip away unwanted mixer products, and is applied to the limiter amplifier in **Q1046** (**BA4116FV**), which removes amplitude variations in the 450 kHz IF, before detection of the speech by the ceramic discriminator **CD1001** (**JTBM450CX24**).

2-4. AUDIO AMPLIFIER

Detected signal from **Q1046** (**BA4116FV**) is applied to De-Emphasis circuit **Q1009-3/-4** (**LM2902PW**). The signal which appeared from **Q1009** (**LM2902PW**) is fed through the Scrambler IC **Q1049** (**CMX264**) and the buffer amplifier **Q1009-1** (**LM2902PW**) to the AF volume (**VR1001**). The audio signal is applied to audio amplifier **Q1005** (**TDA2822L**). The output signal from **Q1005** (**TDA2822L**) is in audio speaker.

2-5. SQUELCH CIRCUIT

The squelch circuit is composed of a noise amplifier, band-pass filter, and noise detector within **Q1046** (**BA4116FV**) and level shifter **Q1032** (**M62364FP**-CH2). When a carrier isn't received, the noise at the output of the detector stage in **Q1046** (**BA4116FV**) is amplified by the level shifter **Q1032** (**M62364FP**-CH2). The amplified noise is applied to the band-pass filter section in **Q1046** (**BA4116FV**), then detected to DC voltage by the detector stage in **Q1046** (**BA4116FV**). The DC voltage is inputted to 98-pin (NOISE port) of the CPU **Q1035** (**R5F2L3ACANFP**).

When a carrier is received, the DC voltage at the 98-pin of the CPU **Q1035** (**R5F2L3ACANFP**) becomes "low" level, because the noise is compressed.

When the detected voltage at the 98-pin of the CPU **Q1035** (**R5F2L3ACANFP**) is "high" level, the 17-pin (AF MUTE) of the CPU **Q1035** (**R5F2L3ACANFP**) becomes "low" level. As a result, turns the AF mute switch section of **Q1049** (**CMX264**) to "OFF" to disable the audio output.

3. Transmitter System

3-1. MIC AMPLIFIER

The AF signal from internal microphone MC1001 or external microphone connected to J1002 (**MIC/SP** jack) is amplified with microphone amplifier **Q1017-3** (**NJM12902V**).

This signal is applied to the high pass filter **Q1054-1** (**LM2904PW**) and buffer amplifier **Q1020-4** (**LM2902PW**). Afterwards, the AF signal is adjusted by the D/A converter **Q1032** (**M62364FP**-CH1). The adjusted AF signal is applied to the splatter filter **Q1017-4** (**NJM12902V**), Low-pass filter **Q1017-1/-2** (**NJM12902V**), and buffer amplifier **Q1020-2** (**LM2902PW**), the mic audio is applied to the D/A converter **Q1032** (**M62364FP**-CH4) which adjusts the audio for Max deviation for normal or narrow band operation. The mic audio is then applied to varactor diode **D1031** (**HVC383B**) that modulates the VCO transmit signal.

3-2. DRIVE AND FINAL AMPLIFIER

The modulated signal from the TX VCO **Q1042** (**2SC4227**) is buffered by **Q1038** (**2SC5005**). Then the signal is buffered by **Q1031** (**2SC5227**) for the final amplifier driver **Q1026** (**RQA0004PXDQS**). The low-level transmit signal is then applied to **Q1019** (**RQA0011DNS**) for final amplification up to 5watts output power.

The transmit signal then passes through the antenna switch **D1003** (**RLS135**), low pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-3. AUTOMATIC TRANSMIT POWER CONTROL

The current detector **Q1012-2** (**LM2904RW**) detects the current of **Q1026** (**RQA0004PXDQS**) and **Q1019** (**RQA0011DNS**), and converts the current difference to the voltage difference.

The output from the current detector **Q1012-2** (**LM2904RW**) is compared with the reference voltage and amplified by the power control amplifier **Q1012-1** (**LM2904RW**).

The output from **Q1012-1** (**LM2904RW**) controls the gate bias of the final amplifier **Q1019** (**RQA0011DNS**) and the driver **Q1026** (**RQA0004PXDQS**).

The reference voltage changes into two values (Transmit Power "High" and "Low") controlled by **Q1032** (**M62364FP**-CH8).

4. PLL Frequency Synthesizer

The frequency synthesizer consists of PLL IC, VCO, TCXO (X1003), and buffer amplifier.

The output frequency from TCXO is 16.8 MHz and the tolerance is ±2.5 ppm (in the temperature range –30 to +60 degrees).

4-1. VCO

While the radio is receiving, the RX VCO **Q1040** (**2SK508**) generates a programmed frequency between 223.675 and 230.925 MHz (Marine Band) or 201.650 and 241.650 MHz (LMR Band) as 1st local signal.

While the radio is transmitting, the TX VCO **Q1042** (**2SC4227**) generates a frequency between 156.025 and 162.000 MHz (Marine band) or 134.000 and 174.000 MHz (LMR Band).

During receive, the signal from VCO is amplified by buffer amplifier **Q1038** (**2SC5005**). The output signal **Q1038** (**2SC5005**) applied to (a) pin-8 of the PLL IC **Q1048** (**MB15E03SL**) to keep the radio on frequency (b) the 1st mixer **Q1036** (**3SK293**) as the 1st local signal through **D1029** (**DAN235E**).

During transmission, the TX signal from the VCO is applied to buffer amplifier **Q1031** (**2SC5227**) through **D1029** (**DAN235E**).

4-2. PLL

The PLL IC **Q1048** (**MB15E03SL**) consists of reference divider, main divider, phase detector, charge pumps and pulse swallow operation. The reference frequency from TCXO is inputted to 1-pin of PLL IC **Q1048** (**MB15E03SL**) and is divided by reference divider.

The other hand, inputted feed back signal to pin 8 of PLL IC **Q1048** (**MB15E03SL**) from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated.

The phase difference pulse and the pulse from through the charge pumps and LPF is converted into DC voltage to control the VCO.

The oscillation frequency of VCO is locked by the control of this DC voltage.

The PLL serial data from CPU **Q1035** (**R5F2L3ACANFP**) is sent with three lines of CLK (81-pin), DATA (82-pin) and P STB (83-pin).

The lock condition of PLL is output from the UL (2-pin) terminal and UL becomes "H" at the time of the lock condition and becomes "L" at the time of the unlocked condition. The CPU **Q1035** (**R5F2L3ACANFP**) always watches for an unlocked condition. If an unlock condition is seen by the CPU **Q1035** (**R5F2L3ACANFP**) it prevents the radio from transmitting and receiving.