HX280S Circuit Description

1. Receive Signal Path

Incoming RF from the antenna jack is delivered to the RF Unit and passes through a low-pass filter consisting of coils L1001, L1002 and L1004, capacitors C1005, C1014, C1015 and C1019, and antenna switching diode D1004.

Signals within the frequency range of the transceiver enter a band-pass filter consisting of coils L1013 and L1016, capacitors C1060, C1064 and C1067, then amplified by Q1015 and enter a Varactor-tuned band-pass filter consisting of coils L1021 and L1022, capacitors C1106, C1107, C1108, C1120, C1221, and diodes D1025 and D1026, before first mixing by Q1022.

Buffered output from the VCO is amplified by Q1007 to provide a pure first local signal between 134.35 and 141.575 MHz for injection to the first mixer Q1022.

The 21.7 MHz first mixer product then passes through monolithic crystal filter XF1001/XF1002 to strip away all but the desired signal, which is then amplified by Q1024.

The amplified first IF signal is applied to FM IF subsystem IC Q1026, which contains the second mixer, second local oscillator, limited amplifier, noise amplifier, and RSSI amplifier.

A second local signal is produced from the PLL reference/second local oscillator of X1001 (21.25 MHz). The 21.25 MHz reference signal is delivered to mixer section of Q1026 which produce the 450 kHz second IF mixed with the first IF signal.

The second IF then passes through the ceramic filter CF1001 to strip away unwanted mixer products, and is then applied to the limited amplifier in Q1026, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001.

2. Audio Amplifier

The demodulated audio signal from the Q1026 passes through a band-pass filter and High-pass filter, then applied to the de-emphasis of Q1005. Then passes through the audio mute switch Q1034, the audio volume VR1004 and the audio power amplifier Q1032, providing up to 700 mW of audio power to the 16 Ω loudspeaker.

3. Squelch Control

The squelch circuitry consists of a noise amplifier and band-pass filter and noise detector within Q1026.

When no carrier received, noise at the output of the detector stage in Q1026 is amplified and band-pass filtered by the noise amplifier section of Q1026 and the network between pins 7 and 8, and then rectified by detection circuit in Q1026.

The resulting DC squelch control voltage is passed to pin 64 of the microprocessor Q1025. If no carrier is received, this signal causes pin 38 of Q1025 to go low and pin 67 to go high. Pin 67 signals of Q1025 to disable the supply voltage to the audio amplifier Q1032.

Thus, the microprocessor blocks output from the audio amplifier, and silences the receiver, while no signal is being received (and during transmission, as well).

4. Transmit Signal Path

The speech input from the microphone MC1001 passes through the audio amplifier Q1003, which is adjusted the microphone gain. The speech signal passes through pre-emphasis circuit to Q1003, which contains the IDC, and low-pass filter.

The filtered audio signal is applied to varactor diode D1014, which frequency modulates the VCO Q1008.

The modulated signal from the VCO Q1008 is buffered by Q1007. The low-level transmit signal is then passes through the TX switching diode D1017 to the buffer amplifier Q1016,

driver amplifier Q1013, then amplified transmit signal is applied to the final amplifier Q1009 up to 5.0 watts output power.

The transmit signal then passes through the antenna switch D1005 and is low-pass filtered to suppress harmonic spurious radiation before delivery to the antenna.

4-1 Automatic Transmit Power Control

Current from the final amplifier is sampled by C1011 and C1022, and R1004 and R1008, and is rectified by Q1002. The resulting DC is fed back through Q1004 to the drive amplifier Q1013 and final amplifier Q1009, for control of the power output.

When the microprocessor selects ”High” or “Low” power levels, pin 66 of Q1025 to go low at “High” power selected or pin 66 of Q1025 to go high at “Low” power selected.

5. PLL Frequency Synthesizer

The PLL circuitry on the Main Unit consists of VCO Q1008, VCO buffer Q1007, PLL subsystem IC Q1015, which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and charge pump, and crystal X1001 which frequency stability is ±5 ppm @ -20 to +60 °C.

While receiving, VCO Q1008 oscillates between 134.35 and 141.575 MHz according to the transceiver version and the programmed receiving frequency. The VCO output is buffered by Q1007 then applied to the prescaler section of Q1021. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1021, before being sent to the programmable divider section of Q1021.

The data latch section of Q1021 also receives serial dividing data from the microprocessor Q1025, which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 25.0 kHz derivative of the current VCO frequency.

Meanwhile, the reference divider sections of Q1021 divides the 21.25 MHz crystal reference from the reference oscillator section of Q1021, by 850 to produce the 25.0 kHz loops reference.

The 25.0 kHz signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1021, which produces a pulsed output with pulse duration depending on the phase difference between the input signals.

This pulse train is filtered to DC and returned to the Varactor D1011 and D1012.

Changes in the level of the DC voltage applied to the Varactor, affecting the reference in the tank circuit of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator.

The VCO is thus phase-locked to the crystal reference oscillator. The output of the VCO Q1008 after buffering by Q1007 is applied to the first mixer as described previously.

For transmission, the VCO Q1008 oscillates between 156.025 and 157.425 MHz according to the model version and programmed transmit frequency. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IF s, as in the receiving case). Also, the VCO is modulated by the speech audio applied to D1014, as described previously.

6. Miscellaneous Circuits

Push-To-Talk Transmit Activation

When the PTT switch on the main PCB is closed, pin 72 of Q1025 goes low. This signal disables the receiver by disabling the 5 V supply bus at Q1011 to the front-end, FM IF subsystem IC Q1026.

At the same time, Q1010 activate the transmit 5 V supply line to enable the transmitter.