HX750S Circuit Description

Receiver Signal Flow

VHF Bands Reception

Received VHF bands signals pass through the low-pass filter/high-pass filter circuit, T/R switch circuit composed of diode switch D1040 (**RLS135**), D1041 (**RSL135**), and protector diode D1042 (**1SS400**) before additional filtering by a high-pass filter prior to application to RF amplifier Q1043 (**2SC5006**). The amplified RF signal is passed through the band-pass filter to first mixer Q1035 (**3SK318**). Meanwhile, VHF output from the VCO is applied through diode Band switch D1024 (**DAN235E**) to mixer Q1035 as the first local signal.

First Intermediate Frequency

The 47.25 MHz first intermediate frequency from first mixers is passed through 47.25 MHz monolithic crystal filter (MCF) XF1001 to IF amplifier Q1042 (**2SC4915-0**) for input to pin 16 of Narrow IF IC Q1040 (**NJM2591V**) after amplitude limiting by D1037 (**DA221**).
Meanwhile, a portion of the output of 11.7 MHz crystal X1001 is multiplied fourfold by Q1037 (**2SC4915**) to provide the 46.8 MHz second local signal, applied to the IF IC. Within the IC, this signal is mixed with the 47.25 MHz first intermediate frequency signal to produce the 450 kHz second intermediate frequency.
This second IF is filtered by ceramic filter CF1001 (**LTWC450F**) and amplified by the limiting amplifier within the IF IC before quadrate detection by ceramic discriminator CD1001 (**JTBC450C7**).
Demodulated audio is output from pin 9 of the IF IC Q1040
The demodulated audio signal from the Q1040 is Passed Through a band-pass filter and de-emphasis filter to the volume control IC Q1018 (**BU502FS**) The audio signal passed through the volume control IC to the audio power amplifier Q1001 **(TDA2822D),** providing up to 0.7 W to 16 Ohm loudspeaker.

Squelch Control

Signal components in the neighborhood of 15 kHz contained in the discriminator output pass through an active band-pass filter composed of R1211, R1213, R1214, C1172, C1182 and the operational amplifier between pins 7 and 8 within IF IC Q1040. They are then rectified by D1031 and D1033 (both **DA221**) to obtain a DC voltage corresponding to the level of noise. This voltage is input to pin 16 of CPU Q1017 (**LC87F5BP8A-F56G2**), which compares the input voltage with a previously set threshold. If the DC squelch control voltage is “High” microprocessor Q1017(**LC87F5BP8A-F56G2**)control Pin 22 of volume control IC Q1018(BU2502FS) goes “LOW”, this disabling the AF audio. Also, the microprocessor steps scanning, if active, and allows audio to pass through the volume control IC Q1018 (**BU2502FS**)

Transmitter Signal Flow

Transmit/Receive Switching

Closing PTT switch S1001 pulls the base of Q1003 (**2SA1744R**) low, causing the collector to go high. This signal is input to pin 22 (PTT) of CPU Q1017, allowing the CPU to recognize that the PTT switch has been pushed. When the CPU detects closure of the PTT switch, pin 31 (TX/RX) goes high. This control signal is switches Q1044 (**UMD5N**). At the same time, PLL division data is input to PLL IC Q1019 (**LV2105V**) from the CPU, to disable the receiver power saver. Also, switching Q1041 (**UMD5N**) to disable the receiver circuits. Then causing the red side of BUSY/TX lamp D1016 to light.

Modulation

Voice signal input from either built-in microphone MC1001 (**CZ034DP363)** or external jack J1001 is pre-emphasized by C1014 and R1021, and processed by microphone amplifier Q1007 (**NJM12902AV**), **IDC** (instantaneous deviation control) circuit to prevent over-modulation, and active low-pass filter.

Transmission

Modulating audio passes through deviation setting D/A converter Q1018 to MOD of the VCO. This signal is applied to varactor D1021 (**HSC277**) in the tank circuit of VCO Q1020 (**2SC5231**), which oscillates at the desired transmitting frequency. The modulated VCO signal is buffered by amplifier Q1021 (**2SC5555**) and delivered through T/R diode switch D1024. The modulated low-level transmit signal from the VCO is applied to amplifier Q1030 (**2SC5226-5**). The modulated transmit signal from the VCO is amplified by Q1033 (**RD01MUS1**) and RF power amplifier Q1039 (**RD09MUP2**) up to 6 W. The RF output passes through TX diode switch D1040. RF output is passed by T/R switch and low-pass filter to suppress harmonics and spurious products before output to the antenna at the antenna terminal.

PLL Frequency Synthesizer

PLL IC Q1019 consists of a data shift register, reference frequency divider, phase comparator, charge pump, intermittent operation circuit, and band selector switch. Serial PLL data from the CPU is converted into parallel data by the shift register in the PLL IC and is latched into the comparative frequency divider and reference frequency divider to set a frequency dividing ratio for each. An 11.7 MHz reference signal produced by X1001 is input to REF pin 1 of the PLL IC. The internal reference frequency divider divides the 11.7 MHz reference by 2,340 (or 1,872) to obtain a reference frequency of 5 kHz (or 6.25 kHz), which is applied to the phase comparator. Meanwhile, a sample of the output of VCO Q1021 is input to the PLL IC, where it is frequency-divided by the internal comparative frequency divider to produce a comparative frequency also applied to the phase comparator. The phase comparator compares the phase between the reference frequency and comparative frequency to output a pulse corresponding to the phase difference between them. This pulse is input to the charge pump, and the output from the charge pump passes through a loop filter composed of L1005, R1138, C1106, R1140, C1109, R1143, and

C1112, which convert the pulse into a corresponding smoothed varactor control voltage (VCV). The VCV is applied to varactor D1019 and D1020 (**HVC350B**) in the VCO tank circuit to eliminate phase difference between the reference frequency and comparative frequency, and so locking the VCO oscillation frequency to the reference crystal. The VCO frequency is determined by the frequency-dividing ratio sent from the CPU to the PLL IC. During receiver power save operation, the PLL circuit operates intermittently to reduce current consumption, for which the intermittent operation control circuit reduces the lock-up time.