Circuit Description

Receiver

RF signals pass through a low-pass filter, an antenna switching circuit consisting of **D1004** (**RLS135**) and **D1005** (**RLS135**) and a high-pass filter. Passed signals are amplified with a FET transistor **Q1018** (**3SK294**). Amplified signals are filtered by a band-pass filter to remove unwanted signals. Filtered signals are delivered to the first mixer to generate the first intermediate frequency (IF).

A local signal made by a VCO is input into the first mixer **Q1025** (**3SK318**), then it generates the 1st IF at 47.25MHz. The 1st IF passes through a monolithic crystal filter **XF1001** (47.25MHz) to the IF amplifier **Q1028** (**2SC4915-0**). And the 1st IF is input into the FM IC **Q1031** (**NJM2591V**).

The 2nd local signal (46.8MHz) which is multiplied a crystal oscillator 11.7MHz fourfold with a transistor **Q1029** (**2SC4915-0**) is input into the FM IC.

Inside of the FM IC, the 2nd IF (450kHz) is generated by a mixer mixed with the 1st IF and 2nd local signal, then the 2nd IF is filtered by a ceramic filter **CF1001** (**LTWC450F**) and amplified by a limiting amplifier before quadrate detection by a ceramic discriminator **CD1001** (**JTBM450CX24**) to demodulate.

The demodulated audio signal passes through a de-emphasis network, a high-pass filter **Q1046** (**2SC4617-R**) and a low-pass filter **Q1041** (**2SC4617-R**) to a volume control IC **Q1030** (**BU2502FS**). Controlled audio signal pass through a audio mute IC **Q1034** (**CD4066BPW**) to the audio power amplifier **Q1047** (**TDA2822D**) to provide up to 0.7 W to 16 Ohms loudspeaker.

Squelch control

Some part of the demodulated audio signal is input into an active band-pass filter inside of the FM IC. The output signal from this filter (which means the noise component) is rectified by **D1026** and **D1027** (both **DA221**) after amplified by a transistor **Q1033** (**2SC4617-R**). As a result, obtained DC voltage is read by a CPU **Q1032** (**µPD78F1167GC**).

A CPU compares own squelch set point with this rectified DC. If the DC level is lower than the squelch set point, a CPU controls the mute circuit to mute the audio output.

Modulation

Voice signal from either a built-in microphone **MC1001** (**CZ034DP363**) or an external jack J1001 is pre-emphasized by a pre-emphasis network **C1231** and **R1184**. Pre-emphasized signal is amplified by an op-amp **Q1003** (**LM2904PW**). Amplified signal passes through the IDC (instantaneous

deviation control) circuit and a low-pass filter networks **Q1003** to a volume control IC **Q1030**.
A volume control IC adjusts the modulation to optimum level. The voice signal is delivered to a varactor diode **D1011** (**HVC306B**) in a VCO, then a VCO is modulated directly.

Transmitter

The modulated RF signal from a VCO pass through a diode switch **D1023** (**DAN235E**) to a pre-amplifier **Q1020** (**2SC5226-5**). Amplified RF signal is amplified by a driver-amplifier **Q1015** (**RD01MUS1**) and amplified by a power-amplifier **Q1009** (**RD09MUP2**) up to 6 W.
The RF power output passes through antenna switching diode **D1004** to a low-pass filter network. A low-pass filter suppresses harmonic spurious products before an antenna jack.

Automatic Power Control

Some part of the RF power is sampled by capacitors C1009 and C1020 and rectified by a diode **D1003** (**RB715F**) to obtain the DC voltage level. This DC voltage is compared with the power control voltage from D/A IC **Q1030** by op-amps **Q1004** (**LM2094PW**). As a result, compared output voltage controls RF power devices' bias to get the stable output.

PLL Synthesizer

The 1st Local signal maintains stability from the PLL synthesizer by using the 11.7 MHz reference signal from crystal **X1001**. PLL synthesizer IC **Q1026** (**LV2105V**) consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data, a phase comparator, and applied to the external charge pump which consists of **Q1021** (**2SA1774-R**) and **Q1038** (**2SC4617-R**).
The PLL synthesizer IC divides the 11.7 MHz reference signal by 936 using the reference counter (12.5 kHz comparison frequency).
The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator, and applied to the charge pump.
A voltage proportional to their phase difference is delivered to the low-pass filter circuit, and then fed back to the VCO as a voltage with phase error, controlling and stabilizing the oscillating frequency. This synthesizer also operates as a modulator during transmit.
The VCO consists of **Q1010** (**2SC5231CB**) and varactor diodes **D1008**/**1009** (all **HVC350B**), which oscillates at 47.25 MHz below from the receving frequency. And the VCO oscillates at the fundamental transmit frequency during a transmitting with direct frequency-modulation using

varactor diode **D1011** (**HVC306B**). The VCO output is input into buffer amplifier **Q1008** (**2SC5006**) to obtain stable output.
The DC supply for the VCO is regulated by **Q1017** (**2SC4617-R**).

DSC Encoder/ Decoder

Encoder

CPU **Q1032** encodes the DSC (Digital Selective Calling) signals. This signal is input into the op-amp **Q1003**.
The processes of DSC transmitting are the same as voice modulation.

Decoder

The received DSC signals on channel 70 are filtered by a low-pass filter **Q1037** (**2SC4617-R**). Then this signal is input into the FSK decoder IC **Q1045** (**NJM2211M**) to convert the analog signal into the digital code. CPU **Q1032** watches the digital code and is computing the DSC.

1050 Hz Weather Alert Decoder

Some part of the signal from a low-pass filter output for the DSC is amplified by a transistor **Q1038** (**2SC4617-R**). Amplified signal is input into the Schmitt inverter IC **Q1006** (**SN74LVC3G14DCT**) to obtain the weather alert tone pulse. CPU **Q1032** watches this pulse to count the weather alert tone frequency.

MPU

Operation is controlled by a CPU **Q1032** (**μPD78F1167GC**). This CPU uses a 9.8304 MHz crystal X1002 for the system clock. This CPU includes a reset circuit.

EEPROM

The EEPROM **Q1036** (**BR24L64F-W**) retains TX and RX data for all memory channels, prescaler dividing, IF frequency, local oscillator injection side, and reference oscillator data.