HX500S Circuit Description

Receiver Signal Flow

VHF Bands Reception

Received VHF bands signals pass through the low-pass filter/high-pass filter circuit, T/R switch circuit composed of diode switch D1048 (**RLS135**), D1049 (**1SV307**), and protector diode D1050 (**1SS302**) before additional filtering by a high-pass filter prior to application to RF amplifier Q1065 (**2SC5555**). The amplified RF signal is passed through the band-pass filter to first mixer Q1042 (**3SK318**). Meanwhile, VHF output from the VCO is applied through diode Band switch D1025 (**1SS400**) and T/R switch D1026 (**DAN222**) to mixer Q1042 as the first local signal.

The TUNE-voltage from the D/A converter Q1014 (**M62364PF**) is amplified by DC amplifier Q1037 (**2SA1774-R**) and Q1039 (**UMW1**), and applied to varactors D1033, D1035, D1038, and D1039 (**HVC369B**), D1028, D1029, D1036, D1037, D1040, and D1041 (**1SV325**) in the variable frequency band-pass filters. By changing the electrostatic capacitance of the varactors, optimum filter characteristics are provided for each specific operating frequency.

First Intermediate Frequency

The 47.25 MHz first intermediate frequency from first mixers is passed through 47.25 MHz monolithic crystal filter (MCF) XF1001 to IF amplifier Q1072 (**2SC4915-0**) for input to pin 16 of Narrow IF IC Q1063 (**TA31136FN**) after amplitude limiting by D1045 (**DA221**).

Meanwhile, a portion of the output of 11.7 MHz crystal X1001 is multiplied fourfold by Q1070 (**2SC4617-R**) and Q1077 (**2SC4915-0**) to provide the 46.8 MHz second local signal, applied to the IF IC. Within the IC, this signal is mixed with the 47.25 MHz first intermediate frequency signal to produce the 450 kHz second intermediate frequency.

This second IF is filtered by ceramic filter CF1001 (**LTWC450F**) and amplified by the limiting amplifier within the IF IC before quadrate detection by ceramic discriminator CD1001 (**JTBC450C7**).

Demodulated audio is output from pin 9 of the IF IC.

The demodulated audio signal from the Q1063 passes through a band-pass filter and squelch gate Q1029 (**NJM12902V**) before de-emphasis filter.

The resulting audio is amplified by AF amplifier Q1009 (**TDA7233D**) and output through MIC/EAR jack J1001 to internal speaker or an external earphone.

Squelch Control

Signal components in the neighborhood of 15 kHz contained in the discriminator output pass through an active band-pass filter composed of R1226, R1230, R1239, C1176, C1182 and the operational amplifier between pins 7 and 8 within IF IC Q1063. They are then rectified by D1032 and D1034 (**DA221**) to obtain a DC voltage corresponding to the level of noise. This

voltage is input to pin 16 of CPU Q1026 (**LC87F5BP8A-F56G2**), which compares the input voltage with a previously set threshold. When the input voltage drops below the threshold, normally due to the presence of a carrier, turning on squelch gate Q1029 and allowing any demodulated audio to pass. At the same time, Q1002 and/or Q1004 and/or Q1006 goes on, causing the BUSY/TX lamp D1009 (**SDDF01000A**) to light.

Transmitter Signal Flow

Transmit/Receive Switching

Closing PTT switch S1002 pulls the base of Q1008 (**DTA144EE**) low, causing the collector to go high. This signal is input to pin 22 (PTT) of CPU Q1026, allowing the CPU to recognize that the PTT switch has been pushed. When the CPU detects closure of the PTT switch, pin 31 (TX/RX) goes high. This control signal is switches Q1083 (**UMD5N**). At the same time, PLL division data is input to PLL IC Q1027 (**MB15A01PFV1**) from the CPU, to disable the receiver power saver. Also, switching Q1076 (**UMB3N**) to disable the receiver circuits. Then causing the red side of BUSY/TX lamp D1009 to light.

Modulation

Voice signal input from either built-in microphone MC1001 (**SKB-2244S**) or external jack J1001 is pre-emphasized by C1020 and R1034, and processed by microphone amplifier Q1010 (**NJM12902AV**), **IDC** (instantaneous deviation control) circuit to prevent over-modulation, and active low-pass filter.

Transmission

Modulating audio passes through deviation setting D/A converter Q1014 to MOD of the VCO. This signal is applied to varactor D1016 (**HSC277**) in the tank circuit of VCO Q1034 (**2SC5555**), which oscillates at the desired transmitting frequency. The modulated VCO signal is buffered by amplifier Q1040 (**2SC5555**) and delivered through T/R diode switch D1026. The modulated low-level transmit signal from the VCO is applied to amplifier Q1048 (**2SC5226-5**). The modulated transmit signal from the VCO is amplified by Q1056 (**2SK3475**) and RF power amplifier Q1066 (**2SK3476**) up to 5 W. The RF output passes through TX diode switch D1048. RF output is passed by T/R switch and low-pass filter to suppress harmonics and spurious products before output to the antenna at the antenna terminal.

PLL Frequency Synthesizer

PLL IC Q1027 consists of a data shift register, reference frequency divider, phase comparator, charge pump, intermittent operation circuit, and band selector switch. Serial PLL data from the CPU is converted into parallel data by the shift register in the PLL IC and is latched into the comparative frequency divider and reference frequency divider to set a frequency dividing ratio for each. An 11.7 MHz reference signal produced by X1001 is input to REF pin 1 of the PLL IC. The internal reference frequency divider divides the 11.7 MHz reference by 2,340 (or 1,872) to obtain a reference frequency of 5 kHz (or 6.25 kHz), which is applied to the phase comparator. Meanwhile, a sample of the

output of VCO Q1040 is input to the PLL IC, where it is frequency-divided by the internal comparative frequency divider to produce a comparative frequency also applied to the phase comparator. The phase comparator compares the phase between the reference frequency and comparative frequency to output a pulse corresponding to the phase difference between them. This pulse is input to the charge pump, and the output from the charge pump passes through a loop filter composed of L1005, R1142, C1098, R1143, C1104, R1151, and C1110, which convert the pulse into a corresponding smoothed varactor control voltage (VCV). The VCV is applied to varactor D1015 (**1SV325**) in the VCO tank circuit to eliminate phase difference between the reference frequency and comparative frequency, and so locking the VCO oscillation frequency to the reference crystal. The VCO frequency is determined by the frequency-dividing ratio sent from the CPU to the PLL IC. During **receiver power save** operation, the PLL circuit operates intermittently to reduce current consumption, for which the intermittent operation control circuit reduces the lock-up time.