CPV350 Circuit Description

Reception and transmission are switched by 16-bit MPU IC **Q3004** on the CNTL Unit. The receiver uses double-conversion superheterodyne circuitry, with a 30.4 MHz 1st IF and 450 kHz 2nd IF. The 1st local is produced by a PLL synthesizer, yielding the 30.4 MHz 1st IF. The 2nd local uses a 29.950 MHz crystal oscillator, yielding the 450 kHz 2nd IF. The 2nd mixer and other circuits use a custom IC to convert and amplify the 2nd IF and detect FM to obtain demodulated signals. During transmit, the PLL synthesizer oscillates at the desired frequency directly, for amplification to obtain RF power output. During transmit, voice modulation is applied to this synthesizer. Transceiver functions, such as TX/RX control, PLL synthesizer settings, and channel programming, are controlled using the MPU.

Receiver

Incoming RF signals from the antenna connector are delivered to the RF Unit, and pass through a low-pass filter (LPF) consisting of coils L1009 & L1010 and capacitors C1010, C1017, & C1038, and antenna switching diode **D1005** for delivery to the receiver front end.

Signals within the frequency range of the transceiver are then passed through a bandpass filter consisting of coils L1001 & L1002 and capacitors C1005, C1007, C1024, C1030, & C1044, before RF amplification by **Q1018**.

The amplified RF is then passed through a bandpass filter again consisting of coils L1003, L1004, & L1005 and capacitors C1126, C1129, C1134, C1143, C1151, C1158, & C1165, the pure in-band input signal is delivered to the main 1st mixer which is composed of balun transformers (T1001, T1002, and T1003) and quadrate FETs **Q1032**, **Q1033**, **Q1036**, and **Q1037**.

Buffered output from the MAIN VCO is amplified by **Q1021** and **Q1016** and low-pass filtered by coils L1034 and L1036 and capacitors C1179, C1180, C1182, C1183 and C1187, to provide a pure 1st local signal between 125.65 and 131.625 MHz for delivery to the main 1st mixer.

The 30.4 MHz 1st mixer product is amplified by **Q1042**, then passes through monolithic crystal filters XF1003 and XF1004 (±6.5 kHz BW), and is amplified by **Q1047** and **Q1051**.

After that, it delivered to the input of the FM IF subsystem IC **Q1049**. This IC contains the 2nd mixer, 2nd local oscillator, limiter amplifier, FM detector, noise amplifier, and squelch gates.

The 2nd local in the FM IF subsystem IC is produced from crystal **X1001** (29.950 MHz), and the 1st IF is converted to 450 kHz by the 2nd mixer and stripped of unwanted components by ceramic filter **CF1001**.

After passing through a limiter amplifier, the signal is demodulated by the FM detector. Demodulated receive audio from the FM IF subsystem IC is delivered to the AF Unit, then amplified by **Q2009** and **Q2010**. The amplified signal is passed through the AF selector switch **Q2012** to the amplifier **Q2018**. The amplified signal is brought to the RAM UNIT through the AF mute switch **Q2013**.

The AF signal which was selected by the AF switch **Q7013** is delivered to the electronic

volume control IC **Q7022**. The adjusted audio signal by **Q7022** is delivered to the AF power amplifier **Q7008** to obtain the drive level for the speaker. The amplified audio signal is delivered to the 16 Ohms internal loudspeaker or a external speaker terminal in the accessory cable.

PLL Synthesizer

The 1st Local signal maintains stability from the PLL synthesizer by using a 29.950 MHz reference signal from crystal **X1001**. PLL synthesizer IC **Q1034** consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data, a phase comparator, and a charge pump.

The PLL synthesizer IC divides the 29.950 MHz reference signal by 2396 using the reference counter (12.5 kHz comparison frequency). The reference oscillator feeds to the PLL synthesizer IC **Q1034** for the 2nd local signal.

The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator, and applied to the charge pump.

A voltage proportional to their phase difference is delivered to the low-pass filter circuit, then fed back to the VCO as a voltage with phase error, controlling and stabilizing the oscillating frequency. This synthesizer also operates as a modulator during transmit.

The MAIN VCO is consisted of **Q1023** and varactor diodes **D1008**, **D1009**, **D1010**, and **D1011**, which oscillates at 30.4 MHz below from the receiving frequency. The MAIN VCO output passes through buffer amplifier **Q1021** to obtain stable output, then applied to the main 1st mixer. The DC supply for the MAIN VCO is regulated by **Q1013**.

The TX & SUB VCO is consisted of **Q1031** and varactor diodes **D1014**, **D1015**, **D1016**, and **D1017**, which oscillates at 134.225 MHz for the CH70 receiving and the fundamental transmit frequency during a transmit, with direct frequency-modulation using varactor diode **D1013**. The TX & SUB VCO output passes through buffer amplifier **Q1028** to obtain stable output. The TX & SUB VCO output is passed through another buffer amplifier **Q1024** and diode switch **D1007** to the sub 1st mixer which is composed of balun transformers (T1004, T1005, and T1006) and quadrate FETs **Q1026**, **Q1027**, **Q1029**, and **Q1030** during receive, and to drive amplifiers **Q1020** for transmit. The DC supply for the TX & SUB VCO is regulated by **Q1022**.

Transmitter

The voice audio from the microphone is delivered to the RAM Unit and the voice audio is amplified by **Q7005** for a pre-emphasis and passes through the AF switch **Q7013** to the AF Unit. After that, this audio is brought to the limiter amplifiler (IDC: instantaneous deviation control) and low-pass filter network on the AF Unit.The audio is adjusted for optimum deviation level and delivered to the next stage.

Voice or DSC (Digital Selective Calling) encode signal inputs from the low-pass filter network **Q2020** is applied to the TX & SUB VCO **Q1031** and varactor diode **D1014**, **D1015**, **D1016**, & **D1017**, which oscillates the fundamental transmit frequency with direct frequency-modulation using varactor diode **D1013**. The modulated signal is amplified by the buffer amplifier **Q1028** and **Q1024**, then passed through the diode switch **D1007** to drive amplifiers **Q1020** and RF power amplifier module **Q1001**.

The RF energy then passes through antenna switch **D1006** and low-pass filter (LPF) consisting of coils L1009 and L1010 and capacitors C1010, C1017, & C1038, and finally to the antenna connector.

RF output power from the RF power amplifier module **Q1001** is sampled by C1023 and C1032 and is rectified by **D1004**. The resulting DC is fed through Automatic Power Controllers **Q1002** to RF power amplifier module **Q1001**, thus providing positive control of the power output.

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of coils and capacitors, resulting in more than 70 dB of harmonic suppression prior to delivery of the RF energy to the antenna.

DSC Encoder/ Decoder

Encoder

The DSC (Digital Selective Calling) encode signal which D/A converted in the 16-bit MPU IC **Q3004** on the CNTL Unit is fed through the low-pass filter **Q2020** on the AF Unit to the TX & SUB VCO **Q1031** on the RF Unit.

Decoder

Incoming the receiving DSC code on the CH70 from the antenna connector are passed through a SUB-RX RF amplifier **Q1015** to the bandpass filter consisting of coils L1006, L1007, & L1008 and capacitors C1122, C1127, C1132, C1139, C1146, C1154, and C1159, then the filtered signal deliver to the sub 1st mixer which is composed of balun transformers (T1004, T1005, and T1006) and quadrate FETs **Q1026**, **Q1027**, **Q1029**, and **Q1030**.

Buffered output from the TX & SUB VCO **Q1031** is amplified by **Q1028** and **Q1024** and bandpass filtered by coils L1028 & L1029 and capacitors C1145, C1148, C1153, C1155, & C1160, to provide a pure 1st local signal (134.225 MHz) for delivery to the sub 1st mixer.

The 22.3 MHz 1st mixer product then passes through monolithic crystal filters XF1001 and XF1002 (±6.5 kHz BW) and buffer amplifier **Q1043** and **Q1044**, then deliver to the SUB-RX FM IF subsystem IC **Q1050**. This IC contains the 2nd mixer, 2nd local oscillator, limiter amplifier, FM detector, noise amplifier, and squelch gates.

The 2nd local is produced by crystal X1002 (21.850 MHz) then deliver to the 2nd mixer in the SUB-RX FM IF subsystem IC **Q1050**. The 1st IF is converted to 450 kHz by the 2nd mixer and stripped of unwanted components by ceramic filter CF1002.

Filtered signal from the ceramic filter CF1002 is applied to the limiter amplifier in the SUB-RX FM IF subsystem IC **Q1050**, and then demodulate by the FM detector in the SUB-RX FM IF subsystem IC **Q1050**. Demodulated signal from the SUB-RX FM IF subsystem IC **Q1050** is passes through the low-pass filter **Q1046** to the DSC Decoder IC **Q1048** which the receiving DCS code is decoded. The decoded DCS signal delivered to the 16-bit MPU IC **Q3004**.

The SUB-RX 1st Local signal maintains stability from the PLL synthesizer by using a

29.950 MHz reference signal from crystal **X1001**. PLL synthesizer IC **Q1034** consists of a prescaler, reference counter, swallow counter, programmable counter, a serial data input port to set these counters based on the external data, a phase comparator, and a charge pump.

The PLL synthesizer IC divides the 29.950 MHz reference signal by 2396 using the reference counter (12.5 kHz comparison frequency). The reference oscillator feeds to the PLL synthesizer IC **Q1034** for the 2nd local signal.

The VCO output is divided by the prescaler, swallow counter and programmable counter. These two signals are compared by the phase comparator, and applied to the charge pump.

A voltage proportional to their phase difference is delivered to the low-pass filter circuit, then fed back to the VCO as a voltage with phase error, controlling and stabilizing the oscillating frequency.

The TX & SUB VCO is consisted of **Q1031** and varactor diode **D1014**, **D1015**, **D1016**, and **D1017**, which oscillates at 134.225 MHz. The TX & SUB VCO output passes through buffer amplifier **Q1028** to obtain stable output.

1050 Hz Weather Alert Decoder

1050 Hz Weather Alert signal from the FM IF subsystem IC **Q1049** on the RF Unit is demodulated by **Q2007** on the AF Unit, then is applied to 16-bit MPU IC **Q3004** on the CNTL Unit.

PA (Public Address) Circuit

A voice audio from the microphone is delivered to the RAM Unit. A voice audio is amplified by **Q7005** and passes through the AF switch **Q7013**. After that, the voice audio passes the AF/MIC select switch **Q2013** to the buffer amplifier **Q2023**. The audio then passes through the LB/HAIL select switch **Q2011** and MUTE switch **Q2012** to the buffer amplifier **Q2018**. The amplified audio is passed through the LB/HAIL select switch **Q2011** and buffer amplifier **Q2023** to the electronic volume control IC **Q2017** for volume control. The adjusted audio is delivered to the audio power amplifier **Q2014** which is amplified the voice audio up to 30 watts, and then passes through the relay switch RL2001 to the external PA speaker.

LB (Listen Back) Circuit

The listen back audio from the PA speaker is delivered to the AF Unit. The audio is passed through the relay switch RL2001 and buffer amplifier **Q2023** to the LB/HAIL selector switch **Q2011**, then passes through the MUTE switch **Q2012** to the buffer amplifier **Q2018**. The audio is supplied to the AF power amplifier **Q7008** through the same circuits as the receiver audio network (**Q2013**, **Q7013** and **Q7022**) to let out a sound from the speaker.

A portion of the audio from the **Q2012** is passed through the buffer amplifier **Q2018** and AF/MIC select switch **Q2013** to the RAM microphones, if connected.

Fog Horn Circuit

A 400 Hz square wave for foghorn is generated by the microprocessor **Q3004** on the CNTL Unit, then deliver to the AF Unit. A 400 Hz square wave passes through the buffer amplifier **Q2023** to the electronic volume control IC **Q2017** for volume control. The adjusted audio is delivered to the audio power amplifier **Q2014** which is amplified the voice audio up to 30 watts, and then passes through the relay switch RL2001 to the external PA speaker.

MPU

Operation is controlled by 16-bit MPU IC **Q3004** on the CNTL Unit. The system clock uses a 14.74560 MHz crystal X3001 for a time base. IC **Q3003** resets the MPU when the power is on, and monitors the voltage of the regulated 5V power supply line.

EEPROM

The EE-PROM **Q3006** on the CNTL Unit retains TX and RX data for all memory channels, prescaler dividing, IF frequency, local oscillator injection side, and reference oscillator data.