VX-450 (UHF) Series Circuit Description

1. Circuit Configuration by Frequency

The receiver is a Double-conversion Super-heterodyne with a first intermediate frequency (IF) of 67.65MHz and a second IF of 450kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 67.65MHz.
This is then mixed with the 67.2MHz second local oscillator output to produce the 450kHz second IF. This is detected to give the demodulated signal.
The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, antenna switching diode, high pass filter and removed undesired frequencies by varactor diode D1006,D1007 and D109,D1010 (tuned band-pass filer).
The passed signal is amplified in Q1007 (BF1212WR) and moreover cuts an image frequency with the tuned band pass filter and comes into the 1st mixer.

2-2. First Mixer

The 1st mixer consists of the Q1015 (3SK293). Buffered output from the VCO is amplified by Q1014 (2SC5005) to provide a pure first local signal between 332.35 and 402.35 MHz for injection to the first mixer.
The IF signal then passes through monolithic crystal filters XF1001 (±7.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by Q1025 (2SC5526).
The amplified first IF signal is applied to FM IF subsystem IC Q1033 (NJM2591V) which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and RSSI amplifier.
The signal from reference oscillator X1001 becomes 4 times of frequencies in Q1033, it is mixed with the IF signal and becomes 450 KHz.
The second IF then passes through the ceramic filter CF1001 or CF1002 to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1033, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001 (ECDA450C24).

2-4. Audio amplifier

Detected signal from Q1033 (NJM2591V) is inputted to Audio Processor IC Q1013 .
The signal which appeared from Q1001 is in high pass filter Q1041 (NJM12902V).
The signal which passed Q1041 goes to AF volume (VR1001). And then the signal goes to audio amplifier Q1048 (TDA2822L-50B).The output signal from J1006 is in audio speaker.

2-5. Squelch Circuit

There are 16 levels of squelch setting from 0 to 15. The level 0 means open the squelch. The level 1 means the threshold setting level and level 14 means tight squelch. From 2 to 13 is established in the middle of threshold and tight.
The bigger figure is nearer the tight setting. The level 15 becomes setting of carrier squelch.

2-5-1. Noise Squelch

Noise squelch circuit is composed of the band path filter and noise detector of Q1033.
When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1033 is amplified in Q1037 through the band path filter, is detected to DC voltage with D1031 and is inputted to 15 pin (the A/D port) of the Q1035 (CPU).
When a carrier is received, the DC voltage becomes low because the noise is compressed.
When the detected voltage to CPU is high, the CPU stops AF output with Q1049 "OFF" by making the 90 pin (CPU) "L" level.
When the detection voltage is low, the CPU makes Q1049 ON with making 90 pin "H" and the AF signal is output.

2-5-2. Carrier Squelch

The CPU (14pin: A/D port) detect RSSI voltage output from Q1033 12 pin, and controls AF output.
The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage.
The process of the AF signal control is same as Noise Squelch
The shipping data is adjusted -1dBu (EMF) higher than squelch tight sensitivity.

3. Transmitter System

3-1. Mic Amplifier

The AF signal from internal microphone MC2001 or external microphone J1004 in to Audio processor IC Q1013. (selected 34pin or 35pin) Q1013 is which contains the microphone amplifier, compandor, Pre-emphasis, limiter and splatter filter, the processed signal to made FM modulation to transmit carrier by the modulator D1014 (HVC383B) of VCO.
Q1013 is built-in DTMF Receiver, and Inversion Type Encryption.

3-2. Drive and Final amplifier

The modulated signal from the VCO Q1023 (2SC4227) is buffered by Q1017 (2SC5005) . Then the signal is buffered by Q1010 (2SC3336) for the final amplifier driver Q1015 (RQA0004PXDQS). The low-level transmit signal is then applied to Q1006 (RQA0011DNS) for final amplification up to 5watts output power.
The transmit signal then passes through the antenna switch D1005 (HVU131) and is low pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-4. Automatic Transmit Power Control

The current detector Q1040-1(NJM12904V) detects the current of Q1006 and Q1008, and converts the current difference to the voltage difference.
The output from the current detector Q1040-1 is compared with the reference voltage and amplified by the power control amplifier Q1040-2.
The output from Q1040-2 controls the gate bias of the final amplifiers Q1006 and the final amplifier driver Q1008.
The reference voltage changes into four values (Transmit Power High and Low) controlled by Q1040 (NJM12904V).

3-5. PLL Frequency Synthesizer

The frequency synthesizer consists of PLL IC, Q1036 (AK1541), VCO, TCXO (X1001).
The output frequency from TCXO is 16.8MHz and the tolerance is +/- 2.5 ppm (in the temperature range -30 to +60 degrees).

3-5-1. VCO

While the radio is receiving, the RX oscillator Q1019 (2SK508) in VCO generates a programmed frequency between 332.35 and 402.35MHz as 1st local signal.
While the radio is transmitting, the TX oscillator Q1023 (2SC4227) in VCO generates a frequency between 400 and 470MHz.
The output from oscillator is amplified by buffer amplifier Q1017 (2SC5005) and becomes output of VCO. The output from VCO is divided, one is amplified by Q1022 and feed back to the PLL IC 17 pin. The other is amplified in Q1014 and in case of the reception, it is put into the mixer as the 1st local signal through D1011, in transmission, it is buffered Q1010, and more amplified in Q1008 and it is put into the final amplifier Q1008.

3-5-2. VCO Tuning Voltage

Tuning voltage of VCO is expanding the lock range of VCO by controlling the cathode of varactor diode at the voltage and the control voltage from PLL IC.

3-5-3. PLL

The PLL IC consists of reference divider, main divider, phase detector, charge pumps and pulse swallow operation. The reference frequency from TCXO is inputted to 10 pin of PLL IC and is divided by reference divider.
The other hand, inputted feed back signal to 17 pin of PLL IC from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated.
The phase difference pulse and the pulse from through the charge pumps and LPF. It becomes the DC voltage to control the VCO.
The oscillation frequency of VCO is locked by the control of this DC voltage.
The PLL serial data from CPU is sent with three lines of SDO (40pin), SCK (36pin) and PSTB (30pin).
The lock condition of PLL is output from the UL (18Pin) terminal and UL becomes "H" at the time of the lock condition and becomes "L" at the time of the unlocked condition. The CPU always watches over the UL condition, and when it becomes "L" unlocked condition, the CPU prohibits transmitting and receiving.