VX-4500-G6-45 / VX-4600-G6-45 Circuit Description

1. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 67.65 MHz and a second IF of 450 kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 67.65MHz. This is then mixed with the 67.2MHz second local oscillator output to produce the 450 kHz second IF. This is detected to give the demodulated signal. the transmit signal frequencies generated by the PLL VCO and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, and removed undesired frequencies by varactor diode. tuned band-pass filer consisting of diodes D1013 and D1015, and Coils L1015 and L1018, capacitors C1017, C1116, C1118, C1130 and C1117,C1135,C1137 and C1139,1151,1156.The passed signal is amplified in Q1021 and moreover cuts animage frequency with the tuned band-path filter consisting of Coils L1025, L1028 and capacitors C1173C,1181,C1182,C1183 and C1188,C1197, C1198, C1205 and C1212. and comes into the 1st mixer.

2-2. First Mixer

The 1st mixer consists of the Q1040. Buffered output from the VCO is amplified by Q1026 to provide a pure first local signal between 332.35 and 402.35 MHz for injection to the first mixer. The output IF signal is enters from the mixer to the crystal filter. The IF signal then pass through monolithic crystal filters XF1001 (±5.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by Q1049. The amplified first IF signal is applied to FM IF subsystem IC Q1054 which contains the second mixer second local oscillator limiter amplifier noise amplifier and S-meter amplifier. The signal from reference oscillator X1002 becomes 4 times of frequencies in Q1054, it is mixed with the IF signal and becomes 450 kHz. The second IF then passes through the ceramic filter CF1002 (for wide channels) CF1001, CF1003 (for narrow channels) to strip away unwanted mixer products which removes amplitude variations in the 450 kHz IF before detection of the speech by the ceramic discriminator CD1001.

2-4. Audio amplifier

Detected signal from Q1054 is inputted to Q1010 pin28 and is output by Q1010 pin17 through the band path filter. When the optional unit is installed the Q1010 is made "OFF" and the AF signal from Q1010 pin21 goes the and returns to Q1010 pin 20 from the optional unit. When the optional unit is not installed, Q1010 is made "ON" the AF signal goes through Q1010 pin20/21. The signal is stored in the AF volume via AF mute and de-emphasis inside Q1010 . The AF volume is controlling Q1010 by the CPU. After that, it enters AF power amplifier Q1003 after passing AF volume the output of Q1003 drives a speaker (it chooses the external SP or internal SP in J1001).

2-5. Squelch Circuit

There are 16 levels of squelch setting from 0 to 15. The level 0 means open the squelch. The

level 1 means the threshold setting Level and level 15 means tight squelch. From 1 to 14 is established in the middle of threshold and tight. The bigger figure is nearer the tight setting. The level 16 becomes setting of carrier squelch.

2-5-1. Noise Squelch
Noise squelch circuit is composed of the band path filter of Q1054 noise amplifier Q1060 and noise detector D1048, D1052. When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1054 is amplified in Q1060 through the band path filter Q1054 is detected to DC voltage with D1048, D1052 and is inputted to 15 pin the A/D port of the Q1041 CPU. When a carrier is received the DC voltage becomes "LOW" because the noise is compressed. When the detected voltage to CPU is "HIGH," the CPU stops AF output with Q1010 "OFF" "L"level. When the detection voltage is low the CPU makes Q1010"ON" with making AF signal is output.

2-5-2. Carrier Squelch
The pin 14 (A/D port) of Q1047 CPU detect RSSI voltage output from pin 12 of Q1054, and controls AF output. The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage. The process of the AF signal control is same as Noise Squelch. The shipping data is adjusted 3dB higher than squelch tight sensitivity.

3. Transmitter System

3-1. MIC Amplifier
The AF signal from microphone jack J2001 (8ch) or J3001 is amplified with microphone amplifier Q1010 is amplified after microphone selection switch Q1010 and passes microphone gain volume Q1010. The control from the CPU it passes output and it passes a pre-emphasis circuit.. When an option unit isn't attached and the AF signal from Q1010 pin 38goes via the option unit, it returns to Q1010 pin39 when an option unit isn't attached Q1010 is inputted to the pre-emphasis circuit. The signal passed limiter and splatter filer of Q1010 is adjusted by maximum deviation adjustment volume. The adjusted low frequency signal ingredient is amplified by Q1047 added modulation terminal of TCXO (X1002) the FM modulation is made by reference oscillator.
The high frequency signal ingredient is amplified, and adjusted the level by volume. Q1010 to make frequency balance between low frequency. After that it is made FM modulation to transmit carrier by the modulator D1026 of VCO.

3-2. Drive and Final amplifier the modulated signal from the VCO Q1017 is buffered by Q1026 and amplified by Q1023 . The low-level transmit signal is then applied to the Power Module Q1013 for final amplification up to 45 watts output power. The transmit signal then passes low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-3. Automatic Transmit Power Control
The output power of Power Module is detected by CM coupler, it is detected by D1005 and D1008 and is input to comparator Q1048. The comparator
compares two different voltages and makes output power stable by controlling the bias voltage of Power Module. There are 3 levels of output power (Hi, Lo3, Lo2 and Lo1) it is switched by the voltage of Q1010 pin44.

3-4. PLL Frequency Synthesizer
The frequency synthesizer consists of PLL IC Q1043 VCO, TCXO (X1002) and buffer amplifier. The output frequency from TCXO is 16.8 MHz and the tolerance is ±2.5 ppm (in the

temperature range -30 to +60 degrees).

3-4-1. VCO

While the radio is receiving, the RX oscillator Q1034 in VCO generates a programmed frequency between 332.35 and 402.35 MHz as 1st local signal. While the radio is transmitting the TX oscillator Q1036 (2SC3356) in VCO generates a frequency between 400 and 470 MHz. The output from oscillator is amplified by buffer amplifier Q1029 and becomes output of VCO. The output from VCO is divided one is amplified by Q1039 and feed back to pin17 of the PLL IC Q1043. it is amplified about the RF signal Q1029 Which was made by VCO. RF changes with the carrier signal of the transceiver and the mixer local signal of the receiver with D1020

3-4-2. VCV CNTL

Tuning voltage (VCV) of VCO is expanding the lock range of VCO by controlling the of varactor diode at the voltage and the control voltage from PLL IC Q1043. as for the control voltage adjustment by the varactor diode. It control the negative to make with Q1025 with the D/A converter inside Q1010 and Q1037, it has to the anode potential of the varacor diode variably.

3-4-3. PLL

The PLL IC Q1043 consists of reference divider, main divider, phase detector, charge pumps and delta-sigma fractional accumulator. The reference frequency from TCXO is inputted to pin 10 of PLL IC Q1043 and is divided by reference divider. This IC is decimal point dividing PLL IC Q1043 and the dividing ratio becomes 1/8 of usual PLL frequency step. Therefore, the output of reference divider is 8 times of frequencies of the channel step. For example when the channel stepping is 5 kHz, the output of reference divider becomes 40 kHz. The other hand, inputted feed back signal to pin 1 of PLL IC Q1043 from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated. The phase difference pulse and the pulse from fractional accumulator pass through the charge pumps and LPF. It becomes the DC voltage (VCV) to control the VCO. The oscillation frequency of VCO is locked by the control of this DC voltage. The PLL serial data from CPU Q1041 is sent with three lines of SDO (pin 20), SCK (pin 22) and PSTB (pin 45). The lock condition of PLL is output from the UL (pin 18) terminal and UL becomes “H” at the time of the lock condition and becomes “L” at the time of the unlocked condition. The CPU Q1041 always watches over the UL condition, and when it becomes “L” unlocked condition, the CPU Q1041 prohibits transmitting and receiving.