VX-350 Serious Circuit Description

1. Circuit Configuration by Frequency

The receiver is a Double-conversion Super-heterodyne with a first intermediate frequency (IF) of 50.85MHz and a second IF of 450kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 50.85MHz.
This is then mixed with the 50.4MHz second local oscillator output to produce the 450kHz second IF. This is detected to give the demodulated signal.
The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, antenna switching diode, high pass filter and removed undesired frequencies by varactor diode (tuned band-pass filer).
The passed signal is amplified in Q1021 and moreover cuts an image frequency with the tuned band pass filter and comes into the 1st mixer.

2-2. First Mixer

The 1st mixer consists of the Q1036. Buffered output from the VCO is amplified by Q1031 to provide a pure first local signal between 399.15 and 461.15MHz for injection to the first mixer.
The IF signal then passes through monolithic crystal filters XF1001(±5.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by Q1048.
The amplified first IF signal is applied to FM IF subsystem IC Q1053 which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.
The signal from reference oscillator X1002 becomes 3 times of frequencies in Q1053, it is mixed with the IF signal and becomes 450KHz.
The second IF then passes through the ceramic filter CF1001 (wide channels), CF1002 (narrow channels) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1053, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001.

2-4. Audio amplifier

Detected signal from Q1053 is inputted to mute switch Q1001-3 and option switch Q1001-2. The signal which appeared from Q1001-2 is in band pass filter Q1066.
In the case an optional unit is installed, the Q1001-2 is made OFF and the AF signal from Q1001-3 goes the optional unit. In the case an optional unit is not installed, Q1001-2 is made ON and the signal goes through Q1001-2.
The signal which passed Q1066 goes to AF volume (VR1001). And then the signal goes to audio amplifier Q1007.
The output signal from Q1007 is in audio speaker.

2-5. Squelch Circuit

There are 16 levels of squelch setting from 0 to 15. The level 0 means open the squelch. The level 1 means the threshold setting level and level 14 means tight squelch. From 2 to 13 is established in the middle of threshold and tight.
The bigger figure is nearer the tight setting. The level 15 becomes setting of carrier squelch.

2-5-1. Noise Squelch

Noise squelch circuit is composed of the band path filter of Q1053, noise amplifier

Q1058, and noise detector D1042, D1043.
When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1053 is amplified in Q1058 through the band path filter Q1053, is detected to DC voltage with D1042, D1043 and is inputted to 48pin (the A/D port) of the Q1044 (CPU).
When a carrier is received, the DC voltage becomes low because the noise is compressed.
When the detected voltage to CPU is high, the CPU stops AF output with Q1001-1 "OFF" by making the 39pin (CPU) "L" level.
When the detection voltage is low, the CPU makes Q1001-1 ON with making 39pin "H" and the AF signal is output.

2-5-2. Carrier Squelch

The CPU (47pin: A/D port) detects RSSI voltage output from Q1053 12 pin, and controls AF output.
The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage.
The process of the AF signal control is same as Noise Squelch
The shipping data is adjusted 3dB higher than squelch tight sensitivity.

3. Transmitter System

3-1. Mic Amplifier

The AF signal from internal microphone MC1001 or external microphone J1002 is amplified with microphone amplifier Q1069-2, after passes microphone gain volume Q1017.
AF signal is passes a pre-emphasis circuit.
Q1001-1 becomes OFF when an option unit is attached and the AF signal from Q1068 goes via the option unit. When an option unit isn't attached, Q1001-1 becomes ON, the signal passes Q1001-1 and is input to the limiter amplifier Q1068-2.
The signal passed splatter filter of Q1068 and adder amplifier Q1065 is adjusted by maximum deviation adjustment volume Q1017.
The AF signal ingredient is amplified Q1065. After that, it is made FM modulation to transmit carrier by the modulator D1023 of VCO.

3-2. Drive and Final amplifier

The modulated signal from the VCO Q1049 is buffered by Q1042 and amplified by Q1031. Then the signal is buffered by Q1026 for the final amplifier driver Q1020. The low-level transmit signal is then applied to Q1013 for final amplification up to 5watts output power.
The transmit signal then passes through the antenna switch D1002 and is low pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-4. Automatic Transmit Power Control

The current detector Q1064-1 detects the current of Q1013 and Q1020, and converts the current difference to the voltage difference.
The output from the current detector Q1064-1 is compared with the reference voltage and amplified by the power control amplifier Q1064-2.
The output from Q1064-2 controls the gate bias of the final amplifiers Q1013 and the final amplifier driver Q1020.
The reference voltage changes into four values (Transmit Power High and Low) controlled by Q1017.

3-5. PLL Frequency Synthesizer

The frequency synthesizer consists of PLL IC, Q1059, VCO, TCXO (X1002) and buffer amplifier.
The output frequency from TCXO is 16.8MHz and the tolerance is +/- 2.5 ppm (in the temperature range -30 to +60 degrees).

3-5-1. VCO

While the radio is receiving, the RX oscillator Q1046 in VCO generates a programmed frequency between 399.15 and 461.15MHz as 1st local signal.
While the radio is transmitting, the TX oscillator Q1049 in VCO generates a frequency between 450 and 512MHz.
The output from oscillator is amplified by buffer amplifier Q1042 and becomes output of VCO. The output from VCO is divided, one is amplified by Q1052 and feed back to the PLL IC 5pin. The other is amplified in Q1031 and in case of the reception, it is put into the mixer as the 1st local signal through D1019, in transmission, it is buffered Q1026, and more amplified in Q1020 through D1019 and it is put into the final amplifier Q1013.

3-5-2. VC0 Tuning Voltage

Tuning voltage of VCO is expanding the lock range of VCO by controlling the cathode of varactor diode at the voltage and the control voltage from PLL IC. The control voltage is added to the anode of varactor diode after converted to by Q1069-1 which is output voltage of D/A converter Q1017-CH5.

3-5-3. PLL

The PLL IC consists of reference divider, main divider, phase detector, charge pumps and fractional accumulator. The reference frequency from TCXO is inputted to 8pin of PLL IC and is divided by reference divider. This IC is decimal point dividing PLL IC and the dividing ratio becomes 1/8 of usual PLL frequency step. Therefore, the output of reference divider is 8 times of frequencies of the channel step. For example, when the channel stepping is 5 kHz, the output of reference divider becomes 40 kHz.
The other hand, inputted feed back signal to 5pin of PLL IC from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated.
The phase difference pulse and the pulse from fractional accumulator pass through the charge pumps and LPF. It becomes the DC voltage to control the VCO.
The oscillation frequency of VCO is locked by the control of this DC voltage.
The PLL serial data from CPU is sent with three lines of SDO (64pin), SCK (1pin) and PSTB (32pin).
The lock condition of PLL is output from the UL (18Pin) terminal and UL becomes "H" at the time of the lock condition and becomes "L" at the time of the unlocked condition. The CPU always watches over the UL condition, and when it becomes "L" unlocked condition, the CPU prohibits transmitting and receiving.