VX-820/870 (UHF) series Circuit Description

1. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 50.85MHz and a second IF of 450kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 50.85MHz.
This is then mixed with the 50.4MHz second local oscillator output to produce the 450kHz second IF. This is detected to give the demodulated signal.
The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, antenna switching diode, high pass filter and removed undesired frequencies by varactor diode (tuned band-pass filer).
The passed signal is amplified in Q1021 and moreover cuts an image frequency with the tuned band pass filter and comes into the 1st mixer.

2-2. First Mixer

The 1st mixer consists of the Q1034, T1001, T1002 and T1003. Buffered output from the VCO is amplified by Q1032 to provide a pure first local signal between 399.15 and 461.15MHz for injection to the first mixer.
The IF signal then passes through monolithic crystal filters XF1001(±5.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by Q1056.
The amplified first IF signal is applied to FM IF subsystem IC Q1065 which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.
The signal from reference oscillator X1003 becomes 3 times of frequencies in Q1065, it is mixed with the IF signal and becomes 450KHz.
The second IF then passes through the ceramic filter CF1001 (wide channels), CF1002 (narrow channels) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1065, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001.

2-4. Audio amplifier

Detected signal from Q1065 is inputted to Q1031 and is output through the band path filter inside Q1031.
In the case an optional unit is installed, the Q1078 is made OFF and the AF signal from Q1031 goes the optional unit. In the case an optional unit is not installed, Q1078 is made ON and the signal goes through Q1078.
The signal then goes through de-emphasis part and expander Q1022. When the function of expander is off, the signal will be bypassed by Q1014.
The output signal of expander (or a signal from de-emphasis) goes through AF mute switch Q1083 and amplified by Q1082.
The signal goes to Q1029, and the output from Q1029 is amplified with AF power amplifier Q2017 after passing AF volume Q1020.
The output of Q2017 drives a speaker (it chooses the external SP or internal SP in external terminal, SELECT)

2-5. Squelch Circuit

There are 13 levels of squelch setting from 0 to 12. The level 0 means open the squelch. The level 1 means the threshold setting level and level 11 means tight squelch.
From 2 to 10 is established in the middle of threshold and tight. The bigger figure is nearer the tight setting.
The level 12 becomes setting of carrier squelch.

2-5-1. Noise Squelch

Noise squelch circuit is composed of the band path filter of Q1065, noise amplifier Q1069,

and noise detector D1049, D1050.

When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1065 is amplified in Q1069 through the band path filter Q1065, is detected to DC voltage with D1049, D1050 and is inputted to 16pin (the A/D port) of the Q1067 (CPU).

When a carrier is received, the DC voltage becomes low because the noise is compressed.

When the detected voltage to CPU is high, the CPU stops AF output with Q1078 "OFF" by making the 59pin (CPU) "L" level.

When the detection voltage is low, the CPU makes Q1078 ON with making 59pin "H" and the AF signal is output.

2-5-2. Carrier Squelch

The CPU (15pin: A/D port) detect RSSI voltage output from Q1065 12 pin, and controls AF output.

The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage.

The process of the AF signal control is same as Noise Squelch

The shipping data is adjusted 3dB higher than squelch tight sensitivity.

3. Transmitter System

3-1. Mic Amplifier

The AF signal from internal microphone J2002 21pin or external microphone J2002 6pin is amplified with microphone amplifier Q2014, after microphone selection switch Q2015, and passes microphone gain volume Q1020.

The AF signal which was controlled in the correct gain passes compandor Q1022. When not using a compandor, with the control from the CPU, it passes in the compandor circuit inside of Q1022 and it is output and it passes a pre-emphasis circuit.

Q1078 becomes OFF when an option unit is attached and the AF signal from Q1022 goes via the option unit. When an option unit isn't attached, Q1078 becomes ON, the signal passes Q1078 and is input to the pre-emphasis amplifier Q1031.

The signal passed limiter and splatter filter of Q1031 is adjusted by maximum deviation adjustment volume Q1020.

The adjusted low frequency signal ingredient is amplified by Q1075, added modulation terminal of TCXO (X1003), the FM modulation is made by reference oscillator.

The high frequency signal ingredient is amplified Q1075, and adjusted the level by volume Q1020 to make frequency balance between low frequency. After that, it is made FM modulation to transmit carrier by the modulator D1030 of VCO.

3-2. Drive and Final amplifier

The modulated signal from the VCO Q1051 is buffered by Q1040 and amplified by Q1032. Then the signal is buffered by Q1027 for the final amplifier driver Q1024. The low-level transmit signal is then applied to Q1019 for final amplification up to 5 watts output power.

The transmit signal then passes through the antenna switch D1012 and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-3. Automatic Transmit Power Control

The current detector Q1072 detects the current of Q1019 and Q1024, and converts the current difference to the voltage difference.

The output from the current detector Q1072 is compared with the reference voltage and amplified by the power control amplifier Q1072.

The output from Q1072 controls the gate bias of the final amplifiers Q1019 and the final amplifier driver Q1024.

The reference voltage changes into four values (TX Power High, Low3, Low2 and Low1) controlled by Q1020.

3-4. PLL Frequency Synthesizer

The frequency synthesizer consists of PLL IC, Q1068, VCO, TCXO (X1003) and buffer amplifier.

The output frequency from TCXO is 16.8MHz and the tolerance is ±2.5 ppm (in the temperature range -30 to +60 °C).

3-4-1. VCO

While the radio is receiving, the RX oscillator Q1046 in VCO generates a programmed frequency between 399.15 and 461.15MHz as 1st local signal.

While the radio is transmitting, the TX oscillator Q1051 in VCO generates a frequency between 450 and 512MHz.

The output from oscillator is amplified by buffer amplifier Q1040 and becomes output of VCO. The output from VCO is divided, one is amplified by Q1049 and feed back to the PLL IC 5pin. The other is amplified in Q1032 and in case of the reception, it is put into the mixer as the 1st local signal through D1023, in transmission, it is buffered Q1027, and more amplified in Q1024 through D1023 and it is put into the final amplifier Q1019.

3-4-2. VCV CNTL

Tuning voltage (VCV) of VCO is expanding the lock range of VCO by controlling the anode of varactor diode at the negative voltage and the control voltage from PLL IC. The negative voltage is added to the varactor diode after converted to negative by Q1030 which is output voltage of D/A converter Q1020.

3-4-3. PLL

The PLL IC consists of reference divider, main divider, phase detector, charge pumps and fractional accumulator. The reference frequency from TCXO is inputted to 8pin of PLL IC and is divided by reference divider. This IC is decimal point dividing PLL IC and the dividing ratio becomes 1/8 of usual PLL frequency step. Therefore, the output of reference divider is 8 times of frequencies of the channel step. For example, when the channel stepping is 5 kHz, the output of reference divider becomes 40 kHz.

The other hand, inputted feed back signal to 5 pin of PLL IC from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated.

The phase difference pulse and the pulse from fractional accumulator pass through the charge pumps and LPF. It becomes the DC voltage (VCV) to control the VCO.

The oscillation frequency of VCO is locked by the control of this DC voltage.

The PLL serial data from CPU is sent with three lines of SDO (20pin), SCK (22pin) and PSTB (27pin).

The lock condition of PLL is output from the UL (17Pin) terminal and UL becomes "H" at the time of the lock condition and becomes "L" at the time of the unlocked condition. The CPU always watches over the UL condition, and when it becomes "L" unlocked condition, the CPU prohibits transmitting and receiving.