# VXA-300 Circuit Description

***Receive Signal Path***

Incoming RF from the antenna jack is passed through a low-pass filter and high-pass filter consisting of coils L1022, L1025, L1026, L1027, L1028 & L1029, capacitors C1271,C1276,C1277,C1278,C1280,C1281,C1282,C1283,C1285,C1286,C1289,C1290,C1293,C1294 & C1295 and antenna switching diodes D1039 and D1042 to the receiver front end section.

Signals within the frequency range of the transceiver is applied to the receiver front end which contains RF amplifier Q1076 and varactor-tuned band-pass filter consisting of coils L1014, L1017, L1018, L1019, L1024, L1025 & L1031, capacitors C1241, C1243, C1245, C1246, C1248, C1250, C1255, C1256, C1259, C1266, C1272 & C1273, and diodes D1034, D1035, D1038 & D1041, then applied to the 1st mixer Q1068.

Buffered output from the VCO is amplified by Q1049 to provide a pure 1st local signal between 143.4 and 172.4 MHz for injection to the 1st mixer. The 35.4 MHz 1st mixer product then passes through monolithic crystal filter XF1001 (7.5 kHz BW) which strips away all but the desired signal, which is then amplified by mixer post-amp Q1061.

The amplified 1st IF signal is applied to the AM/FM IF subsystem IC Q1058, which contains the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier and AM/FM detector.

A 2nd local signal is generated by PLL IC Q1041 from the 17.475 MHz crystal X1002 .The17.475MHz signal is doubled by Q1054 to produce the 450 kHz 2nd IF when mixed with the 1st IF signal within Q1058. The 2nd IF then passes through the ceramic filter CF1001 to strip away unwanted mixer products.

In the FM mode, a 2nd IF signal from the ceramic filter CF1001 applied to the limiter amplifier section of Q1058, which removes amplitude variations in the 450 kHz IF before detection of the speech by the ceramic discriminator CD1001. Detected audio from Q1058 is passed through the de-emphasis, consisting of the resistors R1144, R1152, R1155 & R1199, capacitors C1118, C1119, C1124, C1149 & C1151, and Q1037-2.

In the AM mode, detected audio from Q1058 is passed through the audio amplifier Q1037-1 and ANL circuit, then applied to the AF amplifier Q1037-2. When impulse noise received, a portion of the AM detector output signal from the AM/FM IF subsystem Q1058, including pulse noise is rectified by D1019. The resulting DC is applied to the ANL MUTE gate Q1039, thus reducing the pulse noises.

The processed audio signal from Q1037-1 is passed through the AF mute and amplifier Q1037-2 to the audio tone equalizer Q1021, Q1018, Q1023, Q1026 and Q1020. The equalized audio signal is passed through the volume control to the audio power amplifier Q1001, providing up to 0.8 Watts to 16 Ω loudspeaker or audio power amplifier Q1005, providing up to 0.4 Watts to 8 Ω the headphone jack.

A portion of the AF signal from the AM/FM IF subsystem Q1058 converted into DC voltage within the IC, and then passes through the AGC amplifier Q1063 and Q1066 to the inversion amplifiers Q1075 and Q1062. These amplifier reduce the amplifier gain of the IF amplifier Q1061 and the RF amplifier Q1076 while receiving a strong signal.

***Squelch Control***

When signal is received, appear the DC squelch control voltage at pin 15 of AM/FM IF subsystem Q1058 according to the receiving signal strength. This DC is applied to pin 16 of microprocessor Q1024.

The DC squelch control voltage is compared with the SQL threshold level by the microprocessor Q1024. If the DC squelch control voltage is lower, pin 7 of Q1024 goes high. This signal activates the AF MUTE gate Q1037-2, thus disabling the AF audio.

Also, the microprocessor stops scanning, if active, and allows audio to pass through the AF MUTE gate Q1037-2.

***Transmit Signal Path***

Speech input from the microphone is passed through the microphone amplifier Q1011-1, then applied to the ALC amplifier Q1017. The amplified speech signal is passed through the high-pass filter Q1011-3 and low-pass filter Q1011-4, which adjust the modulation level, then fed to the AM modulator Q1069.

When using the optional headset, the SIDETONE signal from J1002 becomes “HIGH”, turning Pin10 of Q1024 on; pin 91 of Q1024 therefore a portion of the speech signal applied to the AF power amplifier Q1001 as a monitor signal.

The carrier signal from the VCO Q1046 passes through the buffer amplifier Q1049 and TX/RX switch D1026.

The signal from D1026 is amplified by Q1060 and Q1064, and ultimately applied to the final amplifier Q1069 which increases the signal level up to 5 watts output power. The transmit signal then passes through the antenna switch D1039, and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

***Automatic Transmit Power Control***

RF power output from the final amplifier is sampled by C1275/C1279 and is rectified by D1043. The resulting DC is fed through the Automatic Power Controller Q1074, thus allowing control of the power output.

***Transmit Inhibit***

When the transmit PLL is unlocked, pin 7 of PLL chip Q1041 goes to a logic low. The resulting DC “unlock” control voltage is switches off TX inhibit switches Q1053, and Q1055 to disable the supply voltage to transmitter RF amplifiers Q1048 and Q1049, disabling the transmitter.

***Spurious Suppression***

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency. Additional harmonic suppression is provided by a low-pass filter consisting of L1025, L1028 & L1029 and C1271, C1280, C1282, C1285, C1289 & C1293, resulting in more than 60 dB of harmonic suppression prior to delivery of the RF signal to the antenna.

***PLL Frequency Synthesizer***

PLL circuitry consists of VCO Q1046, VCO buffer Q1049 & Q1051, and PLL subsystem IC Q1041, which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and charge pump.

Stability is maintained by a regulated 3.5 V supply via Q1048 and 5V supply via Q1043 which feeds the PLL reference oscillator Q1041, as well as capacitors associated with the 17.475 MHz frequency reference crystal X1002.

In the receive mode, VCO Q1019 oscillates between 153.4 and 172.4 MHz. The VCO output is buffered by Q1049 and Q1051, and applied to the prescaler section of Q1041. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1041, before being applied to the programmable divider section of Q1041. The data latch section of Q1041 also receives serial dividing data from the microprocessor Q1024, which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 5 kHz derivative of the current VCO frequency.

Meanwhile, the reference divider section of Q1041 divides the 17.475 MHz crystal reference from the reference oscillator section by 3495 to produce the 5 kHz loop reference. The 5 kHz signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1041, which produces a pulsed output with pulse duration depending on the phase difference between

the input signals. This pulse train is filtered to DC and returned to the varactor D10124.

Changes in the level of the DC voltage applied to the varactors affect the reactance in the tank circuit of the VCO, changing the oscillating frequency of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator. The VCO is thus phase-locked to the crystal reference oscillator.

The output of the VCO Q1046 is buffered by Q1049 before application to the 1st mixer, as described previously.

For transmission, the VCO Q1046 oscillates between 118 and 137 MHz. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the receiving case).

Receive and transmit buses select which VCO is made active by Q1038. Q1077 and Q1078 amplify the Tune voltage for application to the tracking band-pass filters in the receiver front end.

When the power saving feature is active, the microprocessor periodically signals to the PLL IC Q1041 to conserve power, and to shorten lock-up time.

***Push-To-Talk Transmit Activation***

The PTT switch on the microphone is control to pin 22 of microprocessor Q1024, so that when the PTT switch is closed, pin 31 of Q1024 goes high. This signals cut off the receiver by disabling the 5 V supply bus at Q1034 which feeds the front-end, FM IF subsystem IC Q1058, and receiver VCO circuitry. At the same time, Q1055 and Q1053 activates the transmit 5 V supply line to enable the transmitter.