# VX-537 Circuit Description

## 1 Overview

The VX-537 is a UHF/FM hand-held transceiver designed to operate in the frequency range of 450 to 490 MHz.

## 2 Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 44.25 MHz and a second IF of 450 kHz. Incoming signals from the antenna are mixed with the local signal from PLL to produce the first IF of 44.25 MHz.

This is then mixed with the 43.8 MHz second local oscillator (using the 14.6 MHz reference crystal) output to produce the 450kHz second IF. This is detected to give the demodulated signal.

The transmit signal frequency is generated by PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

## 3 Receive Signal Path

### 3-1 Front-end RF Amplifier

Incoming RF from the antenna jack is delivered to the RF Unit and passes through a low-pass filter and high-pass filter consisting of coils L1003, L1004, L1006, L1008, L1001, L1002, L1005, L1007, L1009 & L1010, capacitors C1003, C1004, C1006, C1008, C1011, C1014, C1022, C1025, C1002, C1005, C1007, C1009, C1013,C1017,C1018, C1020, C1021, C1204, C1028 & C1031 and antenna switching diode D1004.

Signals within the frequency range of the transceiver are then amplified by Q1005 and enter a varactor-tuned band-pass filter consisting of coils L1016, L1017 & L1019, capacitors C1052, C1053, C1060, C1063, C1067, C1068, C1070, C1072, C1073, C1074, C1082, C1084 & C1092 resisters R1024, R1033 and R1048, and diodes D1008, D1009, D1010, D1011, D1012 & D1013 before first mixer.

### 3-2 First Mixer

Buffered output from the VCO is amplified by Q1012 to provide a pure first local signal between 405.75 and 445.75 MHz for injection to the first mixer Q1032. The 44.25 MHz first mixer product then passes through monolithic crystal filters XF1001 to strip away all but the desired signal.

### 3-3 IF Amplifier

The first IF signal is amplified by Q1027.

The amplified first IF signal is applied to FM IF subsystem IC Q1023 which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.

A second local signal is generated by Q1024 using the 14.6 MHz crystal X1001 as a reference, producing a 43.8 MHz signal which yields a 450 kHz second IF when mixed with the first IF signal within Q1023.

The second IF then passes through the ceramic filter CF1001 (wide channels), CF1002 (narrow channels) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1023, which removes amplitude variations in the 450 kHz IF, before detection of the speech by the ceramic discriminator CD1001.

### 3-4 Audio Amplifier

Detected audio from Q1023 is applied to Q2023 and audio low-pass filter, and then past the volume control (Q2017) to the audio amplifier Q2004 (external speaker) or Q2009 (internal speaker), providing up to 0.5 Watts to the optional headphone jack or 16-Ω loudspeaker.

***Attention: Audio output is BTL output.***

**3-5 Squelch Control**

The squelch circuitry consists of a noise amplifier & band-pass filter within Q1023, and noise detector D1025, D1027.

When no carrier received, noise at the output of the detector stage in Q1023 is amplified and band-pass filtered by the noise amplifier section of Q1023 and the network between pins 7 and 8, and then rectified by D1025

The resulting DC squelch control voltage is passed to pin 19 of the microprocessor Q2025.

If carrier is received, this signal causes pin 6 of Q2026 to go low and pin 89 of Q2025 to go high. Pin 6 of Q2026 signals Q2005, Q2013 and Q2016 to disable the supply voltage to the audio amplifier Q2004 and Q2009, while pin 89 makes Q2006 hold the green (Busy) half of the LED off, when pin 6 of Q2026 is low and pin 89 of Q2025 is high.

The microprocessor then checks the DTMF decoder chip on the Optional Unit, the CTCSS and the CDCSS code for DTMF or CTCSS or CDCSS code squelch information, if enabled, respectively. If not transmitting and CTCSS or CDCSS is not activated, or if the received tone or code matches that programmed, the microprocessor stops scanning, if active, and allows audio to pass through the audio amplifier Q2004, Q2009 to the loudspeaker by enabling the supply voltage to it via Q2005 and Q2011 .

**4 Transmit Signal Path**

**4-1 Microphone Amplifier**

Speech input from the microphone is amplified in Q2030 after there is a filter and is sent to Q2017 and sent to Dummy Unit (or Optional Unit). The audio, which returned from Dummy Unit, passes Q2023 to be pre-emphasized.

The processed audio is then mixed with a CTCSS tone generated by Q2023 and delivered to D1015 for frequency modulating the PLL carrier up to ±5 kHz from the unmodulated carrier at the transmitting frequency.

If a CDCSS code is enabled for transmission, the code is generated by the microprocessor Q2025 and delivered to X1001 (TCXO 14.6 MHz) for CDCSS modulating.

If DTMF is enabled for transmission, the tone is generated by the microprocessor Q2025 and applied to the splutter filter (Q2023) in place of speech audio. Also, the tone is amplified for monitoring in the loudspeaker.

**4-2 Noise Canceling Microphone Circuit**

The two signals from internal microphone (main and sub) are input to the positive input (sub) and to the negative input (main) and of the Q2030. If the same signal is input to both main and sub, the main signal is canceled at the output of Pin1 of the Q2030. In other words, noise from nearby sources not directly connected to the transceiver enters the main and sub input at the same signal and is therefore canceled out.

When a signal is only input to main and there is no signal at sub, the main signal is output as is from Q2030.

**4-3 Drive and Final Amplifier**

The modulated signal from the VCO Q1022 is buffered by Q1032 and amplified by Q1017 and Q1013. The low-level transmit signal is then applied to the Power Module Q1007 for final amplification up to 5 Watts output power.

The transmit signal then passes through the antenna switch D1004 and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

**4-4 Automatic Transmit Power Control**

RF power output from the final amplifier is sampled by C1016, C1019, is rectified by D1005. The resulting DC is fed back through Q1018 to the Power Module, and thus the power output.

The microprocessor selects either “High” or one of three “Low” power levels.

**4-5 Transmit Inhibit**

When the Transmit PLL is unlocked, pin 18 of PLL chip Q1025 goes to logic low. The resulting DC unlock control voltage is passed to pin 20 of the microprocessor Q2025. While the transmit PLL is unlocked, pin 85 of Q2025 remains low, which then turns off the Automatic Power Controller Q1011 and Q1018 to disable the supply voltage to the Power Module Q1007, disabling the transmitter.

**4-6 Spurious Suppression**

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to final transmitting frequency, modulated directly in the transmit VCO. Additional harmonic suppression is provided by a low-pass filter consisting of L1004, L1006 & L1008 and C1004, C1006, C1008, C1011, C1014 & C1022, resulting in more than 60 dB of harmonic suppression prior to delivery to the antenna.

**5 PLL Frequency Synthesizer**

PLL frequency synthesizer consists of the VCO Q1021 (RX) and Q1022 (TX), VCO buffers Q1017, Q1012, Q1016, PLL subsystem IC Q1025 and X1001 (TCXO 14.6MHZ).

The frequency stability is ±2.5 ppm within temperature range of -30 to +60 °C. the output of the 14.6 MHz reference is applied to pin 8 of the PLL IC.

While receiving, VCO oscillates between 405.75 MHz and 445.75 MHz according to the transceiver version and the programmed receiving frequency. The VCO generates 405.75 to 445.75 MHz for providing to the first local signal. In TX, the VCO generates 450 to 490 MHz.

The output of the VCO is amplified by the Q1016 and routed to the pin 5 of the PLL IC.

Also the output of the VCO is amplified by the Q1012 and routed first local /Power Module according to D1014.

The PLL IC consists of a prescaler, fractional divider, reference divider, phase comparator, and charge pump. This PLL IC is fractional-N type synthesizer and performs in the 40 or 50 kHz reference signal, which is eighth of the channel step (5, 6.25 or 7.5 kHz). The input signal from pin 5 and 8 of the PLL IC is divided down to the 40 or 50 kHz and compared at phase comparator. The pulsed output signal of the phase comparator is applied to the charge pump and transformed into DC signal in the loop filter. The DC signal is applied to the pin 1 of the VCO and locked to keep the VCO frequency constant.

PLL date is output from DTA (pin100), CLK (pin2) and PSTB (pin98) of the microprocessor Q2025. The data are input to PLL IC when the channel is changed or when transmission is changed to reception and vice versa. A PLL lock condition is always monitored by the pin20 of the Q2025. When the PLL is unlocked, the UL goes low.

**6 Miscellaneous Circuits**

**6-1 Push-To-Talk Transmit Activation**

The PTT switch on the microphone is connected to pin 32 of microprocessor Q2025, so that when the PTT switch is closed, pin 85 of Q2025 goes high. This signals the microprocessor to activate the TX / RX controller Q1003, which then disables the receiver by disabling the 5 V supply bus at Q1006 to the front-end, FM IF subsystem IC Q1023 and receiver VCO circuitry.

At the same time, Q1001, Q1002 activates the TX 5V supply line to enable the transmitter.