VX-1700 Circuit Description

Receive Signal Path

Incoming RF signal from the ANT jack is delivered to the PA Unit, and passes through the TX/RX relay RL2009 to J2006.

The RF signal is then applied to J1001 on the MAIN Unit, and passed through the limiter circuit consisting of D1006, D1007, D1008, and D1009 to prevent distortion from high RF signal input, and is fed to one of eight band-pass filters which strip away unwanted signals prior to delivery of the incoming signal to the RF amplifiers, Q1022 and Q1024.

The amplified RF signal passes through a low-pass filter to the doubly-balanced mixer D1032, where the RF signal is mixed with the 1st local signal delivered from buffer amplifier Q1029, resulting in a 45.274 MHz 1st IF signal.

The 45.274 MHz 1st IF signal is fed through monolithic crystal filter XF1001, which strips away unwanted mixer products, and is amplified by 1st IF amplifier Q1050; the 1st IF signal is then applied to the 2nd mixer Q1052, where it is mixed with the 45.25 MHz 2nd local signal delivered from buffer amplifier Q1075, resulting in a 24 kHz 2nd IF signal.

The 24 kHz 2nd IF signal is fed through buffer amplifiers Q1031 and Q1041 to the A/D converter Q1071, then delivered to the DSP IC Q1035, where the 24 kHz 2nd IF signal is demodulated in accordance with the mode selection data from the main CPU Q1018. The demodulated signal is delivered to the D/A converter Q1081 which converts the demodulated signal to audio.

The audio signal from the D/A converter Q1081 is fed through a low-pass filter at Q1036, which eliminates high-pitched noise on the audio signal, and is fed to the AF mute gate Q1092, then applied to the audio amplifier Q1055. The amplified audio signal is delivered to J3001 on the PANEL Unit, then passes through the speaker switch RL3001/Q3006 to the internal or external speaker.

The DSP IC Q1035 outputs AGC data which is proportionate to the received signal strength to the main CPU Q1018. The main CPU Q1018, in turn, outputs a DC voltage in accordance with the received signal strength. This DC voltage is fed through buffer amplifier Q1039 to RF amplifiers Q1022 & Q1024 and gate 2 of IF amplifier Q1050, to reduce their gains when strong signals are present in the receiver passband.

Transmit Signal Path

The speech audio from the microphone is delivered to J8001 on the MIC Unit, then applied to J1005 on the MAIN Unit.

The speech audio is amplified by Q1032-1, then passed though the clipper, D1044, and further amplified by Q1032-2.

The amplified speech audio is fed through the A/D converter Q1081, then delivered to the DSP IC Q1035, where the speech audio is modulated in the 24 kHz TX 1st IF signal in accordance with the mode selection data from the main CPU, Q1018.

The modulated signal is fed through the D/A converter Q1071 and buffer amplifier Q1034 to the singly-balanced mixer Q1054 where the 24 kHz TX 1st IF signal is mixed with 1st local signal delivered from buffer amplifier Q1075, resulting in a 45.25 MHz IF signal.

The resulting 45.25 MHz IF signal is buffered by Q1049, then delivered to the monolithic crystal filter XF1001, which strips away unwanted mixer products, and then is amplified by Q1043. The amplified IF signal is delivered to doubly-balanced mixer D1032, where it is mixed with the PLL local signal from the buffer amplifier, Q1029.

The resulting the RF signal at the transmit frequency is fed through a low-pass filter circuit, and then is amplified by Q1026 and buffer amplifier Q1025, and then filtered by one of eight band-pass filters to suppress out-of-band responses. The RF signal is then amplified by Q1001 and delivered to the PA Unit.

On the PA Unit, the low-level RF signal from the MAIN Unit is amplified by pre-driver Q2001, push-pull driver Q2008/Q2009, and push-pull final amplifier Q2012/Q2013, which provides up to 125 watts (below 4MHz) or 100 watts (above 4 MHz) of RF output power.

The RF output from the final amplifier is fed through the one of seven low-pass filters,

sampling directional coupler T2005, and TX/RX relay RL2009 before delivery to the antenna jack.

The sampling directional coupler senses forward and reverse power output, which is rectified by D2017 and D2018, respectively, and the DC voltage is then amplified by Q2015 on the PA Unit.

The DC voltages derived from forward and reverse power are applied to J1003 on the MAIN Unit, and then amplified by Q1040 and Q1044. The amplified DC voltage is fed back to the 2nd gate of the 45.275 MHz IF amplifier Q1043, so that the transmitter's IF gain can be regulated by this sensing of the power output, preventing overdrive or damage caused by transmission into an excessive impedance mismatch at the antenna.

PLL Circuit

The PLL local signal for the receiver 1st local and the transmitter final local is generated by one of two VCOs: Q1072 or Q1073 in conjunction with varactor diodes D1047, D1048, D1049, D1050, D1051, D1052, D1053, and D1054 on the MAIN Unit. The oscillating frequency is determined primarily by the level of DC voltage applied to the varactor diodes. The VCO output is buffered by Q1066, amplified by Q1074, and band-pass filtered by capacitors C1389, C1391, C1397, C1400, C1409, and C1420 and coils L1070, L1071, L1074, and L1076. The filtered PLL local signal is fed through buffer amplifiers Q1027, Q1028, and Q1029 to the TX final mixer or RX 1st mixer D1032.

A portion of the output of buffer amplifier Q1066 is further amplified by Q1064, then delivered to the PLL subsystem IC Q1056, which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. The sample VCO signal is divided by the programmable divider section of the Q1056. Meanwhile, the output from the 22.625 MHz TCXO reference oscillator, X1003, is amplified by Q1062 and divided by the DDS IC Q1060 in accordance with the PLL dividing data from the main CPU, Q1018, then fed through the buffer amplifiers Q1063 to ceramic filter CF1001. The divided and filtered reference signal is applied to the reference divider section of the PLL subsystem IC Q1056, where it is divided by 72 to produce the loop reference.

The divided signal from the programmable divider (derived from the VCO), and that derived from the reference oscillator, are applied to the phase detector section of the PLL subsystem IC Q1056, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is fed through the loop filter, consisting of resistor R1233 and capacitors C1298 and C1308, then fed back to the VCO varactor diodes D1047, D1048, D1049, D1050, D1051, D1052, D1053 and D1054.

Changes in the DC voltage applied to these varactor diodes affect the reactance in the tank circuit of VCOs Q1072 and Q1073, changing the oscillating frequency according to the phase difference between the signals derived from the VCO and the TCXO reference oscillator. The VCO is thus phase-locked to the reference frequency standard.

A portion of the output of reference signal from TCXO X1003 is multiplied by four at Q1070. The resulting 90.5 MHz signal is buffered by Q1075, then applied to a low-pass filter, consisting of capacitors C1401, C1405, C1410, C1411, and C1421 and coils L1075 and L1077. The filtered reference signal is applied to the TX 1st mixer Q1054 and RX 2nd mixer Q1052.

Control Circuit

Major frequency control functions such as channel selection, display, and PLL divider control are performed by main CPU Q1018 on the MAIN Unit, at the command of the user via the tuning knob and function switches on the front panel.

The programmable divider data for the PLL from the main CPU is applied directly to DDS IC Q1016 and PLL subsystem IC Q1056.

The Mode selection data from the main CPU is also delivered to DSP IC Q1035 to control the various circuits required for the selected mode.

The Band selection binary data from the main CPU is decoded (BCD to Decimal) by Q1011. The resulting decimal outputs are level-shifted by Q1003 to select the active band-pass filter on the MAIN Unit required for the operating frequency. Also, the decimal outputs from Q1003 are delivered to PA Unit, where they are used to select the active low-pass filter required for the operating frequency.

TX/RX Control

When the PTT switch is pressed, pin 21 of the main CPU goes low, which causes pin 60 of the main CPU to go high. This signal disables the receiver 12 V bus at Q1046. At the same time, pin 59 of the main CPU goes high to activate the transmit 12 V bus at Q1048.

Power Supply & Regulation

The +5 V bus for the main CPU is derived from the 13.5 V bus via regulator Q1012 on the MAIN Unit. The +8 V bus is derived from the 13.5 V bus via regulator Q1007 on the MAIN Unit.

A portion of the +8 V bus is regulated by Q1008 for the +5 V bus, and is regulated by Q1006 for the +2.6 V bus required by the DSP IC Q1035.