# VXR-9000V Circuit Description

***Receive Signal Path***

Incoming RF from the RX antenna jack is delivered to the MAIN Unit and passes through the protection diode D1001 and D1002 and a varactor-tuned band pass filter consisting of coils L1044 and L1048, capacitors C1400, C1402, C1403, C1407, C1408, C1409 and C1410, and varactor diodes D1033 and D1034.

Signals are then applied to the RF amplifier, Q1063. The amplified RF signal is applied through a varactor-tuned band pass filter consisting of coils L1050 and L1051, capacitors C1427, C1429, C1430, C1431, C1433, C1434, C1435 and C1436, and varactor diode D1035 and D1036 to the 1st mixer Q1018 along with the first local signal from the PLL circuit.

The first local signal is generated between 221.35 and 247.35 MHz by the RX VCO, which consists of FET Q1048 and varactor diodes D1018, D1019, D1020 and D1021 according to the programmed receiving frequency; the local signal then passes through buffer amplifier Q1059 and first local amplifier Q1019 to the first mixer Q1018.

The 73.35 MHz first IF signal is applied to monolithic crystal filters XF1001/XF1002 (Wide) or XF1501/XF1502 (Narrow) which strip away unwanted mixer products, and the IF signal is applied to the first IF amplifiers Q1022 (Wide) / Q1502 (Narrow). The amplified first IF signal is then delivered to the FM IF subsystem IC Q1028, which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and FM detector.

A 2nd local oscillator signal, generated by the 72.895 MHz crystal X1002, produces the 455 kHz second IF signal when mixed with the first IF signal within Q1028. The second IF signal passes through ceramic filter CF1001 or CF1002 which strips away all but the desired signal, and then passes through the limiter amplifier within Q1028 to ceramic discriminator CD1001, which removes any amplitude variations in the 455 kHz IF signal before detection of speech. The detected audio passes through the low pass filter, consisting of R1199 and C1244, which rejects the 455 kHz IF component.

The audio signal from the MAIN Unit is delivered to the CNTL Unit and passes through the audio amplifier Q1020 to the active high pass filter section of Q3020, which rejects the sub-audible frequency component. The filtered audio signal is delivered to electronic volume Q1056, which adjusts the audio sensitivity to compensate for audio level variations, then passes through audio amplifier Q1020, audio switch Q1040, attenuator consisting of R1233, and limiter amplifier Q1050, to the electronic volume control Q1056, where the maximum deviation is set. The audio signal subsequently passes through the 3-section active low pass filter consisting of Q1017-1/-2/-3 and audio amplifier Q1001 to providing the repeater transmit audio.

A portion of the audio signal from the active high pass filter section of Q3020 is de-emphasized by R3095 and C3080, providing a flat audio response. The filtered audio then passes through the active band pass filter Q3021 and audio mute gate Q3015 to audio power amplifier Q1057, providing up to 2 Watts of audio power to the 8 Ω loudspeaker.

***Sub-Audible Signaling (DECODER)***

A portion of the audio signal from the audio amplifier Q1020 passes through the 3-section active low pass filter Q1025 and the low pass filtering section of Q3020 to separate the CTCSS tones from the received audio signal. The CTCSS tones are sent to the CTCSS decoder section of Q3020. When a CTCSS tone is received, the CTCSS information is delivered to pin 77 of Main CPU Q3014 from pin 4 and 8 of Q3020 which compares the CTCSS tone with the programmed tone.

Another portion of the audio signal amplified by Q1020 passes through the 3-section active low pass filter Q3044 to separate the DCS codes from the received audio signal. The low pass filtered signal passes through the phase detector Q3044 to pin 39 of Main CPU Q3014. When a DCS code is received, the Main CPU Q3014 compares the DCS code with

the programmed code.

If the received CTCSS tone or DCS code matches the programmed tone or code, pin 4 of the Main CPU Q3014 goes low, turning off the squelch switch Q3015 and passing the received audio signal to the audio power amplifier Q1057.

***Squelch Control***

The squelch circuit consists of noise amplifier Q1033 and noise detector D1015 on the MAIN Unit, and control circuitry within Main CPU Q3014 on the CNTL Unit.

When no carrier is received, noise at the output of the audio detector stage of Q1028 is amplified by Q1033, and then rectified by D1015 to provide a DC control voltage for the squelch switch. The resulting DC voltage is delivered to pin 23 of J1005.

The DC voltage from the MAIN Unit is delivered to the A-D analog input port (pin 51) of the Main CPU Q3014 on the CNTL Unit, which compares the squelch threshold level to that which is memorized in EEPROM Q3006 or set by the front panel SQL control.

***RX PLL and VCO Circuits***

The receiver's PLL circuitry consists of PLL subsystem IC Q1052 on the MAIN Unit, which contains a reference oscillator/divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. Stability is obtained by a regulated 5 V DC supply via Q1062 and temperature compensated 14.4 MHz crystal oscillator X1003.

The RX VCO made up two VCO circuit, one is Low-Band RX VCO, consisting of FET Q1048 and varactor diodes D1018, D1019, D1020 and D1021, and another one is High-Band RX VCO, consisting of FET Q1049 and varactor diodes D1027, D1028, D1029 and D1030, oscillates between 221.35 MHz and 247.35 MHz according to the programmed receiving frequency. The RX VCO output passes through buffer amplifier Q1059 and first local amplifier Q1019 to the first mixer Q1018, as described previously. A portion of the RX VCO output is applied to the prescaler/swallow counter section of PLL IC Q1052. There the RX VCO signal is divided by 64 or 65, according to a control signal from the Main CPU Q3014 on the CNTL Unit, before being applied to the programmable divider section of PLL IC Q1052.

The data latch section of the PLL IC Q1052 also receives serial dividing data from the Main CPU Q3014, which causes the pre-divided RX VCO signal to be further divided by 75,330 – 81,330 (or 60,264 – 65,064) in the programmable divider section of PLL IC Q1052, depending upon the desired receive frequency, so as to produce a 5 kHz (or 6.25 kHz) derivative of the current RX VCO frequency. Meanwhile, the reference divider section of the PLL IC Q1052 divides the 14.4 MHz crystal reference from the reference oscillator X1003 and Q1045 by 2880 (or 2304) to produce the 5 kHz (or 6.25 kHz) loop reference.

The 5 kHz or 6.25 kHz signal from the programmable divider (derived from the RX VCO) and that derived from the crystal are applied to the phase detector section of the PLL IC Q1052, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is then converted to DC, low pass filtered, then fed back to the RX VCO varactor diodes D1018/D1019/D1020/D1021 and D1027/D1028/D1029/D1030.

Changes in the DC voltage applied to the varactor diodes D1018/D1019/D1020/D1021 and D1027/D1028/D1029/D1030 affect the reactance in the tank circuit RX VCO Q1048/Q1049, changing the oscillating frequency according to the phase difference between the signals derived from the RX VCO and the crystal reference oscillator. The RX VCO is thus phase-locked to the reference frequency standard.

***Transmit Signal Path***

The speech audio from the CNTL Unit is applied to the varactor diode D1010, which frequency modulates the TX VCO from the unmodulated carrier at the transmit frequency. The modulated transmit signal is buffered by Q1026, then passes through the RF amplifier

Q1030 and RF diode switch D1016 to the PA Unit.

The transmit signal is applied to the RF amplifier Q5001 and Q5008, then finally amplified by power amplifier Q5015 and Q5016 up to 50 Watts. Harmonic and spurious radiation in the final output is suppressed by a low pass filter consisting of coils L5007, L5008 and L5010, plus capacitors C5071, C5078, C5082, C5085, C5088 and C5125 on the PA Unit, before delivery to the TX antenna jack.

***TX PLL and VCO Circuits***

The transmitter's PLL circuitry consists of PLL subsystem IC Q1008 on the MAIN Unit, which contains a reference oscillator/divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. Stability is obtained by a regulated 5 V DC supply via Q1062 and temperature compensated 14.4 MHz crystal oscillator X1001.

The TX VCO consisting of FET Q1021 and varactor diodes D1008 and D1019 oscillates between 148 MHz and 174 MHz according to the programmed transmit frequency. The theory of operation of the remainder of the PLL circuitry is similar to that of the RX PLL circuit; however, dividing data from the Main CPU Q3014 on the CNTL Unit is such that the VCO frequency is the actual transmit frequency.

***APC (Automatic Power Control)***

RF power output from the final amplifier Q5015/Q5016 is sampled by C5056/C5061 and is then rectified by D5007 and D5008. The resulting DC voltage from the Main CPU Q3014 on the CNTL Unit, to produce a control voltage for the Automatic Power Controller Q5004 and Q5002, which regulates supply voltage to Q5001.

***CNTL (Control) Unit***

The CNTL Unit consists of 8-bit CPU Q3014, EEPROM Q3006, RX and TX speech audio circuits, and various analog switches for the CPU and repeater interconnections.

Microprocessor operational code is stored in Q3006, while channel data and repeater configuration information is programmed from an external PC connected to the front panel's MIC jack via a VPL-1 programming cable.

The output from the Main CPU Q3014 contains serial control data used for REPEATER/BASE mode control, as well as TX and RX PLL data. Crystal X3002 oscillates at 12.288 MHz, and provides stable clock timing for the Main CPU. When the repeater is powered on, the voltage at pin 62 of Q3014 becomes stable, and the output of voltage detector IC Q3012, which is tied to pin 59 (RST) of Q3014 becomes high, resetting the Main CPU.

***Base Operation (TX, Mic-Input Audio)***

Microphone input is delivered past the MIC MUTE switch Q4002, then passes through the audio amplifier and active high pass filter at Q4001.

passed through the microphone amplifier Q1011-1, then applied to the ALC amplifier Q1017. The amplified speech signal is passed through the high-pass filter Q1011-3 and low-pass filter Q1011-4, which adjust the modulation level, then fed to the AM modulator Q1069.

When using the optional headset, the SIDETONE signal from J1002 becomes "HIGH", turning Pin10 of Q1024 on; pin 91 of Q1024 therefore a portion of the speech signal applied to the AF power amplifier Q1001 as a monitor signal.

The carrier signal from the VCO Q1046 passes through the buffer amplifier Q1049 and TX/RX switch D1026.

The signal from D1026 is amplified by Q1060 and Q1064, and ultimately applied to the final amplifier Q1069 which increases the signal level up to 5 watts output power. The transmit signal then passes through the antenna switch D1039, and is low-pass filtered to

suppress away harmonic spurious radiation before delivery to the antenna.

***Automatic Transmit Power Control***

RF power output from the final amplifier is sampled by C1275/C1279 and is rectified by D1043. The resulting DC is fed through the Automatic Power Controller Q1074, thus allowing control of the power output.

***Transmit Inhibit***

When the transmit PLL is unlocked, pin 7 of PLL chip Q1041 goes to a logic low. The resulting DC “unlock” control voltage is switches off TX inhibit switches Q1053, and Q1055 to disable the supply voltage to transmitter RF amplifiers Q1048 and Q1049, disabling the transmitter.

***Spurious Suppression***

Generation of spurious products by the transmitter is minimized by the fundamental carrier frequency being equal to the final transmitting frequency. Additional harmonic suppression is provided by a low-pass filter consisting of L1025, L1028 & L1029 and C1271, C1280, C1282, C1285, C1289 & C1293, resulting in more than 60 dB of harmonic suppression prior to delivery of the RF signal to the antenna.

***PLL Frequency Synthesizer***

PLL circuitry consists of VCO Q1046, VCO buffer Q1049 & Q1051, and PLL subsystem IC Q1041, which contains a reference divider, serial-to-parallel data latch, programmable divider, phase comparator and charge pump.

Stability is maintained by a regulated 3.5 V supply via Q1048 and 5V supply via Q1043 which feeds the PLL reference oscillator Q1041, as well as capacitors associated with the 17.475 MHz frequency reference crystal X1002.

In the receive mode, VCO Q1019 oscillates between 153.4 and 172.4 MHz. The VCO output is buffered by Q1049 and Q1051, and applied to the prescaler section of Q1041. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1041, before being applied to the programmable divider section of Q1041. The data latch section of Q1041 also receives serial dividing data from the microprocessor Q1024, which causes the pre-divided VCO signal to be further divided in the programmable divider section, depending upon the desired receive frequency, so as to produce a 5 kHz derivative of the current VCO frequency.

Meanwhile, the reference divider section of Q1041 divides the 17.475 MHz crystal reference from the reference oscillator section by 3495 to produce the 5 kHz loop reference. The 5 kHz signal from the programmable divider (derived from the VCO) and that derived from the reference oscillator are applied to the phase detector section of Q1041, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is filtered to DC and returned to the varactor D10124.

Changes in the level of the DC voltage applied to the varactors affect the reactance in the tank circuit of the VCO, changing the oscillating frequency of the VCO according to the phase difference between the signals derived from the VCO and the crystal reference oscillator. The VCO is thus phase-locked to the crystal reference oscillator.

The output of the VCO Q1046 is buffered by Q1049 before application to the 1st mixer, as described previously.

For transmission, the VCO Q1046 oscillates between 118 and 137 MHz. The remainder of the PLL circuitry is shared with the receiver. However, the dividing data from the microprocessor is such that the VCO frequency is at the actual transmit frequency (rather than offset for IFs, as in the receiving case).

Receive and transmit buses select which VCO is made active by Q1038. Q1077 and Q1078 amplify the Tune voltage for application to the tracking band-pass filters in the receiver front end.

When the power saving feature is active, the microprocessor periodically signals to the PLL IC Q1041 to conserve power, and to shorten lock-up time.

***Push-To-Talk Transmit Activation***

The PTT switch on the microphone is control to pin 22 of microprocessor Q1024, so that when the PTT switch is closed, pin 31 of Q1024 goes high. This signals cut off the receiver by disabling the 5 V supply bus at Q1034 which feeds the front-end, FM IF subsystem IC Q1058, and receiver VCO circuitry. At the same time, Q1055 and Q1053 activates the transmit 5 V supply line to enable the transmitter.