VXR-9000V-A Circuit Description

Receive Signal Path

Incoming RF from the RX antenna jack is delivered to the RX Unit and passes through the protection diode D1001 and a varactor-tuned band pass filter consisting of coils L1003 and L1004, capacitors C1015, C1018, C1021, C1032, and C1044, and diodes D1003 and D1004. Signals are then applied to the RF amplifier, Q1009. The amplified RF signal is applied through a varactor-tuned band pass filter consisting of coils L1010 and L1011, capacitors C1079, C1092, C1082, C1095 and C1075, and diodes D1007 and D1005 to the first mixer Q1018 along with the first local signal from the PLL circuit.

The first local signal is generated between 207.35 MHz and 233.35 MHz by the RX VCO, which consists of FET Q1048 and varactor diodes D1018, D1019 according to the programmed receiving frequency; the local signal then passes through buffer amplifier Q1059 and first local amplifier Q1019 to the first mixer Q1018.

The 73.35 MHz first IF signal is applied to monolithic crystal filters XF1001 and XF1002 which strip away unwanted mixer products, and the IF signal is applied to the first IF amplifiers Q1022. The amplified first IF signal is then delivered to the FM IF subsystem IC Q1028, which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and FM detector.

The second local oscillator signal, generated by the 72.895 MHz crystal X1002, produces the 455 kHz second IF signal when mixed with the first IF signal within Q1028. The second IF signal passes through ceramic filter CF1001 or CF1002 which strips away all but the desired signal, and then passes through the limiter amplifier within Q1028 to ceramic discriminator CD1001, which removes any amplitude variations in the 455 kHz IF signal before detection of speech. The detected audio passes through the low pass filter, consisting of R1199 and C1244, which rejects the 455 kHz IF component.

The audio signal from the RX Unit is delivered to the CNTL Unit and passes through the audio amplifier Q1020 to the active high pass filter section of Q3020, which rejects the sub-audible frequency component. The filtered audio signal is delivered to electronic volume Q1056, which adjusts the audio sensitivity to compensate for audio level variations, then passes through audio amplifier Q1020, audio switch Q1040, attenuator consisting of R1233, and limiter amplifier Q1050, to the electronic volume control Q1056, where the maximum deviation is set. The audio signal subsequently passes through the 3-section active low pass filter consisting of Q1017-1/-2/-3 and audio amplifier Q1001 to providing the repeater transmit audio.

A portion of the audio signal from the active high pass filter section of Q4024 is de-emphasized consisting of Q3036, R3198, and C3144, providing a flat audio response. The filtered audio then passes through the active band pass filter Q3021 and audio mute gate Q3015 to audio power amplifier Q1057, providing up to 2 Watts of audio power to the 8 Ω loudspeaker.

Sub-Audible Signaling (Decoder)

A portion of the audio signal from the audio amplifier Q1020 passes through the 3-section active low pass filter Q1025 and the low pass filtering section of Q3020 to separate the CTCSS tones from the received audio signal. The CTCSS tones are sent to the CTCSS decoder section of Q3020. When a CTCSS tone is received, the CTCSS information is delivered to pin 20 of the Main CPU Q3014 from pin 4 and 8 of Q3020, which compares the CTCSS tone with the programmed tone.

Another portion of the audio signal amplified by Q1020 passes through the 3-section active low pass filter Q3044 to separate the DCS codes from the received audio signal. The low pass filtered signal passes through the phase detector Q3044 to pin 39 of the Main CPU Q3014. When a DCS code is received, the Main CPU Q3014 compares the DCS code with the programmed code.

If the received CTCSS tone or DCS code matches the programmed tone or code, pin 4 of the Main CPU Q3014 goes low, turning on the squelch switch Q3015 and passing the received audio signal to the audio power amplifier Q1057.

Squelch Control
The squelch circuit consists of noise amplifier Q1033 and noise detector D1015 on the RX Unit, and control circuitry within main microprocessor Q3014 on the CNTL Unit.

When no carrier is received, noise at the output of the audio detector stage of Q1028 is amplified by Q1033, and then rectified by D1015 to provide a DC control voltage for the squelch switch. The resulting DC voltage is delivered to pin 23 of J1005.

The DC voltage from the RX Unit is delivered to the A-D analog input port (pin 51) of the Main CPU Q3014 on the CNTL Unit, which compares the squelch threshold level to that which is memorized in EEPROM Q3006 or set by the front panel SQL control

RX PLL and VCO Circuits

The receiver's PLL circuitry consists of PLL subsystem IC Q1052 on the MAIN Unit, which contains a reference oscillator/divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. Stability is obtained by a regulated 5 VDC supply via Q1062 and temperature compensated 14.4 MHz crystal oscillator X1003.

The RX VCO made up tow VCO circuits, one is Low-Band RX VCO, consisting of FET Q1048 and varactor diodes D1018, D1019, and another one is High-Band RX VCO, consisting of FET Q1049 and varactor diodes D1020 and D1021, oscillates between 207.35 MHz and 233.35 MHz according to the programmed receiving frequency. The RX VCO output passes through buffer amplifier Q1059 and first local amplifier Q1019 to the first mixer Q1018, as described previously. A portion of the RX VCO output is applied to the prescaler/swallow counter section in the PLL IC, Q1052. There the RX VCO signal is divided by 64 or 65, according to a control signal from the Main CPU Q3014 on the CNTL Unit, before being applied to the programmable divider section of the PLL IC Q1052.

The data latch section of the PLL IC Q1052 also receives serial dividing data from the Main CPU Q3014, which causes the pre-divided RX VCO signal to be further divided by 75,330 to 81,330 (or 60,264 to 65,064) in the programmable divider section in the PLL IC Q1052, depending upon the desired receive frequency, so as to produce a 5 kHz (or 6.25 kHz) derivative of the current RX VCO frequency. Meanwhile, the reference divider section of the PLL IC Q1052 divides the 14.4 MHz crystal reference from the reference oscillator X1003 and Q1045 by 2880 (or 2304) to produce the 5 kHz (or 6.25 kHz) loop reference.

The 5 kHz or 6.25 kHz signal from the programmable divider (derived from the RX VCO) and that derived from the crystal are applied to the phase detector section of the PLL IC Q1052, which produces a pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is then converted to DC, low pass filtered, then fed back to the RX VCO varactor diodes D1018/D1019 and D1020/D1021.

Changes in the DC voltage applied to the varactor diodes D1018/D1019 and D1020/D1021 affect the reactance in the tank circuit RX VCO Q1048/1049, changing the oscillating frequency according to the phase difference between the signals derived from the RX VCO and the crystal reference oscillator. The RX VCO is thus phase-locked to the reference frequency standard.

Transmit Signal Path

The speech audio from the CNTL Unit is applied to the varactor diode D1010, which frequency modulates the TX VCO from the unmodulated carrier at the transmit frequency. The modulated transmit signal is buffered by Q1026, then passes through the RF amplifier Q1030 and RF diode switch D1016 to the PA-2 Unit.

The transmit signal is applied to the RF drive amplifier Q8003, then finally amplified by power amplifier Q8007 up to 50 Watts. Harmonic and spurious radiation in the final output is suppressed by a low pass filter consisting of coils L8005 to L8007, plus capacitors C8055, C8057, C8058, C8059, C8060 and C8061 on the PA-2 Unit, before delivery to the TX antenna jack.

TX PLL and VCO Circuits

The Transmitter's PLL circuitry consists of PLL subsystem IC Q1008 on the MAIN Unit, which contains a reference oscillator/divider, serial-to-parallel data latch, programmable divider, phase comparator and a swallow counter. Stability is obtained by a regulated 5 VDC supply via Q1062 and temperature compensated 14.4 MHz crystal oscillator X1001.

The TX VCO, consisting of FET Q1021 and varactor diodes D1008, D1009, oscillates between 134 MHz and 160 MHz according to the programmed transmit frequency. The theory of operation of the remainder of the PLL circuitry is similar to that of the RX PLL circuit; however, dividing data from the Main CPU Q3014 on the CNTL Unit is such that the VCO frequency is the actual transmit frequency.

APC (Automatic Power Control)

RF power output from the final amplifier Q8007 is sampled by C8041/C8044 and is then rectified by D8006/D8007. The resulting DC voltage is applied to the comparator Q8018, where the voltage is compared with a reference voltage from the Main CPU Q3014 on the CNTL Unit, to produce a control voltage for the Automatic Power Controller Q8006, which regulates supply voltage to Q8004.

CONTROL (CNTL) Unit

The CNTL Unit consists of 8-bit CPU Q3014, EEPROM Q3006, RX and TX speech audio circuits, and various analog switches for the CPU and repeater interconnections.

Microprocessor operational code is stored in Q3006, while channel data and repeater configuration information is programmed from an external PC connected to the front panel's MIC jack via a VPL-1 programming cable.

The output from the Main CPU Q3014 contains serial control data used for REPEATER/BASE mode control, as well as TX and RX PLL data. Crystal X3002 oscillates at 12.288 MHz, and provides stable clock timing for the Main CPU. When the repeater is powered on, the voltage at pin 62 of Q3014 becomes stable, and the output of voltage detector IC Q3012, which is tied to pin 59(RST) of Q3014 becomes high, resetting the Main CPU.

Base Operation (TX, Mic-Input Audio)

Microphone input is delivered past the MIC MUTE switch Q4002, then passes through the audio amplifier and active high pass filter at Q4001 where the signal is processed in the same manner as previously described.