VX-4107/VX-4207 Circuit Description

1. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 50.85 MHz and a second IF of 450 kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 50.85 MHz.
This is then mixed with the 50.4 MHz second local oscillator output to produce the 450 kHz second IF. This is detected to give the demodulated signal.
The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, antenna switching diode, and removed undesired frequencies by varactor diode (tuned band-pass filer: L1047, L1048, L1049, C1030, C1041, C1045, C1057, C1065, C1083, C1058 and C1091).

The passed signal is amplified in Q1022 and moreover cuts an image frequency with the band path filter and comes into the 1st mixer. The Q1020 controls bias of Q1022.

2-2. First Mixer

The 1st mixer consists of the Q1035, T1004, T1005 and T1006. Buffered output from the VCO is amplified by Q1038 to provide a pure first local signal between 349.15 and 419.15 MHz for injection to the first mixer.

The output IF signal is amplified by Q1046 and enters from the mixer to the crystal filter.

The IF signal then passes through monolithic crystal filters XF1001 (±5.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by Q1059.

The amplified first IF signal is applied to FM IF subsystem IC Q1079 which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.

The signal from reference oscillator X1003 becomes 3 times of frequencies in Q1079, it is mixed with the IF signal and becomes 450 kHz.

The second IF then passes through the ceramic filter CF1001 (for wide channels), CF1002 (for narrow channels) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1091, which removes amplitude variations in the 450 kHz IF, before detection of the speech by the ceramic discriminator CD1001.

2-4. Audio amplifier

Detected signal from Q1079 is inputted to Q1037 and is output through the band path filter inside Q1037.

In the case an optional unit is installed, the Q1063 is made OFF and the AF signal from Q1037 goes the optional unit. In the case an optional unit is not installed, Q1037 is made ON and the signal goes through Q1063.

The signal then goes through AF mute switch Q1068, de-emphasis part and expander Q1021. When the function of expander is off, the Q1021 will be bypassed by Q1069.

The output signal of expander (or a signal from de-emphasis) is amplified by Q1066 and it is amplified with AF power amplifier Q1005 after passing AF volume Q1029.

The output of Q1005 drives a speaker (it chooses the external SP or internal SP in J6001)

2-5. Squelch Circuit

There are 13 levels of squelch setting from 0 to 12. The level 0 means open the squelch. The level 1 means the threshold setting level and level 11 means tight

squelch.
From 2 to 10 is established in the middle of threshold and tight. The bigger figure is nearer the tight setting.
The level 12 becomes setting of carrier squelch.

2-5-1. Noise Squelch

Noise squelch circuit is composed of the band path filter of Q1079, noise amplifier Q1091, and noise detector D1059, D1061.
When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1079 is amplified in Q1091 through the band path filter Q1079, is detected to DC voltage with D1059, D1061 and is inputted to 19pin (the A/D port) of the Q1083 (CPU).
When a carrier is received, the DC voltage becomes low because the noise is compressed.
When the detected voltage to CPU is high, the CPU stops AF output with Q1068 "OFF" by making the 40pin "L" level.
When the detection voltage is low, the CPU makes Q1068 ON with making 40pin "H" and the AF signal is output.

2-5-2. Carrier Squelch

The CPU (18pin: A/D port) detect RSSI voltage output from Q1079 12 pin, and controls AF output.
The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage.
The process of the AF signal control is same as Noise Squelch
The shipping data is adjusted 3 dB higher than squelch tight sensitivity.

3. Transmitter System

3-1. Mic Amplifier

The AF signal from microphone jack J4001 (4ch) or J5001 (501ch) is amplified with microphone amplifier Q1066, is amplified with 2nd microphone amplifier Q1088 after microphone selection switch Q1016, and passes microphone gain volume Q1029.
The AF signal which was controlled in the correct gain passes compandor Q1021. When not using a compandor, with the control from the CPU, it passes in the compandor circuit inside of Q1021 and it is output and it passes a pre-emphasis circuit. Q1063 becomes OFF when an option unit is attached and the AF signal from Q1037 goes via the option unit. When an option unit isn't attached, Q1063 becomes ON, the signal passes Q1063 and is input to Q1037.
The signal passed limiter and splatter filer of Q1037 is adjusted by maximum deviation adjustment volume Q1029.
The adjusted low frequency signal ingredient is amplified by Q1074, added modulation terminal of TCXO (X1003), the FM modulation is made by reference oscillator.
The high frequency signal ingredient is amplified Q1074, and adjusted the level by volume Q1029 to make frequency balance between low frequency. After that, it is made FM modulation to transmit carrier by the modulator D1030 of VCO.

3-2. Drive and Final amplifier

The modulated signal from the VCO Q1054 is buffered by Q1049 and amplified by Q1038 and Q1094. The low-level transmit signal is then applied to the Power Module Q1028 for final amplification up to 45 watts output power.
The transmit signal then passes through the antenna switch D1005 and D1006 and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-3. Automatic Transmit Power Control

The output power of Power Module is detected by CM coupler, it is detected by D1013 and D1014 and is input to comparator Q1095.

The cooperator compares two different voltages and makes output power stable by controlling the bias voltage of Power Module.
There are 3 levels of output power (Hi, Mid and Lo), it is switched by the voltage of Q1029-1CH.

3-4. PLL Frequency Synthesizer

The frequency synthesizer consists of PLL IC, Q1085, VCO and TCXO (X1003) and buffer amplifier.
The output frequency from TCXO is 16.8 MHz and the tolerance is ±2.5 ppm (in the temperature range -30 to +60 degrees).

3-4-1. VCO

While the radio is receiving, the RX oscillator Q1054 in VCO generates a programmed frequency between 349.15 and 419.15 MHz as 1st local signal.
While the radio is transmitting, the TX oscillator Q1058 in VCO generates a frequency between 400 and 470 MHz.
The output from oscillator is amplified by buffer amplifier Q1049 and becomes output of VCO. The output from VCO is divided, one is amplified by Q1057 and feed back to the PLL IC 5pin. The other is amplified in Q1038 and in case of the reception, it is put into the mixer as the 1st local signal through D1022, in transmission, it is amplified in Q1038, and more amplified in Q1094 through D1022 and it is put the input terminal of the Power Module.

3-4-2. VCV CNTL

Tuning voltage (VCV) of VCO is expanding the lock range of VCO by controlling the anode of varactor diode at the negative voltage and the control voltage from PLL IC. The negative voltage is added to the varactor diode after converted to negative by Q1035, which is output voltage of D/A converter Q1029.

3-4-3. PLL

The PLL IC consists of reference divider, main divider, phase detector, charge pumps and fractional accumulator. The reference frequency from TCXO is inputted to 8pin of PLL IC and is divided by reference divider. This IC is decimal point dividing PLL IC and the dividing ratio becomes 1/8 of usual PLL frequency step. Therefore, the output of reference divider is 8 times of frequencies of the channel step. For example, when the channel stepping is 5 kHz, the output of reference divider becomes 40 kHz.
The other hand, inputted feed back signal to 5 pin of PLL IC from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated.
The phase difference pulse and the pulse from fractional accumulator pass through the charge pumps and LPF. It becomes the DC voltage (VCV) to control the VCO.
The oscillation frequency of VCO is locked by the control of this DC voltage.
The PLL serial data from CPU is sent with three lines of SDO (2pin), SCK (1pin) and PSTB (3pin).
The lock condition of PLL is output from the UL (18Pin) terminal and UL becomes "H" at the time of the lock condition and becomes "L" at the time of the unlocked condition. The CPU always watches over the UL condition, and when it becomes "L" unlocked condition, the CPU prohibits transmitting and receiving.