

## VX-920/970 (UHF) series Circuit Description

### 1. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 50.85MHz and a second IF of 450kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 50.85MHz.

This is then mixed with the 50.4MHz second local oscillator output to produce the 450kHz second IF. This is detected to give the demodulated signal.

The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

### 2. Receiver System

#### 2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filter, antenna switching diode, high pass filter and removed undesired frequencies by varactor diode (tuned band-pass filter).

The passed signal is amplified in Q1022 and moreover cuts an image frequency with the tuned band pass filter and comes into the 1st mixer.

#### 2-2. First Mixer

The 1st mixer consists of the Q1034, T1001, T1002 and T1003. Buffered output from the VCO is amplified by Q1033 to provide a pure first local signal between 399.15 and 461.15MHz for injection to the first mixer.

The IF signal then passes through monolithic crystal filters XF1001 ( $\pm 5.5$  kHz BW) to strip away all but the desired signal.

#### 2-3. IF Amplifier

The first IF signal is amplified by Q1058.

The amplified first IF signal is applied to FM IF subsystem IC Q1067 which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.

The signal from reference oscillator X1003 becomes 3 times of frequencies in Q1067, it is mixed with the IF signal and becomes 450kHz.

The second IF then passes through the ceramic filter CF1001 (wide channels), CF1002 (narrow channels) to strip away unwanted mixer products, and is applied to the limiter amplifier in Q1067, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD1001.

#### 2-4. Audio amplifier

Detected signal from Q1067 is inputted to Q1032 and is output through the band path filter inside Q1032.

In the case an optional unit is installed, the Q1078 is made OFF and the AF signal from Q1032 goes the optional unit. In the case an optional unit is not installed, Q1078 is made ON and the signal goes through Q1078.

The signal then goes through de-emphasis part and expander Q1023. When the function of expander is off, the signal will be bypassed by Q1016.

The output signal of expander (or a signal from de-emphasis) goes through AF mute switch Q1078 and amplified by Q1077.

The signal goes to Q1030, when the audio equalizer is off. In the case the audio equalizer is on, the signal from Q1077 goes to the buffer amplifier Q1077 for audio equalizer Q1083, Q1025 and Q1029. And then the signal goes to Q1030.

The output from Q1030 is amplified with AF power amplifier Q1015 after passing AF volume Q1020.

The output of Q1015 drives a speaker (it chooses the external SP or internal SP in external terminal, SELECT)

#### 2-5. Squelch Circuit

There are 13 levels of squelch setting from 0 to 12. The level 0 means open the squelch. The level 1 means the threshold setting level and level 11 means tight squelch.

From 2 to 10 is established in the middle of threshold and tight. The bigger figure is nearer the tight setting.

The level 12 becomes setting of carrier squelch.

### **2-5-1. Noise Squelch**

Noise squelch circuit is composed of the band path filter of Q1067, noise amplifier Q1071, and noise detector D1047, D1048.

When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1067 is amplified in Q1071 through the band path filter Q1067, is detected to DC voltage with D1047, D1048 and is inputted to 16pin (the A/D port) of the Q1069 (CPU).

When a carrier is received, the DC voltage becomes low because the noise is compressed.

When the detected voltage to CPU is high, the CPU stops AF output with Q1078 "OFF" by making the 59pin (CPU) "L" level.

When the detection voltage is low, the CPU makes Q1078 ON with making 59pin "H" and the AF signal is output.

### **2-5-2. Carrier Squelch**

The CPU (15pin: A/D port) detect RSSI voltage output from Q1067 12 pin, and controls AF output.

The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage.

The process of the AF signal control is same as Noise Squelch

The shipping data is adjusted 3dB higher than squelch tight sensitivity.

## **3. Transmitter System**

### **3-1. Mic Amplifier**

The AF signal from internal microphone J1001 4pin or external microphone J1001 19pin is amplified with microphone amplifier Q1076, after microphone selection switch Q1001, and passes microphone gain volume Q1020.

The AF signal which was controlled in the correct gain passes compressor Q1023. When not using a compressor, with the control from the CPU, it passes in the compressor circuit inside of Q1023 and it is output and it passes a pre-emphasis circuit.

Q1078 becomes OFF when an option unit is attached and the AF signal from Q1023 goes via the option unit. When an option unit isn't attached, Q1078 becomes ON, the signal passes Q1078 and is input to the pre-emphasis amplifier Q1032.

The signal passed limiter and splatter filter of Q1032 is adjusted by maximum deviation adjustment volume Q1020.

The adjusted low frequency signal ingredient is amplified by Q1075, added modulation terminal of TCXO (X1003), the FM modulation is made by reference oscillator.

The high frequency signal ingredient is amplified Q1075, and adjusted the level by volume Q1020 to make frequency balance between low frequency. After that, it is made FM modulation to transmit carrier by the modulator D1027 of VCO.

### **3-2. Noise canceling microphone**

The two signals from internal microphones (main and sub) are input to the positive input (sub) and to the negative input (main) and of the Q1076. If the same signal is input to both main and sub, the main signal is canceled at the output of Pin7 of the Q1076. In other words, noise from nearby sources not directly connected to the transceiver enters the main and sub input at the same signal and is therefore canceled out.

When a signal is only input to main and there is no signal at sub, the main signal is output as is from Q1076.

### **3-3. Drive and Final amplifier**

The modulated signal from the VCO Q1052 is buffered by Q1042 and amplified by Q1033. Then the signal is buffered by Q1027 for the final amplifier driver Q1021. The low-level transmit signal is then applied to Q1010 for final amplification up to 5watts-output power.

The transmit signal then passes through the antenna switch D1012 and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

### **3-4. Automatic Transmit Power Control**

The current detector Q1072 detects the current of Q1010 and Q1021, and converts the current difference to the voltage difference.

The output from the current detector Q1072 is compared with the reference voltage and

amplified by the power control amplifier Q1072.

The output from Q1072 controls the gate bias of the final amplifiers Q1010 and the final amplifier driver Q1021.

The reference voltage changes into four values (TX Power High, Low3, Low2 and Low1) controlled by Q1020.

### **3-5. PLL Frequency Synthesizer**

The frequency synthesizer consists of PLL IC, Q1070, VCO, TCXO (X1003) and buffer amplifier.

The output frequency from TCXO is 16.8MHz and the tolerance is  $\pm 2.5$  ppm (in the temperature range -30 to +60 °C).

#### **3-5-1. VCO**

While the radio is receiving, the RX oscillator Q1047 in VCO generates a programmed frequency between 399.15 and 461.15MHz as 1st local signal.

While the radio is transmitting, the TX oscillator Q1052 in VCO generates a frequency between 450 and 512MHz.

The output from oscillator is amplified by buffer amplifier Q1042 and becomes output of VCO. The output from VCO is divided, one is amplified by Q1051 and feed back to the PLL IC 5pin. The other is amplified in Q1033 and in case of the reception, it is put into the mixer as the 1st local signal through D1020, in transmission, it is buffered Q1027, and more amplified in Q1021 through D1020 and it is put into the final amplifier Q1010.

#### **3-5-2. VCV CNTL**

Tuning voltage (VCV) of VCO is expanding the lock range of VCO by controlling the anode of varactor-diode at the negative voltage and the control voltage from PLL IC.

The negative voltage is added to the varactor-diode after converted to negative by Q1031, which is output voltage of D/A converter Q1020.

#### **3-5-3. PLL**

The PLL IC consists of reference divider, main divider, phase detector, charge pumps and fractional accumulator. The reference frequency from TCXO is inputted to 8pin of PLL IC and is divided by reference divider. This IC is decimal point dividing PLL IC and the dividing ratio becomes 1/8 of usual PLL frequency step. Therefore, the output of reference divider is 8 times of frequencies of the channel step. For example, when the channel stepping is 5 kHz, the output of reference divider becomes 40 kHz.

The other hand, inputted feed back signal to 5 pin of PLL IC from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated.

The phase difference pulse and the pulse from fractional accumulator pass through the charge pumps and LPF. It becomes the DC voltage (VCV) to control the VCO.

The oscillation frequency of VCO is locked by the control of this DC voltage.

The PLL serial data from CPU is sent with three lines of SDO (20pin), SCK (22pin) and PSTB (27pin).

The lock condition of PLL is output from the UL (18Pin) terminal and UL becomes "H" at the time of the lock condition and becomes "L" at the time of the unlocked condition. The CPU always watches over the UL condition, and when it becomes "L" unlocked condition, the CPU prohibits transmitting and receiving.