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|---|---|---|
| Wireless Data Communications | **BUSINESS GROUP:** | Hardware |
| | **DOCUMENT #:** | 5720-0090-0B-SA |
| | **VERSION #:** | 0 |
| | **DATE:** | Oct 17,2002 |

# *BWS 5000*
# *REV.0A*
# *HARDWARE FUNCTIONAL DESCRIPTION*

## APPROVALS:

| POSITION | NAME | SIGNATURE | DATE |
|---|---|---|---|
| **Originator 1** | Steve Jang | | |
| **Originator 2** | Chad Gilbertson | | |
| **Project Manager** | Rashed Hayder | | |
| **System Architect** | Shane Rogers | | |
| **Software** | Brian Geichen | | |
| **Advance Technology** | Shawn Taylor | | |
| | | | |
| | | | |

Classification:

**RELEASE:**

# MODIFICATION RECORD:

| VERSION | NAME | REASON | DATE |
|---|---|---|---|
| 0A | Chad Gilbertson<br>Steve Jang | Started from BWS 3000 S-BOX 0B<br>- updated RF section with Radia chipset<br>- remove section on AP Full Duplex<br>- updated power control and monitoring<br>- updated RF calibration attenuator<br>- updated RF control<br>- updated power supply (voltage rail adjust)<br>- updated introduction, two board from three<br>- updated RS-232 | Feb 14,2003 |
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# 1 Scope

1.1.1 The Hardware Functional Description document provide details on how the BWS 5000 operates at a functional level.

# 2 Introduction

2.1.1 The BWS 5000 system is a wireless communication network designed for providing broadband internet access to users. Libra allow users to communicate to the base station (AP). The Libra is the CPE (customer premise equipment).

2.1.2 Libra is a single unit,cost reduced solution to replace the IDU and ODU CPE. It uses the same chassis as the ODU CPE and utilizes the integrated antenna. Libra is designed for outdoor use.

2.1.3 Libra consists of two boards.

1). Digital Engine Board

a). Receives user data from RJ-45 processes data using Wi-Lan's proprietary W-OFDM scheme and sends digital baseband data to the RF board for modulation and transmission.

b). Receives digital baseband data from the RF board and extracts user data, which is sent to the RJ-45.

2). RF Board

a). Converts transmit data from the Digital Engine Board to analog baseband for modulation at IF. Modulated IF signal is shifted to RF and transmited.

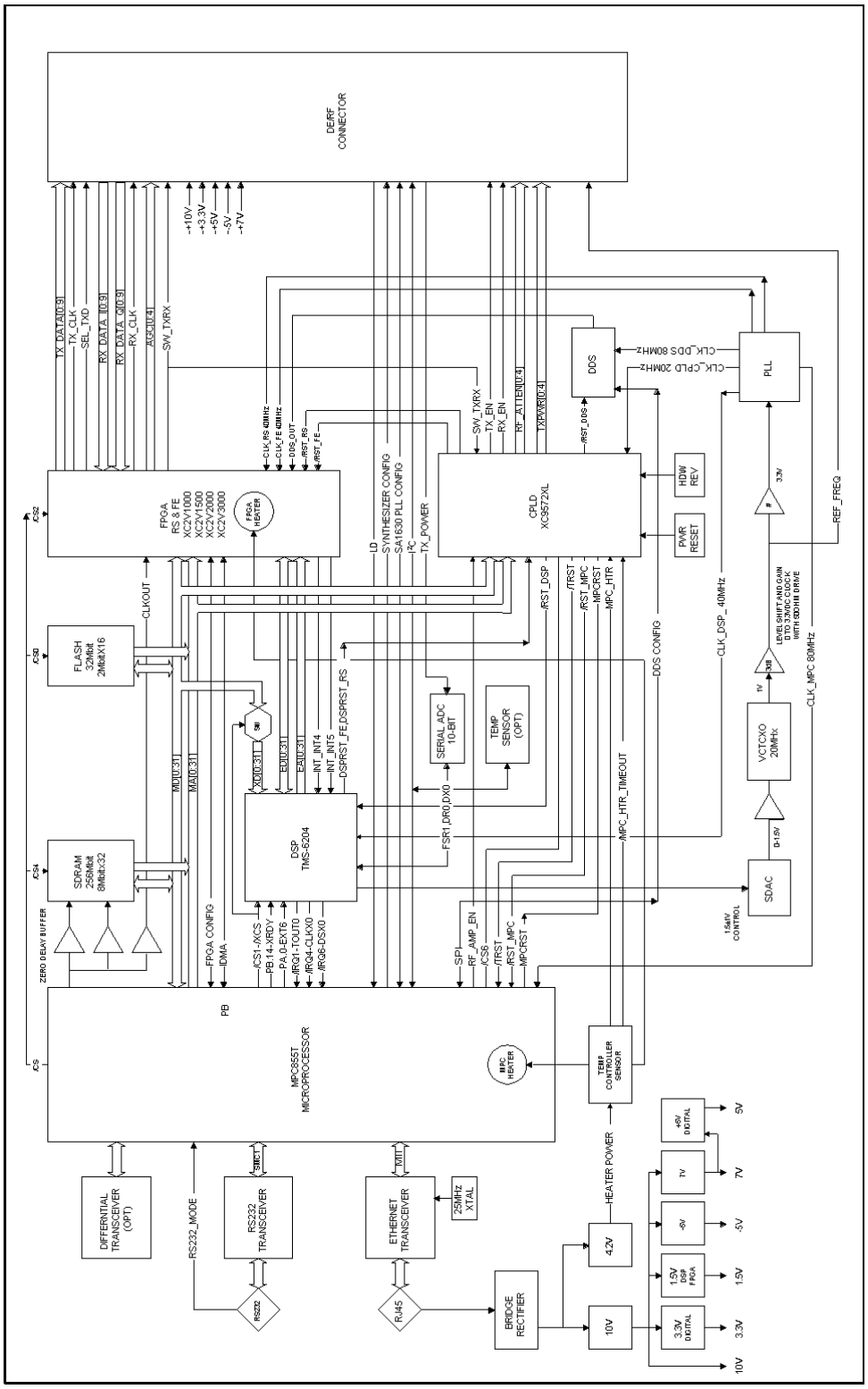
b). Receives RF signal and shifts signal to IF. IF signal is demodulated to obtain analog baseband, which is converted to digital data to be sent to the Digital Engine Board for unpacking.

# 3 Digital Engine Board

## 3.1 Scope

3.1.1 This section provides the principles of operation for the DE Board.

3.1.2 In this section, reference is made to the block diagram.


DE4F CONNECTOR
FPGA RS & FE XC2V1000 XC2V1500 XC2V2000 XC2V3000
CPLD XC95724L
DDS
PLL
FLASH 32Mbit 2Mbitx16
SDRAM 256Mbit 8Mbitx32
DSP TMS-6204
MPC855T MICROPROCESSOR
SERIAL_ADC 10-BIT
TEMP SENSOR (OPT)
VCTCXO 20MHz
SDAC
DIFFERNTIAL TRANSCEIVER (OPT)
RS232 TRANSCEIVER
ETHERNET TRANSCEIVER
25MHz XTAL
BRIDGE RECTIFIER
TEMP CONTROLLER SENSOR
HEATER POWER
4.2V
10V
HDW REV
PWR RESET
DDS CONFIG
CLK_DSP_40MHz
CLK_MPC 80MHz
REF_FREQ
ZERO DELAY BUFFER
FPGA CONFIG
IDMA
PB
SPI
RF_AMP_EN
/CS6
/TRST
/RST_MPC
MPCRST
MPC_HTR
MPC_HTR_TIMEOUT
/RST_DSP
RS232_MODE
SYNTHESIZER CONFIG
SA1630 PLL CONFIG
TX_POWER
SW_TXRX
TX_EN
RX_EN
RF_ATTEN[0:4]
TXPWR[0:4]
CLK_DDS 80MHz
CLK_CPLD 20MHz
CLKOUT
MD[0:31]
MA[0:31]
XD[0:31]
ED[0:31]
EA[0:31]
INT_INT4
INT_INT5
DSPRST_FE,DSPRST_RS
FSR1,DR0,DX0
PA,0-EXT6
IRQ1-TOUT0
IRQ4-CLKX0
IRQ6-DSX0
/CS1-/ACS
PB14-XRDY
FPGA HEATER
MPC HEATER
+10V
+3.3V
+5V
-5V
+7V
+5V DIGITAL
7V
-5V
1.5V DSP FPGA
3.3V DIGITAL
5V
1.5V
3.3V
10V
LEVEL SHIFT AND GAIN D TO 3.3VDC CLOCK WITH 50OHM DRIVE
15dBV CONTROL
0-15V
33V
1V

3.2 Power Supply

3.2.1 Power supply input is rated 28VDC @ 1.5A under full load.

3.2.2 Power is supplied through the RJ-45 Ethernet connector.

1). Pins 4 and 5 28VDC
2). Pins 7 and 8 Ground

3.2.3 The 28VDC is pre-regulated down to 15VDC by a 3A switching regulator where it feeds multiple switching regulators

1). 3.3V Digital I/O and MPC Core
2). 5V Digital
3). 1.5V FPGA and DSP Core
4). –5V Analog
5). +7V Analog (Regulated to +5V by LDO post regulators)

3.2.4 The 15V supply is also used for the power amplifiers on the RF board

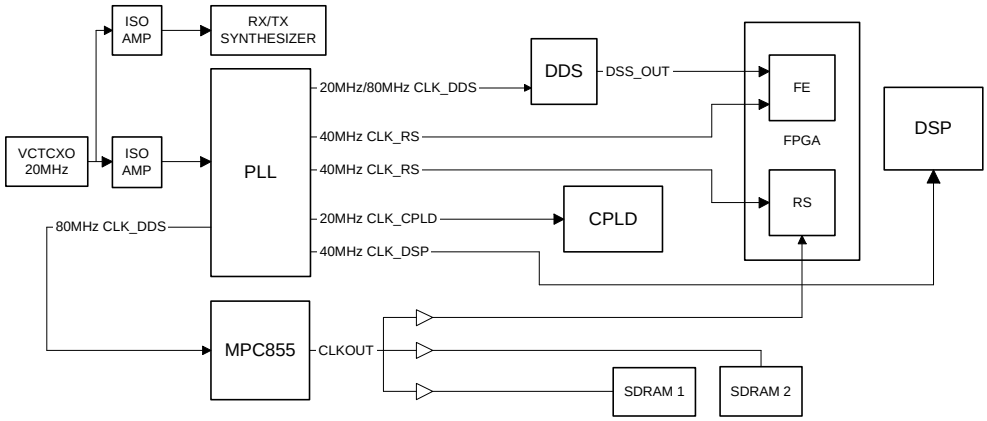
3.2.5 The 28VDC is regulated down to 4.4V by a 3A switching regulator to supply power for the MPC and FPGA heaters.

3.3 Clocks

3.3.1 A 20MHz VCTCXO is the main clock source for LIBRA. The 20MHz clock is split into two signals with isolation amplifiers. One clock is fed to the RF board and other to the PLL. The isolation prevents digital switching noise from entering the RF and high frequency from entering the digital circuit. On the RF board, the 20MHz clock is used as a source for the receive and transmit synthesizer. The PLL provides 80MHz clocks for the MPC and 20/80MHz for the DDS. It also generates 40MHz clocks for the FPGA (RS and FE) and 20MHz for the CPLD.

3.3.2 The VCTCXO frequency is centered on 20MHz and is adjustable ±10ppm by the AFC function in the DSP. The AFC adjusts the VCTCXO frequency such that error in the receive data from the access point is minimized.

3.3.3 The MPC bus runs at 40MHz, half the 80MHz input clock. The 40MHz clock from the MPC is provided on the signal CLKOUT which is used to drive the SDRAM and RS. The CLKOUT signal is buffered with a zero delay buffer for each device.

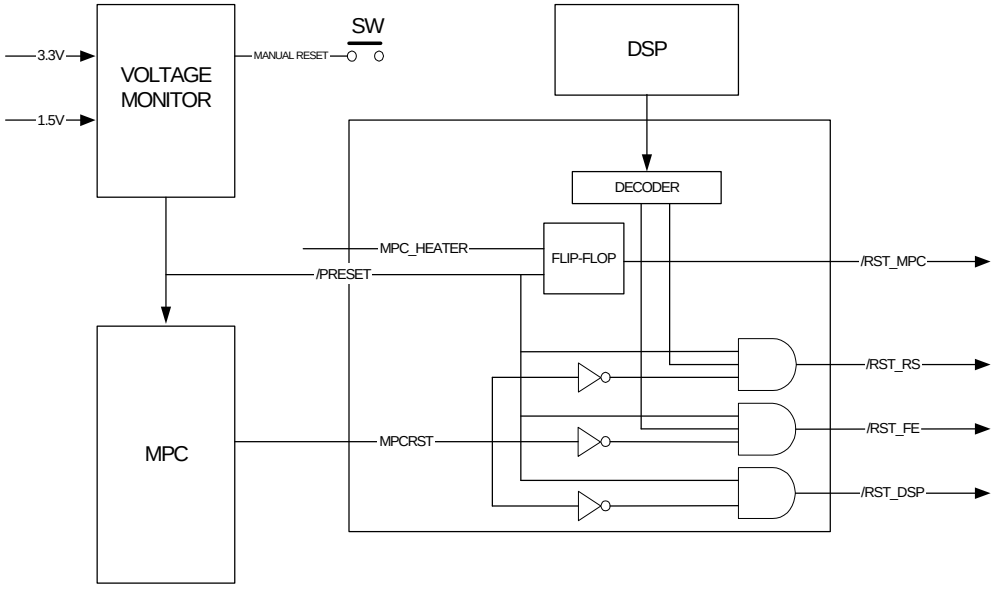



3.4 Reset and Power Management

3.4.1 Power up reset is controlled by a voltage monitoring supervisor, which hold all devices at reset until the 3.3V I/O and 1.5V core supplies are up. If the voltage levels were to fall below a threshold value of 88%, the voltage monitoring supervisor will reset the devices. These devices include MPC, DSP and FPGA (RS and FE) .

3.4.2 After power-up reset has been completed, the MPC boots-up and holds the DSP and FPGA (RS and FE) in reset state through signal MPCRST via the CPLD. Reset signals for DSP, FE, RS and IF are provided by the CPLD. After the MPC loads the FPGA, it releases the MPCRST signal, which releases the DSP and IF. The MPC loads the DSP image through the host port interface. The DSP boots-up and holds the FE and RS in reset state until it is fully initialized. The FE and RS are released from reset.

3.4.3 If the CPLD detects the thermostat calling for heat on the MPC during power reset, the CPLD holds the MPC in reset state for 3 minutes or until the thermostat reaches setpoint. At this point, the MPC case temperature is within spec at which it is allowed to boot-up. If the thermostat calls for heat on the MPC after power reset, the MPC continue to run but the MPC heater turns on.




3.5 Thermal Management

3.5.1 The MPC855T and FPGA devices are rated with minimum operating temperature of 5°C. A temperature controller/sensor placed near the MPC device controls separate IC heaters for the MPC and FPGA. Heaters is Minco type HK5583, 0.012" thick pad heater with self-adhesive backing to be applied to the device. Approximately 4 watts of heat will be applied to each device. Each heater is connected to the board with a 2-pin header.

3.5.2 A temperature sensor is connected to the MPC $I^2C$ bus to allow the MPC to monitor the ambient temperature inside the enclosure. This will allow the MPC to reduce through-put or shutdown at high temperatures to reduce heat dissipation.

3.6 MPC855 Microprocessor

3.6.1 MPC855

The MPC855 Power QUICC is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. The MPC855 PowerQUICC integrates two processing blocks. One block is the Embedded PowerPC Core and the second block is a Communication Processor Module (CPM). The CPM supports 10/100BASE Ethernet. The processor has a large number of I/O pins which can be used as user I/Os, serial ports, $I^2C$ bus, SPI (serial peripheral interface), interrupts and DMA.

3.6.2 Functional Description

1). Interfaces to flash memory (16-bit data bus), SDRAM and SRAM (both 32-bit data bus)
2). Interfaces to DSP XBUS to communicate with DSP
3). CPM interfaces to Ethernet Transceiver (MAC)
4). Reed Solomon Interface
    a). IDMA interface for sending and receiving data
    *b). Optional memory interface (RD/nWR, /MOE, WE)*
5). RS-232 terminal interface to provide menu driven user interface for Libra configuration and monitoring.
6). Configures RF Synthesizer and SA1630PLL during startup.
7). Detects RF Synthesizer lockout
*8). Enables transmit and receive RF amplifiers after successful configuration of RF and IF PLL Synthesizer, preset RF transmit power and lock detect..*
*9). Read temperature enclosure air temperature from temperature sensor.*
*10). Load program image into FPGA*
11). Releases DSP and FPGA after boot-up.

3.6.3 I/O Pin Assignment

| Signal | Size | Description | Type | Location |
|---|---|---|---|---|
| EXT_Int6 | 1 | DSP Interrupt Input | Output | PA0 |
| FPGA_DIN | 1 | FPGA Program Data in | Output | PA1 |
| FPGA_CLK | 1 | FPGA Program Clk | Output | PA2 |
| FPGA_DONE | 1 | FPGA Program Done | Input | PA3 |
| /DRQ1_MPC | 1 | MPC RS | Output | PA4 |
| TX_SYNC_IN | 1 | AP Duplex – Receive | Input | PA5 |
| TX_SYNC_OUT | 1 | AP Duplex - Transmit | Output | PA6 |
| FPGA_PROG | 1 | FPGA Program Prog | Output | PA7 |
| LED_Fail | 1 | LED On if MPC Fail | Output | PA8 |
| LED_OK | 1 | Flashing LED - MPC OK | Output | PA9 |
| *FPGA_INI* | *1* | *FPGA Program Initialize* | *Input* | *PA10* |
| SYNENR | 1 | RF Receive Synthesizer Enable | Output | PA11 |
| SYNDAT | 1 | RF Synthesizer Data | Output | PA12 |
| TX_SYNC_DRV | 1 | AP duplex - Transceiver Mode | Output | PA13 |
| SYNCLK | 1 | RF Synthesizer Clk | Output | PA14 |
| SYNENT | 1 | RF Transmit Synthesizer Enable | Output | PA15 |
| XRDY | 1 | DSP Expansion Port Ready | Input | PB14 |
| /M_TRSTE | 1 | Ethernet Tranceiver Rx High Impedance | Output | PB15 |
| /M_RESET | 1 | Ethernet Tranceiver Reset | Output | PB16 |
| RF_AMP_EN | 1 | Enable RF RX/TX Amp | Output | PB17 |
| VPEN | 1 | Flash VPEN Write Protect | Output | PB18 |
| CKE | 1 | SDRAM Clock Enable | Output | PB19 |
| MPCRST | 1 | MPC Reset Signal to Peripheral | Output | PB20 |
| PLL_STRB | 1 | IF PLL Strobe | Output | PB21 |
| PLL_DATA | 1 | IF PLL Data | Output | PB22 |

| | | | | |
|---|---|---|---|---|
| PLL_CLK | 1 | IF PLL Clock | Output | PB23 |
| RX | 1 | RS-232 Rx | Input | PB24 |
| TX | 1 | RS-232 Tx | Output | PB25 |
| CSCL | 1 | $I^2C$ Clock | Output | PB26 |
| CSDA | 1 | $I^2C$ Data | I/O | PB27 |
| MISO | 1 | SPI Serial Output | Output | PB28 |
| MOSI | 1 | SPI Serial Input | Input | PB29 |
| SPICK | 1 | SPI Clock | Output | PB30 |
| DDS_FQ_UP | 1 | High-Speed DDS Data Store | Output | PB31 |
| /RF_MEM_WP | 1 | RF Board $E^2$PROM Write Protect | Output | PC4 |
| /SDACK1 | 1 | MPC RS | Output | PC5 |
| LD | 1 | RF Synthesizer Lock Detect | Input | PC6 |
| /SDACK2 | 1 | MPC RS | Output | PC7 |
| ANT_A_B | 1 | Antenna Select | Input | PC8 |
| DDS_FSYNC | 1 | DDS Data Configuration Enable | Output | PC9 |
| SW_TXRX | 1 | Communication Mode | Input | PC10 |
| CAL_EN | 1 | Enable Calibration of IRC1332 | I/O | PC11 |
| TP | 1 | Test Point | I/O | PC12 |
| TP | 1 | Test Point | I/O | PC13 |
| /DREQ1 | 1 | MPC RS | Output | PC14 |
| /DREQ0 | 1 | MPC RS | Input | PC15 |
| | | | | |

### 3.6.4 Interrupt Assignment

| IRQx | Signal | Device | Description |
|---|---|---|---|
| 0 | /IRQ0 | | Not Used |
| 1 | /IRQ1 | DSP | IRQ request from XBUS |
| 2 | /IRQ2 | RS | RS Encoder IDMA |
| 3 | /IRQ3 | RS | RD Decoder IDMA |
| 4 | /IRQ4 | DSP | IRQ request from DSP CLKR0 |
| *5* | /IRQ5 | *AP Full Duplex* | AP Full Duplex – TX_SYNC_IN |
| 6 | /IRQ6 | DSP | IRQ request from DSP RSX0 |

### 3.6.5 Memory Map

| CSx | Signal | Device | Address | Size | Width | Description |
|---|---|---|---|---|---|---|
| 0 | /CS0 | Flash | FC000000-FC7FFFFF | 8Mbyte | 16 bit | |
| 1 | /CS1 | Bus Sw | 100000000-10007FFFF | 4 byte | 32 bit | Bus Switch between XBUS DSP/Data Bus MPC |
| 2 | /CS2 | RS | 20000000 | 4 byte | 32 bit | RS Buffer |
| 3 | /CS3 | | | | | Not Used |

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | /CS4 | SDRAM | FE000000-FFFFFFFF | 32Mbyte | 32 bit | Not Used |
| 5 | /CS5 | | | | | Select SRAM |
| *6* | */CS6* | *CPLD* | *00080000 0008000F-* | *16 byte* | *8 bit* | *Address Expansion* |
| 7 | /CS7 | | | | | Not Used |

3.6.6 Hardware Reset Configuration

1). The hard reset configuration word is sampled from the data bus. These bits determine the default values of the corresponding bits in the SIUMCR, IMMR, and MSR

.

| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Field | EARB | IIP | - | | BPS | | - | ISB | | DBGC | | DBPC | | EBDF | | - |
| Default | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

**Hard Reset Configuration Word**

**Hard Reset Configuration Word Field Description**

| Bits | Name | Value | Description |
|---|---|---|---|
| 0 | EARB | 0 | External arbitration. Defines the initial value for ACR[EARB].<br>0: Internal arbitration is performed. |
| 1 | IIP | 1 | Initial interrupt prefix. Defines the initial value of the MSR[IP] which defines the interrupt table location. If IIP is cleared (default), the MSR[IP] initial value is one;<br>If it is set to one, the MSR[IP] initial value is zero. |
| 2-3 | - | 0 | Reserved for future use and should be allowed to float. |
| 4-5 | BPS | 10 | Boot port size. Defines the port size of the boot device.<br>00: 32-bit port size<br>01: 8-bit port size<br>10: 16-bit port size<br>11: Reserved |
| 6 | - | 0 | Reserved for future use and should be allowed to float. |
| 7-8 | ISB | 01 | Initial internal space base select. Defines the initial value of the IMMR bits 0-15 and determines the base address of the internal memory space.<br>00 0x00000000<br>01 0x00F00000<br>10 0xFF000000<br>11 0xFFF00000 |
| 9-10 | DBGC | 11 | Debug pin configuration. Configures the operation of the following signals:<br>11 IP_B[0-1]/IWP[0-1]/VFLS[0-1] functions as VFLS[0-1]<br>IP_B3/IWP2/VF2 functions as VF2<br>IP_B4/LWP0/VF0 functions as VF0 |

| Bits | Name | Value | Description |
|---|---|---|---|
| | | | IP_B5/LWP1/VF1 functions as VF1<br>OP2/MODCK1//STS functions as /STS<br>ALE_B/DSCK/AT1 functions as AT1<br>IP_B2/AT2 functions as AT2<br>IP_B6/DSD1/AT0 functions as AT0<br>IP_B7//PTR/AT3 functions as AT3<br>OP3/MODCK2/DSDO functions as OP3 |
| 11-12 | DBPC | 00 | Debug port pins configuration. Determines the active pins for the development port.<br>00 ALE_B/DSCK/AT1, IP_B6/DSDI/AT0, OP3/MODCK2/DSDO and IP_B7//PTR/AT3 function as defined by DBGC<br>TCK/DSCK functions as DSCK<br>TDI/DSDI functions as DSDI<br>TDO/DSDO functions as DSDO<br>01 ALE_B/DSCK/AT1, IP_B6/DSDI/AT0, OP3/MODCK2/DSDO, and IP_B7//PTR/AT3 function as defined by DBGC<br>TCK/DSCK functions as TCK<br>TDI/DSDI functions as TDI<br>TDO/DSDO functions as TDO |
| 13-14 | EBDF | 01 | External bus division factor. Defines the frequency division factor between GCLK1/GCLK2 and GCLK1_50/GCLK2_50. CLKOUT is similar to GCLK2_50 and GCLK1_50 are use by the system inerface unit and memory controller to interface with the external system.<br>00 Full speed bus<br>01 Half speed bus<br>10 Reserved<br>11 Reserved |
| 15 | - | 0 | Reserved for future use and should be allowed to float. |

3.6.7 Memory

1). SDRAM

a). The 256Mbit of SDRAM configured as 8Mbit x 32bits is used for program execution and data storage. SDRAM clock is generated by CLKOUT signal from the MPC, which is buffered by a zero delay buffer. To minimize buffer delays, user programmable machine B (UPMB) is used implement the MPC interface to the SDRAM. To optimize on cost, two 2Mbit x 16 bits x 4 bank SDRAM ICs will be used to implement the 256Mbit of memory.

b). Micron MT48LC8M16A2 or equivalent

c). Signal CKE, MPC PB19 is assigned as clock enable

2). Flash

a). 32Mbit of flash memory upgradeable to 64 configured as 2Mbit x 16 bits is used for mass storage. This includes program images for MPC, DSP and FPGA.
*b).* Intel type E28F320J3A or equivalent, 56-pin.
*c).* Signal VPEN, MPC PB18 is used for write protection.

3.7 RS-232 Interface

3.7.1 An RS-232 interface connects to a terminal port to provide a menu driven user interface for Libra configuration and monitoring.

3.7.2 SMC 1 on the MPC is connected to a RS-232 transceiver to provide a RS-232 port.

3.7.3 The RS-232 port connector has 5-pins.

1). Transmit
2). Receive
3). Ground
4). SED

3.7.4 Only transmit, receive and ground are required for a terminal interface.

3.8 FPGA Programming

3.8.1 MPC loads FPGA image from flash during startup.

3.8.2 The following signals are required to load the FPGA

1). FPGA_DIN PA1
2). FPGA_CLK PA2
3). FPGA_DONE PA3
4). FPGA_PROG PA7
5). FPGA_INI PA10

3.9 RF Power Control and Monitoring

3.9.1 RF output power must be consistent with specifications to meet EDSI requirements.

3.9.2 Transmit power is user settable in the radio configuration up to a maximum of 17dBm.

3.9.3 Transmit power is controlled by transmit power attenuator. Signals to this attenuator are TXPWR[0:4], 5-bit binary controlled by the MPC.

3.9.4 Power Monitoring

1). Transmit power control is done by a close loop feedback control scheme. To perform feedback control, the actual transmit power is measured by a power detector in the RF circuit.
2). The sinusoidal output signal is converted to a DC voltage using a precision rectifier circuit is minimal filtering. This signal TX_POWER is fed to a serial 10-bit ADC which is controlled by the DSP.
3). To achieve consistent power measurements for each superframe, the data must be consistent. Since training symbols are always consistent the output signal is measured only when training symbols are being transmitted. The DSP will only sample the ADC during transmission of training symbols.

4). Width of PWR_MEASURE signal would correspond with duration of training symbols which are as follows
   a). 10MHz bandwidth 27µS x 5 = 135µS
   b). 5MHz bandwidth 54µS x 5 = 270µS
   c). 3MHz bandwidth (128FFT) 49µS x 5 = 245µS
5). Sampling capability of the 10-bit ADC is 500KSPS or 2µS per sample
6). The DSP communicates to the ADC via SPI interface.
7). The DSP sends the power measurements to the MPC.
8). The MPC averages the power measurements and adjust the TXPWR attenuator until transmit power is consistent with the user setting.

3.10 RF $E^2$PROM Write Protect

3.10.1 A write protect signal, /RF_MEM_WP protects the $E^2$PROM from accidental erasure.

3.11 RF Synthesizer Configuration

3.11.1 During power-up, the MPC writes configuration data to the frequency synthesizer on the RF board

3.11.2 Signals required for SYNTHESIZER_CONFIG are:

1). SYNENT: Enable transmit synthesizer
2). SYNENR: Enable receive synthesizer
3). SYNDAT: Synthesizer configuration data
4). SYNCLK: Clock for sending Synthesizer configuration data

3.12 Modulator/Demodulator PLL Configuration

3.12.1 During power-up, the MPC writes PLL configuration data to the SA1630 modulator/demodulator

3.12.2 Signals required for SA1630_PLL_CONFIG are:

1). PLL_STRB
2). PLL_DATA
3). PLL_CLK

3.13 RF Calibration Attenuator

3.13.1 The RF calibration attenuator adjust the attenuation on both the transmit and receive chain for different frequencies due to non-linearity.

3.13.2 Since the system is half duplex, only one calibration attenuator is required by placing it in the common TX/RX path.

3.13.3 During board calibration, each receive and transmit channel must be calibrated for each channel so that output power is consistent with the same input by adjustment to the RF calibration attenuator. The transmit and receive attenuator values for each channel are stored in flash memory.

3.13.4 During each system transition from receive to transmit mode, the RF calibration attenuator must be set with the transmit attenuator setting. Also, during each system transition from transmit to receive mode, the RF calibration attenuator must be set with the receive attenuator setting. Because the transition is so quick, the RF calibration attenuator setting is controlled by the CPLD.

3.13.5 During startup, the MPC loads the RF calibration attenuator settings into two registers in the CPLD, one for receive and other for transmit. The CPLD sets the

attenuator control signals from the registers depending on transmit or receive mode.

3.14 RF Control

3.14.1 LD (Lockout Detect)

1). This signal is active when the RF Synthesizer detects a lockout condition.

3.14.2 RF_AMP_EN

1). RF_AMP_EN enables transmit and receive power amplifiers on the RF board. It is active once the MPC has set the RF attenuator (RF_ATTEN[0:4], transmit power (TXPWR[0:4] and the RF Synthesizer is not in lockout condition. It is disabled if lockout is detected.

3.14.3 TX_EN

1). TX_EN enables the transmit amplifier if system is in transmit mode, RF_AMP_EN and lock detect is active.

3.14.4 RX_EN

1). RX_EN enables the receive amplifier if system is in receive mode, RF_AMP_EN and lock detect is active. RX_EN is delayed by 3µS after system goes into receive mode.

3.14.5 ANT_A_B_SW (Antenna Select)

1). The ANT_A_B_SW signal allows the MPC to select one of two antennas for the future Vine capability. The signal originates from the MPC as ANT_A_B. ANT_A_B_SW is a synchronized version of ANT_A_B with SW_RXTX.

a). If ANT_A_B goes high, ANT_A_B SW goes high during the next SW_RXTX low to high transition.

b). If ANT_A_B goes low, ANT_A_B SW goes low during the next SW_RXTX high to low transition.

3.15 $I^2C$

3.15.1 The $I^2C$ interface communicates with the RF $E^2$PROM and temperature sensor.

3.15.2 RF Board Calibration Memory

1). Serial $E^2$PROM
2). Address: 1

3.15.3 Temperature Sensor

1). DE Board: Address 3
2). RF Board: Address 0

3.16 Ethernet Transceiver

3.16.1 Ethernet signals come into Libra through the 8-pin DIN connector and goes through an Ethernet isolation transformer. The secondary of the transformer interfaces to the Ethernet transceiver. The Ethernet transceiver supports a MAC interface for 10/100Base-TX operation and interfaces to the MAC module of the MPC855 via the MII interface. The two signal serial management signals are interfaced to the parallel general-purpose I/O port (Port C) of the MPC855 processor.

3.16.2 The Ethernet transceiver will be operating in half duplex mode.

3.16.3 LED Status indicators will be provided on the PCB for the following:

1). Transmit
2). Receive
3). Link
4). Duplex
5). Collision
6). Speed

3.17 CPLD

3.17.1 Xilinx XC9575XL
The CPLD used is a Xilinx XC9575XL with 75 macrocells, 1600 gates and 72 user I/O pins. The CPLD provide discrete logic support in a number of areas to eliminate the need for glue logic.

3.17.2 Functional Description

1). MPC I/O Expansion
   a). RF_ATTEN[0:4] Address: 00080000H Bits: MD29-M31
   b). TXPWR[0:4] Address: 00080001H Bits: MD29:MD31
   c). HDW_REV[0:5] Address: 00080002H Bits: MD28:MD31
2). MPC hardware reset configuration
During power up reset, the hardware reset configuration is applied to the MPC data bus where it is read by the MPC. The appropriate logic is applied to the MPC databus by the CPLD.
3). MPC reads CPLD revision from CPLD
4). Resets MPC, DSP, RS, FE and DDS based on MPCRST and power reset signals.
5). Provides logic to set the MPC into JTAG mode via JTAG jumper mode.
6). Provide TX_EN signal for enabling transmit power amplifier and RX_EN signal for enabling receive power amplifier. Transmit power amplifier is enabled when Libra is in transmit mode (SW_TXRX=0), transmit power set, RF synthesizer configured and not in lockout mode. Receive power amplifier is enabled when Libra is in receive mode (SW_TXRX=1), transmit power set, RF synthesizer configured and not in lockout mode.
TX_EN = RF_AMP_EN and /SW_TXRX
RX_EN = RF_AMP_EN and SW_TXRX
7). Read MPC heater status and holds MPC in reset during power up if heater is calling for heat.
8). Provides antenna select signal ANT_A_B_SW. This signal is control by the MPC ANT_A_B but synchronized with SW_RXTX.

3.18 Hardware Revision Identification

3.18.1 The hardware revision of the DE board is encoded by a 6-bit binary code. The bits are set by pull-up and pull-down resistors on 6 inputs on the CPLD. The revision code is read by the MPC and sent to the DSP and FPGA. By knowing the hardware revision, software can determine which functions are supported. The revision is changed when hardware changes on the board affect MPC, DSP or FPGA software.

3.19 MPC/DSP Bus Switch

3.19.1 The MPC 32-bit data bus is connected to the DSP X-Bus via 32-pole bus switch. The bus switch is open during DSP boot-up where it can read the boot configuration on the X-Bus provided by pull-up and pull-down resistors. After boot-up, the bus switch is closed by /CS1 on the MPC.

3.20 Digital Signal Processor

3.20.1 Functional Description

1). Texas Instrument TMS320C6204B, fixed point
2). Modulates error encoded data from the RS and demodulates data from the FE
3). Determines channel estimations
4). Splits data for each sub-carrier
5). DSP is no longer involved in setting DDS frequency to user set bandwidth via CPLD.
6). AFC function interfaces to DAC and adjusts VCTCXO
7). Interfaces to FPGA through 32-bit data bus
8). Interfaces to MPC through expansion bus
9). Operates at 160MHz, 40MHz input x 4
10). DSP is no longer involved in FPGA programming
11). DSP holds RS and FE in reset after boot-up via I/O pins instead of CPLD.
12). Controls RF transmit power

3.20.2 DSP Memory Map

| Address Range (Hex) | Size (byte) | Description (MAP1) |
|---|---|---|
| 0000 0000 - 00FF FFFF | 4M | Internal Program memory |
| 0040 0000 - 013F FFFF<br>[0040 0000 - 0047 FFFF] | 16M<br>512K | External memory interface nCE0 to F.E. FPGA memory |
| 0180 0000 - 019F FFFF | 2M | Internal peripheral registers |
| 01A0 0000 - 01FF FFFF | 6M | Internal peripheral bus reserved |
| 0200 0000 - 02FF FFFF<br>0200 0000 - 0207 FFFF | 16M<br>512K | External memory interface nCE2 to R-S FPGA memory |
| 0300 0000 - 03FF FFFF | 16M | External memory interface nCE3 to VCTCXO |

3.20.3 Pin Assignments

| Pin Name | Net Name | Description |
|---|---|---|
| EA[21..2] | EA[21..2] | Address bus |
| ED[31..0] | ED[31..0] | Data bus |
| /CE0 | /CE0 | Chip select for FE |
| /CE1 | /CE1 | Not Used (Previously Chip select for CPLD) |
| /CE2 | /CE2 | Chip select for RS |
| /CE3 | /CE3 | Not Used (Previously Chip select for CPLD to control AFC |

| Pin Name | Net Name | Description |
|---|---|---|
| | | DAC) |
| /ARE | /ARE | Asynchronous memory read enable for FPGA, CPLD |
| /AOE | /AOE | Asynchronous memory out enable for FPGA, CPLD |
| /AWE | /AWE | Asynchronous memory write enable for FPGA, CPLD |
| DR1 | | Not Used |
| FSR1 | LD14 | LED14 and power measurement ADC enable |
| CLKR1 | | Not Used |
| DX1 | S_DIN | Serial data input for AFC DAC |
| FSX1 | /S_SYNC | Synchronous signal for SED |
| CLKX1 | S_CLK | Clock for SED. |
| DX0 | LD13 | LED13 and power measurement ADC CLK |
| FSX0 | /IRQ6 | /IRQ6 to MPC |
| CLKX0 | /IRQ4 | /IRQ4 MPC |
| CLKR0 | | DSPRST_FE (Resets Front End) |
| FSR0 | | DSPRST_RS (Resets Reed Solomon) |
| CLKS0 | | Not Used |
| DR0 | ADC_Data | Power measurement ADC data |
| EXT_INT4 | EXT_INT4 | External interrupt4 from FE |
| EXT_INT5 | EXT_INT5 | External interrupt5 from RS |
| EXT_INT6 | EXT_INT5 | External interrupt6 from MPC855 |
| EXT_INT7 | EXT_INT7 | External interrupt7 from RS |
| EMU0 | | Emulation pin0 for JTAG |
| EMU1 | | Emulation pin1 for JTAG |
| TCK | dsp_TCK | JTAG clock |
| /TRST | dsp_/TRST | JTAG reset |
| TDO | dsp_TDO | JTAG data out |
| TDI | dsp_TDI | JTAG data input |
| /XCS | /CS1 | Chip select for host interface from MPC855 |
| XCNTL | MA29 | Control signal selects between XBD and XBISA register from MPC855 |
| XW/R | RD/Nwr | Read/Write of expansion bus from MPC855 |
| TOUT0 | /IRQ1 | Interrupt request for host interface to MPC855 |
| XD[31..0] | XD[31..0] | Expansion data bus for interfacing with MPC855 |
| XRDY | XRDY | Ready to receive data from host |

### 3.20.4 Boot Configuration Control via Expansion Bus

**Boot Configuration word**

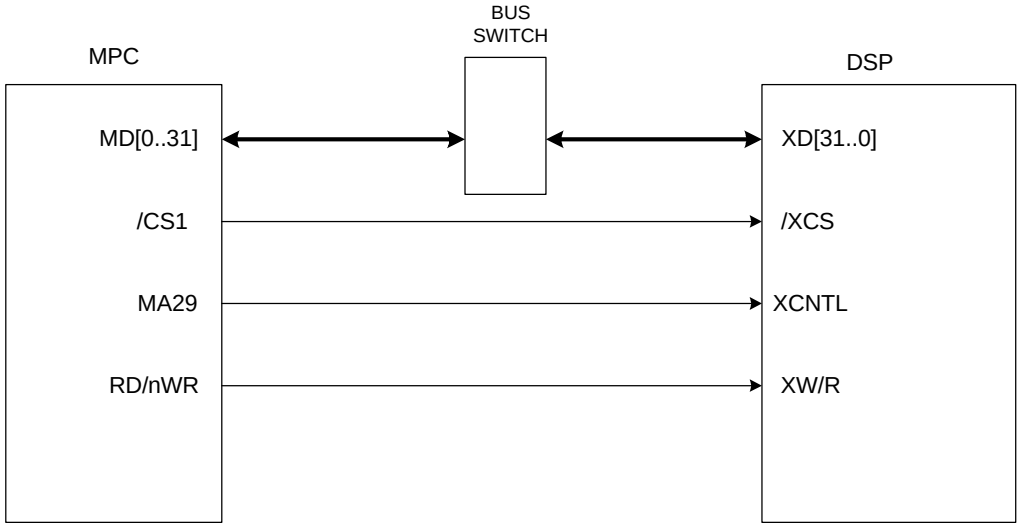
| 31 | 30 | 29 | 28 | 27 | 26 | 24 | 23 | 22 | 20 | 19 | 18 | | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| rsvd | MTYPE XCE3 | | | Rsvd | MTYPE XCE2 | | rsvd | MTYPE XCE1 | | rsvd | MTYPE XCE0 | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | | 0 |
| rsvd | | BLPOL | RWPOL | HMOD | XARB | FMOD | LEND | rsvd | | | BOOTMODE | | |

**Description of Boot Configuration**

| Name | Value | Description |
|---|---|---|
| MTYPE0/1/2/3 | 010 | Memory type<br>010: 32-bit wide asynchronous interface<br>101: 32-bit wide FIFO interface<br>other: reserved |
| BLPOL | 0 | Determines polarity of the XBLAST signal when the DSP is a slave on the expansion bus.<br>0: XBLAST is active low.<br>1: XBLAST is active high. |
| RWPOL | 1 | Determines polarity of expansion bus read/write signal.<br>0: XR/W. Write is active-high.<br>1: XW/R. Read is active-high. |
| HMODE | 0 | Host mode (status in XB HPIC)<br>0: external host interface operates in asynchronous slave mode.<br>1: external host interface is in synchronous master/slave mode. |
| XARB | 0 | Expansion bus arbiter (status in XBGC)<br>0: Internal expansion bus arbiter is disabled<br>1: Internal expansion bus arbiter is enabled |
| FMOD | 0 | FIFO mode (status in XBGC) |
| LEND | 1<br>(JP32) | Little endian mode<br>0: system operates in big endian mode.<br>1: system operrates in little endian mode |
| BOOTMODE[4:0] | 00111 | Dictates the boot-mode of the device, including host port boot, ROM boot, memory map selection.<br>00xxx: Host-port interface<br>01xxx: 8-bit ROM with default timings<br>10xxx: 16-bit ROM with default timings.<br>11xxx: 32-bit ROM with default timings. |

### 3.20.5 Expansion Bus

The expansion bus host port is used to interface the MPC data bus to the DSP in asynchronous mode.




## 3.21 Xilinx XC2V10004FG - FPGA

### 3.21.1 Reed Solomon (RS)

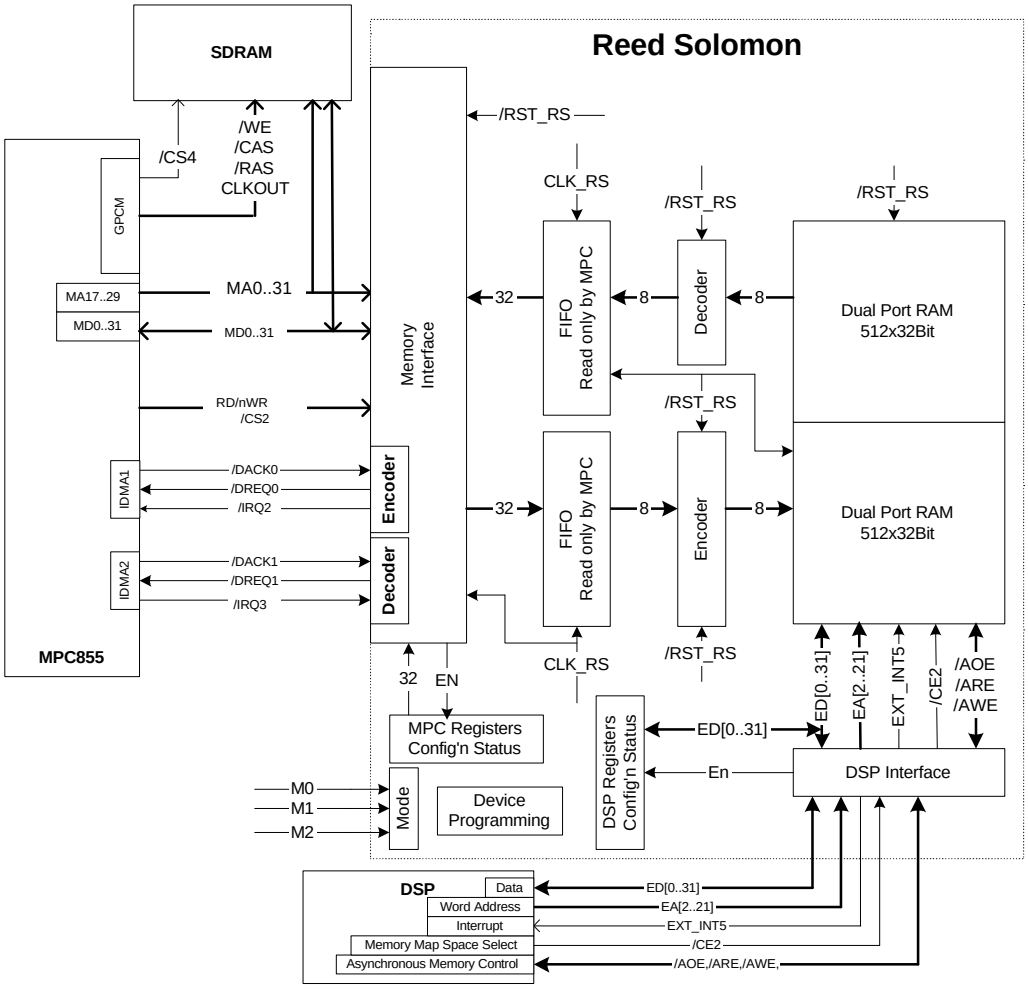
1). Functional Description

*a).* Interfaces to the MPC via IDMA and *optional memory type*

b). Receives transmit data from the MPC and encode error code

c). Receives receive data from DSP and decode error code

d). Transmit and receive data are stored in asynchronous memory




3.21.2 Front End (FE)

1). Functional Description

a). Transmit

FE receives modulated data from the DSP and applies FFT to convert data from frequency to time domain. Generates training symbols and package with data to form superframe in digital baseband.

b). Receive

FE receives digital baseband data from the ADC on the RF board and extracts modulated data. Inverse FFT is applied to the data converting it from time to frequency domain and the data is sent to the DSP for demodulation.

c). Generates transmit and receive clocks from DDS. The output frequency of the DDS is set to the sampling rate set by the MPC.

d). AGC (Automatic Gain Control) function adjusts strength of receive signal through receive IF attenuator on RF board.

2). RF Board ADC and DAC Interface

a). TX_DATA[0:9] Transmit Data 10-bit interleaved I and Q
b). SEL_TXD Transmit I/Q Data Select
c). TX_CLK Transmit Clock
d). RX_D_I[0:9] Receive Data 10-bit I
e). RX_Q_I[0:9] Receive Data 10-bit Q
f). RX_CLK Receive Clock
g). AGC[0:5] AGC (Attenuator control bits)
h). SW_TXRX Transmit or Receive Mode

3). Interfaces to DSP data and address bus asynchronously

3.22 Digital Engine Board/RF Board Interface Connector

3.22.1 This connector interfaces the DE and RF board. The connector is a male 3 x 32, 96-pin DIN 41612, IEC 603-2 industry standard connector.

3.22.2 Connector pinout is as shown in the table below

| Signal | Pin | Description | Type |
|---|---|---|---|
| SW_TXRX | A1 | Tx/Rx Switch | Output |
| PLL_STRB | B1 | SA1630 PLL Strobe | Output |
| PLL_DATA | A2 | SA1630 PLL Data | Output |
| PLL_CLK | B2 | SA1630 PLL Clock | Output |
| TXPWR0 | A3 | IF Tx Attenuator Bit 0 | Output |
| TXPWR1 | B3 | IF Tx Attenuator Bit 1 | Output |
| TXPWR2 | A4 | IF Tx Attenuator Bit 2 | Output |
| TXPWR3 | B4 | IF Tx Attenuator Bit 3 | Output |
| TXPWR4 | A5 | IF Tx Attenuator Bit 4 | Output |
| NC | B5 | No Connection | |
| AGC0 | A6 | IF Rx Attenuator Bit 0 | Output |
| AGC1 | B6 | IF Rx Attenuator Bit 1 | Output |
| AGC2 | A7 | IF Rx Attenuator Bit 2 | Output |
| AGC3 | B7 | IF Rx Attenuator Bit 3 | Output |
| AGC4 | A8 | IF Rx Attenuator Bit 4 | Output |
| AGC5 | B8 | IF Rx Attenuator Bit 5 | Output |
| RX_D_Q0 | A9 | Rx Data I Bit 0 | Input |
| RX_D_Q1 | B9 | Rx Data I Bit 1 | Input |
| RX_D_Q2 | A10 | Rx Data I Bit 2 | Input |
| RX_D_Q3 | B10 | Rx Data I Bit 3 | Input |
| RX_D_Q4 | A11 | Rx Data I Bit 4 | Input |
| RX_D_Q5 | B11 | Rx Data I Bit 5 | Input |
| RX_D_Q6 | A12 | Rx Data I Bit 6 | Input |
| RX_D_Q7 | B12 | Rx Data I Bit 7 | Input |
| RX_D_Q8 | A13 | Rx Data I Bit 8 | Input |

| Signal | Pin | Description | Type |
|---|---|---|---|
| RX_D_Q9 | B13 | Rx Data I Bit 9 | Input |
| RX_CLK | A14 | Rx Data Clock | Output |
| RX_D_I0 | B14 | Rx Data Q Bit 0 | Input |
| RX_D_I1 | A15 | Rx Data Q Bit 1 | Input |
| RX_D_I2 | B15 | Rx Data Q Bit 2 | Input |
| RX_D_I3 | A16 | Rx Data Q Bit 3 | Input |
| RX_D_I4 | B16 | Rx Data Q Bit 4 | Input |
| RX_D_I5 | A17 | Rx Data Q Bit 5 | Input |
| RX_D_I6 | B17 | Rx Data Q Bit 6 | Input |
| RX_D_I7 | A18 | Rx Data Q Bit 7 | Input |
| RX_D_I8 | B18 | Rx Data Q Bit 8 | Input |
| RX_D_I9 | A19 | Rx Data Q Bit 9 | Input |
| TX_DATA0 | B19 | Tx Data IQ Bit 0 | Output |
| TX_DATA1 | A20 | Tx Data IQ Bit 1 | Output |
| TX_DATA2 | B20 | Tx Data IQ Bit 2 | Output |
| TX_DATA3 | A21 | Tx Data IQ Bit 3 | Output |
| TX_DATA4 | B21 | Tx Data IQ Bit 4 | Output |
| TX_DATA5 | A22 | Tx Data IQ Bit 5 | Output |
| TX_DATA6 | B22 | Tx Data IQ Bit 6 | Output |
| TX_DATA7 | A23 | Tx Data IQ Bit 7 | Output |
| TX_DATA8 | B23 | Tx Data IQ Bit 8 | Output |
| TX_DATA9 | A24 | Tx Data IQ Bit 9 | Output |
| TX_CLK | B24 | Tx Data Clock | Output |
| SEL_TXD | A25 | Tx Data I/Q Select | Output |
| SYNENT | B25 | RF Transmit Synthesizer Enable | Output |
| SYNENR | A26 | RF Receive Synthesizer Enable | Output |
| SYNDAT | B26 | RF Synthesizer Data | Output |
| SYNCLK | A27 | RF Synthesizer Clk | Output |
| LD | B27 | RF Synthesizer Lockout Detect | Input |
| TX_EN | A28 | Enable RF TX Amp | Output |
| RX_EN | B28 | Enable RF RX Amp | Output |
| RF_ATTEN0 | A29 | RF Field Calibration Attenuator Bit 0 | Output |
| RF_ATTEN1 | B29 | RF Field Calibration Attenuator Bit 1 | Output |
| RF_ATTEN2 | A30 | RF Field Calibration Attenuator Bit 2 | Output |
| RF_ATTEN3 | B30 | RF Field Calibration Attenuator Bit 3 | Output |
| RF_ATTEN4 | A31 | RF Field Calibration Attenuator Bit 4 | Output |
| TX_POWER | B31 | Transmit Power Level | Analog |
| REF_FREQ | A32 | 20MHz Clock | Output |
| DGND | B32 | Digital Ground | Power |
| +10V | C1 | +10V (Power Amp) | Power |
| AGND | C2 | Analog Ground | Power |
| +10V | C3 | +10V (Power Amp) | Power |

| Signal | Pin | Description | Type |
|---|---|---|---|
| AGND | C4 | Analog Ground | Power |
| +10V | C5 | +10V (Power Amp) | Power |
| AGND | C6 | Analog Ground | Power |
| +10V | C7 | +10V (Power Amp) | Power |
| AGND | C8 | Analog Ground | Power |
| +7V | C9 | +10V (Power Amp) | Power |
| AGND | C10 | Analog Ground | Power |
| +7V | C11 | +7V Analog (RF and IF) | Power |
| AGND | C12 | Analog Ground | Power |
| +7V | C13 | +7V Analog (RF and IF) | Power |
| DGND | C14 | Digital Ground | Power |
| +5VDIG | C15 | +5V Digital | Power |
| DGND | C16 | Digital Ground | Power |
| +5VDIG | C17 | +5V Digital | Power |
| DGND | C18 | Digital Ground | Power |
| +5VDIG | C19 | +5V Digital | Power |
| DGND | C20 | Digital Ground | Power |
| -5V | C21 | -5V Analog | Power |
| DGND | C22 | Digital Ground | Power |
| -5V | C23 | -5V Analog | Power |
| DGND | C24 | Digital Ground | Power |
| 3.3V | C25 | 3.3V Digital | Power |
| DGND | C26 | Digital Ground | Power |
| 3.3V | C27 | 3.3V Digital | Power |
| NC | C28 | No Connection | |
| NC | C29 | No Connection | |
| NC | C30 | No Connection | |
| CSDA | C31 | $I^2C$ Data | I/O |
| CSCL | C32 | $I^2C$ Clock | Output |

## 3.23 JTAG Boundary Scan

3.23.1 Some devices support JTAG boundary scans. A JTAG chain is implemented on these devices to support JTAG testing during manufacturing. The JTAG controller can access all devices through the main JTAG connector.

3.23.2 Devices supporting JTAG

1). MPC855
2). DSP
3). FPGA
4). CPLD

3.23.3 Hardware will be in place to set each device into JTAG boundary scan mode when required.

3.24 Logic Analyzer Interface

3.24.1 Logic analyzer interfaces will be required for debugging.

3.24.2 Interface connector is a 38-pin MICTOR receptacle, AMP 2-767004-2 or equivalent.

3.24.3 Interface Signals

1). MPC address bus
2). MPC data bus
3). MPC signals
4). DSP address bus and signals
5). DSP data bus
6). FE and RS FPGA signals

3.24.4 Pinout to the 38-pin MICTOR receptacle should support Agilent Logic Analyzer for the specific device.

# 4 RF Board

4.1 Scope

4.1.1 This section provides the principles of operation for the RF Board.

4.1.2 Block diagram.

4.1.3 The RF board operates in Time-Division-Duplex mode.

## 4.2 Transmitter Path

The transmitter path converts the data from DE to an RF signal in the 5.8 GHz range and amplifies this signal to the desired output level. Prime requirements are preservation of signal linearity; and reduction of spurious signals.

### 4.2.1 DAC and Baseband

1). In transmit mode, the DE generates a single interleaved (I and Q) digital bus streams that are passed to RF board through DE/RF Connector. The digital-to-analog (DAC) converts the data stream into independent I and Q analog data streams. DAC is a dual 10-Bit, 40MSPS with 2x Interpolation Filters optimized for low distortion performance.

2). From this point the two signals are sent to a pair of baseband amplifier chains – one for I channel, one for Q channel. The I and Q amplifier chains are electrically identical so for sake of simplicity only the I channel will be explained here.

3). The I signal is delivered through high-speed operational amplifier to 5-pole elliptic type low pass filter.

4). After filtering, the I signal then passes through another op-amp. This amplifier also serves as a buffer – isolating the filter from the following modulator stage.

### 4.2.2 Mod/De-Mod, 1st IF Attenuators, Filters and Mixer and Switch

1). The I and Q signals are then passed to an IF quadrature modulator/demodulator. (RC1332)

2). The IF attenuator and IF BPF and Mixer are common to both the transmit and receive paths

3). Attenuator is a 5bit , GaAs IV FET digital attenuator that provides between 0 and 15.5 dB of attenuation in 0.5 dB steps. It consists of 5 step attenuators with values of 0.5; 1; 2; 4 and 8 dB. It operates under control from the DE and is used to set the set the overall gain during factory calibration; and to provide temperature compensation.

4). The Mixer will convert the 1$^{st}$ IF (374 MHz) to the 2$^{nd}$ IF (915 MHz) and vise versa.

5). IF Switch is a low-cost SPDT GaAs IC that switches the IF signal to either the transmit or receive path.

### 4.2.3 TX 2$^{nd}$ IF

1). IF Amp 1 and 2 are SiGe monolithic amplifiers that provide gain at 915 MHz with good linearity.

2). A digital attenuator is not required in this section as it is built into the RC1332

3). xx dB resistive attenuator is used to set the IF level into the mixer and provide a good impedance match to the mixer.

### 4.2.4 Mixer

1). Mixer is a monolithic GaAs double-balanced mixer. It was selected due to its high dynamic input signal range, small size and zero DC bias requirements. It requires at least 13 dBm of local oscillator power to achieve its conversion loss and linearity performance.

#### 4.2.5 1st RF Amplifier and Bandpass Filter

1). 1st RF Amplifier provides approximately 15 dB of gain at 5.8GHz.
2). RF Bandpass Filter is a three pole ceramic filter that is primarily used to attenuate the Local Oscillator and image frequencies.

#### 4.2.6 2nd RF Amplifier

1). 2nd RF Amplifier provides approximately 20 dB of gain. In order to minimize spurious emissions during receive mode, the amplifier is only biased when RF Board is in transmit mode. Bias is provided through the Power Switch. Control of this switch comes from the DE. The time constant of Power Switch is selected to provide an adequately low time constant with the gate-source capacitance of the PMOS switch, while minimizing power dissipation.

#### 4.2.7 RF Power Amplifier

1). RF Power Amplifier is a non-matched GaAs FET that provides 11 dB of gain with a 1-dB compression point of 36 dBm. As with all other active components in the transmitter chain, it is sufficiently back off from compression to achieve the required intermodulation performance. However, as the most costly device in the line-up it is the dominant source of intermodulation products.
2). Power Amplifier is biased to a drain voltage of 8V and drain current of 1400 mA typical. In order to minimize spurious emissions during receive mode, the amplifier is only biased when RF Board is in transmit mode. This also greatly reduces the average power consumption.

#### 4.2.8 Driver and PA Bias Control

1). The primary function if this circuitry is to ensure the discrete RF Power Amplifier is properly biased in transmit mode, that the bias is removed when not in the transmit mode, and that response time from transmit to receive and receive to transmit is sufficiently small to allow the desired turn-around time.

## 4.3 Front End Filter and Switch

#### 4.3.1 Front End Filter

1). The Front End Filter is a 3-pole ceramic filter that provides attenuation of unwanted signals.

#### 4.3.2 Switch

1). The Switch is a DPDT switch that switches the TX or RX to one of two antenna ports. This a hardware requirement for implementation of VINE.

## 4.4 Receiver Path

The receiver path converts the RF signal in the 5.8 GHz range to an IF signal and demodulates this signal to the desired output level. Prime requirements are preservation of signal linearity, and rejection of out-of-band spurious signals.

### 4.4.1 RF LNAs and RF Bandpass Filters

1). LNA 1 is a monolithic GaAs amplifier with a gain of approximately 13 dB and a noise figure of about 1.3 dB. BPF 1 is a 3-pole ceramic filter that provides additional attenuation of unwanted signals.

2). LNA 2 is a monolithic GaAs amplifier with a gain of approximately 19 dB.

3). Amplifiers LNA 1 and LNA 2 are turned off when the RF Board is in transmit mode. Turning off the amplifiers has two benefits. First, it avoids saturation of the amplifiers when transmitter power is present. This reduces the amount of time it takes for the gain to stabilize when the RF Board switches from receive to transmit. Second, it eliminates a potential parasitic feedback path whereby some transmit energy gets coupled to the receiver mixer, down-converted to IF, gets back into the transmit IF and then up-converted in the transmitter. Under certain circumstances it is possible for the transmitter and receiver to oscillate in this condition, but in any event there is a strong potential for undesired transmitter spurious emissions.

### 4.4.2 Mixer

1). Mixer is a monolithic GaAs double-balanced mixer. It was selected due to its high dynamic input signal range, small size and zero DC bias requirements. It requires at least 13 dBm of local oscillator power to achieve its conversion loss and linearity performance.

### 4.4.3 IF Filter and 1st IF Amplifier

1). Band Pass Filter reduces the level of local oscillator signal in the IF path.

2). 1st IF Amplifier is a Si monolithic amplifier that has good gain and linearity at 925 MHz, but little gain at 5.8 GHz and above.

3). Fixed attenuator is used to provide the optimum level to the 2nd IF amplifier.

### 4.4.4 2nd IF Amplifier, Filter and Switches

1). 2nd IF Amplifier is a high-gain, high linearity amplifier that is the final stage of amplification of the receiver. It has sufficient output drive capability to meet the output power requirements while overcoming the loss in the IF attenuators and filters.

2). LC low-pass filter provides further rejection of the receiver local oscillator and image frequencies.

3). IF Switch is a low-cost SPDT GaAs IC that switches the IF signal to either the transmit or receive path.

## 4.5 Local Oscillators

The RF Board requires 3 LO frequencies. One RF LO and 2 IF LO's. The 1st IF LO is included in the RC1332.

### 4.5.1 Voltage Controlled Oscillators

1). The 2nd IF LO will be around 540 MHz and the RF LO will be in the 2.4 to 2.5 GHz range. The output level of the VCO's is between 0 and 5 dBm, and the tuning sensitivity is between 30 and 50 MHz/V.

### 4.5.2 Buffer Amplifier and Splitter

1). The output of the RF VCO is doubled, buffered and split to feed both the RX and TX mixers.

2). The output of the IF VCO is buffered and will feed the mixer in the common IF path.

### 4.5.3 Doubler

1). The RF LO is doubled from 2.4 to 4.8 GHz by the Hittite HMC189 frequency doubler.

2). The doubling function degrades the phase noise by approximately 6dB.

### 4.5.4 PLL Synthesizer

1). PLL Synthesizer is the Analog Devices AD4252 fractional N synthesizer capable of operating to a maximum input frequency of 3 GHz. *Its detection sensitivity is much better if operated at a 3.3 V supply, so the 5 V supply is dropped by dual diode and resistor*. It has a programmable charge-pump output current.

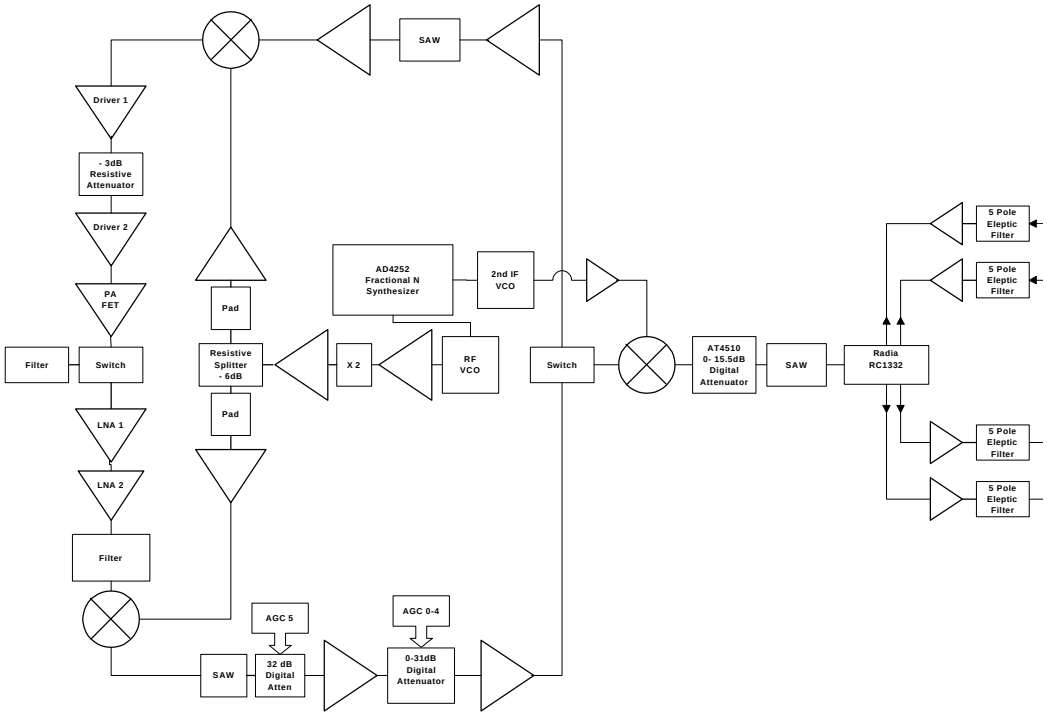
### 4.5.5 Loop Filter

1). The charge-pump output of the PLL is filtered to provide the desired reference attenuation, phase noise and dynamic characteristics.

### 4.5.6 Lock Detect Circuit

1). When the synthesizer is locked an LED is illuminated. The transmit and receive lock-detect signals are diode-ANDed. If either synthesizer goes out of lock, the combined lock-detect output goes high. This combined signal is fed to the DE, which disables the transmitter if it determines that either synthesizer is unlocked.

## 4.6 Block Diagram


SAW
Driver 1
- 3dB Resistive Attenuator
Driver 2
PA FET
Filter
Switch
LNA 1
LNA 2
Filter
Pad
Resistive Splitter - 6dB
Pad
AD4252 Fractional N Synthesizer
2nd IF VCO
X 2
RF VCO
Switch
AT4510 0- 15.5dB Digital Attenuator
SAW
Radia RC1332
5 Pole Eleptic Filter
5 Pole Eleptic Filter
5 Pole Eleptic Filter
5 Pole Eleptic Filter
AGC 5
AGC 0-4
SAW
32 dB Digital Atten
0-31dB Digital Attenuator