PG-1810 Service Manual

(GSM Cellular Phone)

Pantech Co., Ltd., Korea

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1st Edition

For Use by Authorized Service/Maintenance Personal Only

Documents to Receive This Addendum:

PG-1810 Maintenance/Repair/Operating Manual

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SECTION 1. INTRODUCTION

1.1 An Introduction of GSM Digital Cellular Mobile Communication System

GSM (Global System for Mobile communication) concluded that digital technology working in the Time Division Multiple Access (TDMA) mode would provide the optimum solution for the future system. Specifically , a TDMA system has the following advantage

- ► Offers a possibility of channel splitting and advanced speech coding, resulting in improved spectrum efficiency.
- ► Allows considerable improvements to be made with regards to the protection of information.

The GSM system is basically designed as a combination of three major subsystems;
The network subsystem, the radio subsystem, and the operation support system.
The functional architecture of a GSM system can be divided into the Mobile Station (MS), the Base Station (BS), and the Network Subsystem (NS). The MS is carried by the subscriber, the BS subsystem controls the radio link with the MS and the NS performs the switching of calls between the mobile and other fixed or mobile network users as well as mobility management. The MS and the BS subsystem communicate across the Um interface also known as radio link
The specifications relating to MS are as follows:

- TS 100 607-1 : Digital cellular telecommunication system(Phase2+)Mobile Station (MS) con Formance specification Part1: Conformance specification

1.2 Frequency Allocation and Its Use

- Transmit frequency band : 824 MHz ~ 849 MHz(For GSM850), 1850 MHz ~ 1910 MHz (For PCS1900), 1710 ~ 1785 MHz (For DCS)
- Receive frequency band: 869 MHz ~ 894 MHz(For GSM850) , 1930 MHz ~ 1990 MHz (For PCS1900), 1805 MHz ~ 1880 MHz(For DCS)
- Channel spacing : 200 KHz
- ARFCN(Absolute Radio Frequency Channel Number) : 128~251 (For GSM850), 512~810 (For PCS1900), 512~885 (For DCS).
- Separation between Transmit and Receive channels [MHz] : GSM850 : 45 MHz, DCS : 95 MHz, PCS ;80 MHz

For GSM850 Band Fl(n)=824.2+0.2*(n-128) 128 ≤n≤ 251 Fu(n)=Fl(n)+45
824 MHz ~849 MHz : Mobile Transmit,Base receive
869 MHz ~894 MHz : Base Transmit, Mobile receive
For PCS Band Fl(n)=1850.2+0.2*(n-512) 512 ≤n≤ 810 Fu(n)=Fl(n)+80
1850 MHz ~1910 MHz : Mobile Transmit,Base receive
1930 MHz ~1990 MHz : Base Transmit, Mobile receive
** Fl(n)= frequency value of the carrier , Fu(n)= corresponding frequency value in upper band
For DCS Band Fl(n)=1710.2+0.2*(n-512) 512 ≤n≤ 885 Fu(n)=Fl(n)+95
1710 MHz ~1785 MHz : Mobile Transmit,Base receive
1805 MHz ~1880 MHz : Base Transmit, Mobile receive

1.3 Item Name and Usage

PG-1810, GSM digital cell phone, is supercompact, superlight mobile communication terminal for personal use. It has a GSM850 850MHz and DCS 1800MHz/PCS 1900MHz frequency band and adopts GSM850 and DCS/PCS mode having excellent spectrum efficiency, economy, and portability.

This product is GSM Cellular type portable phone, adopting 1-cell Li-ion battery and power saving circuit to maximize its operation time. Also, it is equipped with a monoful intena and color TFT main LCD and CSTN sub LCD with font built in enables both Russia and English text service. And power control (basic feature of GSM), security feature, voice symbol feature, and variable data rate feature are used appropriately to ensure its best performance. This product consists of a handset, battery pack, and Travel charger.

1.4 Characteristics

1) All the active devices of PG-1810 are made of semiconductors to ensure excellent performance and semi-permanent use.
2) Surface mounting device (SMD) is used to ensure high reliability, compactness and lightness.
3) PG-1810 adopts the Silabs's AERO II RF transceiver(Si4210), which is CMOS RF front-end for multi-band GSM digital cellular handsets. The Aero's highly-integrated architecture eliminates the IF SAW filter, low noise amplifiers (LNAs) for three bands, transmit and RF voltage-controlled oscillator (VCO) modules, and more than 60 other discrete components found in conventional GSM handsets to deliver smaller, more cost effective GSM solutions that are easier to design and manufacture.
4) PG-1810 is designed to perform excellently even in the worst environment

Section 2. Electrical Specifications

2.1 General GSM850 / PCS1900 / DCS1800 Band

Mobile Transmit Frequency	824 ~ 849MHz / 1850 ~1910MHz / 1710 ~ 1785MHz
Mobile Receive Frequency	869 ~ 894MHz/ 1930 ~1990MHz / 1805 ~ 1880 MHz
The Number of Time Slot	8
The Number of Channels	124 / 299 / 375
Channel Spacing	200 kHz
Power Supply	Rechargeable Li-Ion Battery 3.7V/720mAH
Operating Temperature	-10℃ ~ +55℃
Dimension	95.5(H) ×46(W) ×18.7(D) mm
Weight	90 g

2.2 Transmitter GSM850 / PCS1900 / DCS1800 Band

Maximum Output Power	33±2 / 30±2dBm / 30±2dBm
Frequency Error	±90Hz / ±180Hz/ ±190Hz
Phase Error	RMS < 5°, PEAK < 20°
Minimum Output Power	5±5 / 0±5dBm
Power Control	5~19 / 0~15 (2 dB Step)
Output RF Spectrum	TS 100 910V6.2.0
Switching Transient	TS 100 910V6.2.0
Intermodulation attenuation	
Conducted Spurious Emissions	Idle Mode GSM850 -57dBm 9KHz~824M / 849MHz~1GHz -59dBm 824MHz~849MHz -47dBm 1GHz ~ 12.75GHz PCS -57dbm 9kHz ~ 1GHz -53dBm 1.850GHz ~ 1.910GHz -47dBm 1GHz ~ 1.850GHz / 1.910GHz ~ 12.75GHz
	Allocated Channel -36dBm 9KHz~ 1GHz -30dBm 1GHz~ 12.75GHz

2.3 Receiver

Reference Sensitivity	-102dBm	
For Adjacent interference For Adjacent(200KHz) interference For Adjacent(400KHz) interference For Adjacent(600KHz) interference	C/Ic	9 dB
	C/Ia1	-9 dB
	C/Ia2	-41 dB
	C/Ia3	-49 dB

Section 3 Operation

3.1 Name of each part

3.2 Display

3.2.1. Main LCD

Parameter	Projected Actual (MAIN LCD)
Display	260K Colors TFT LCD with white LED back lighting Character : (font size : 16×16) 10 lines x 8 characters
Driver	CL761AP (Core Logic)
Module Dimen.	34.2(H) x 54.13(V) x 3.35(D)
Active Area	1.8 " inches
Resolution(pixels)	128 x 160 pixels
Color Display Depth	16 bits + 2 bits

3.2.1. Sub LCD

Parameter	Projected Actual (SUB LCD)
Display	65K Colors CSTN LCD with white LED back lighting Character : (font size : 16×16) 6 lines x 6 characters
Driver	CL761AP (Core Logic)
Module Dimen.	34.4(H) x 54.13(V) x 3.5(D)
Active Area	1.04 " inches
Resolution(pixels)	96 x 96 pixels
Color Display Depth	16 bits

3.3 Keypad

	Market Goal	Projected Actual	Comments
English Keypad	0-9, *,# Send (Color) End/Pwr (Color) OK. Up (Porfile), Down (Phonebook), Left (Favorites), Right (SMS), Soft1 (Menu), Soft2 (Phonebook), C (Cancel / Back), * Key: Etiquette Mode # Key: Keypad Lock 0 Key: International 1 Key: Voice Mail key	0-9, *,# Send (Color) End/Pwr (Color) OK. Up (Porfile), Down (Phonebook), Left (Favorites), Right (SMS), Soft1 (Menu), Soft2 (Phonebook), C (Cancel / Back), * Key: Etiquette Mode # Key: Keypad Lock 0 Key: International 1 Key: Voice Mail key	Meets Goal. (Industrial design sample required) Meets Goal Keys for VR and Lock International Volume up/down

3.4 BLUETOOTH MODULE

Transmitter Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Output Power	Normal/extreme test	-	2	4	dBm
Power Density	Normal/extreme test	-	-	4	dBm
Power Control	Normal/extreme test	2dB ≤ Step size ≤ 8dB			
Frequency Range	Normal/extreme test	2400	-	2483.5	MHz
20dB Bandwidth	Normal/extreme test	-	850	1000	KHz
Adjacent channel power	±2MHz	-	-	-20	dBm
	±3MHz	-	-	-40	dBm
	±4MHz	-	-	-40	dBm
Modulation Characteristics	$\Delta F1_{avg}$	140	-	175	KHz
	$\Delta F2_{max}$	115	-	-	KHz
	$\Delta F2_{avg} / \Delta F1_{avg}$	-	-	80	%
Initial Carrier Frequency Tolerance		-75	-	75	KHz
Carrier Frequency Drift	One slot packet(DH1)	-25	-	25	KHz
	Three slot packet(DH3)	-40	-	40	KHz
	five slot packet(DH5)	-40	-	40	KHz
Transceiver Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Out-of-Band Spurious Emissions	30MHz-1GHz	-	-	-36	dBm
	1GHz-12.75GHz	-	-	-30	dBm
	1.8GHz-5.3GHz	-	-	-47	dBm
	5.1GHz-5.3GHz	-	-	-47	dBm
Receiver Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Sensitivity level	Single slot packets	-70	-80	-	dBm
Sensitivity level	Multi slot packets	-70	-	-	dBm
C/I performance	C/I co-channel	-	-	11	dB
	C/I_{1MHz} (Adjacent channel selectivity)	-	-	0	dB
	C/I_{2MHz} (2nd Adjacent channel selectivity)	-	-	-30	dB
	$C/I_{\geq 3MHz}$ (3rd Adjacent channel selectivity)	-	-	-40	dB
Blocking performance	30MHz-2000MHz	-10	-	-	dBm
	2000MHz-2400MHz	-27	-	-	dBm
	2500MHz-3000MHz	-27	-	-	dBm
	3000MHz-12.75MHz	-10	-	-	dBm
Intermodulation Performance	n=5	-39	-	-	dBm
Maximun Input Level		-20	-10	-	dBm

Section 4. Theory of Operation

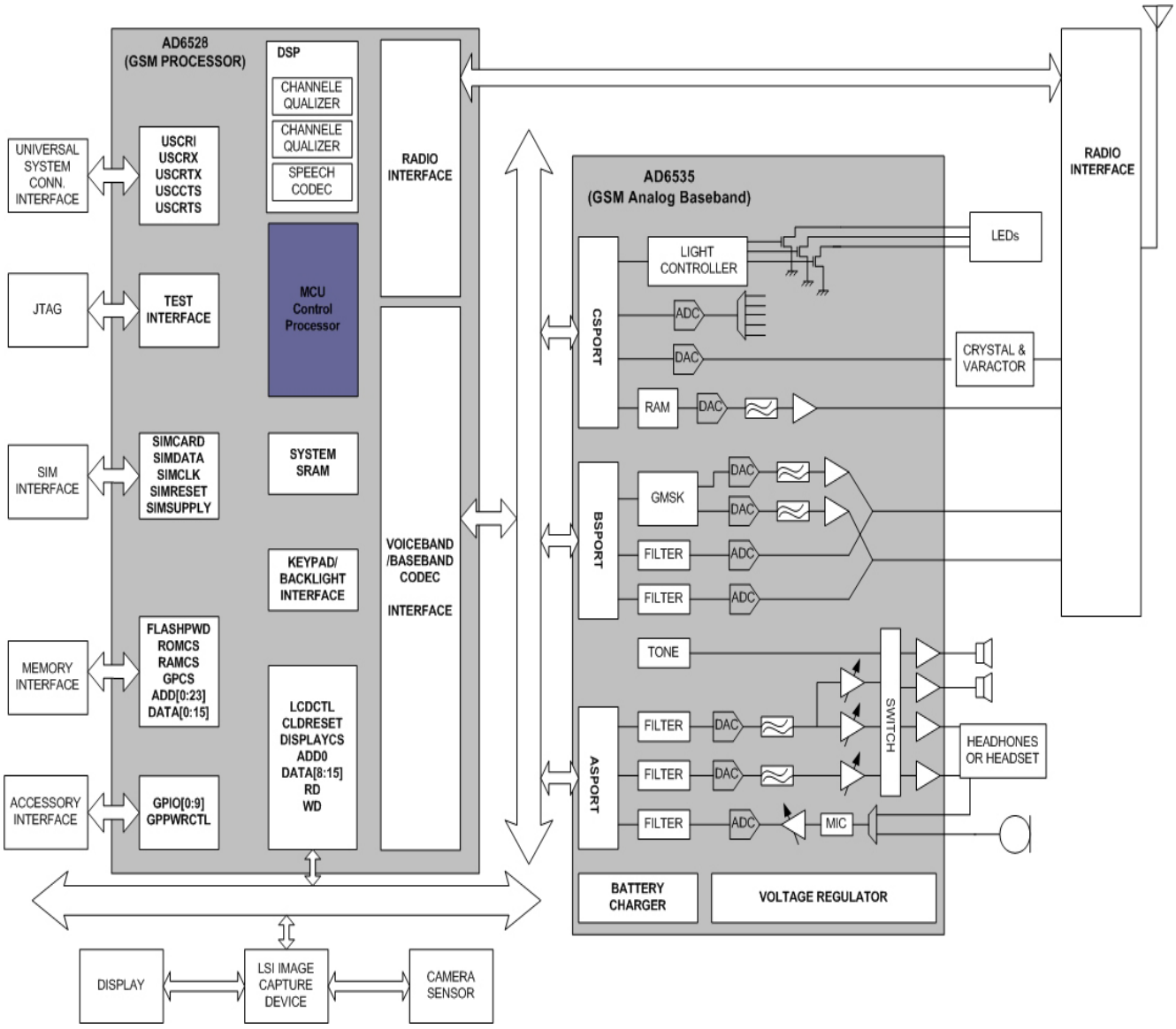
4.1 Logic Section

4.1.1 DC Distribution and Regulation Part

Applying battery voltage and pressing “END” key on the key pad short-circuits “Ground” and “_ PowerON”. AD6535(U202) control that power manage regarding power on/off in handset Pressing POWERKEY on the key pad is active on the handset.

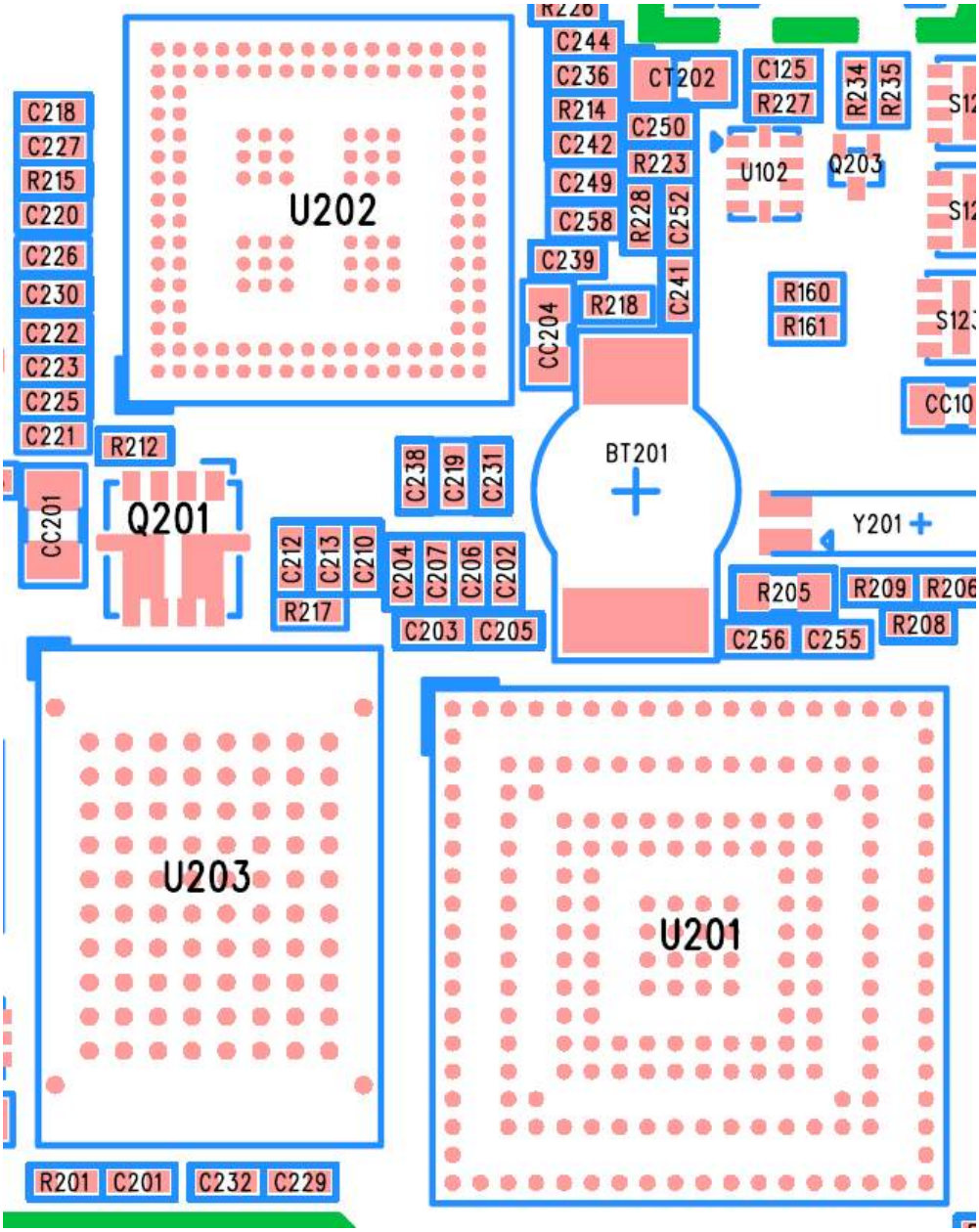
This will turn on all the LDOs, when POWERKEY is held low. The power of RF Tx power amplifier is supplied directly by the battery.

4.1.2 Logic part



4.1.2.1 Summary

The logic part consists of AD6528D ARM7 microprocessor-combined GSM-ASIC, COMBO(flash ROM & SRAM), AD6535 VBC Chip. AD6528D is GSM-ASIC chipset implemented for GSM terminal's system control and baseband digital signal processing.



Major parts used in the logic part are as follows:

1) AD6528D : U201, [ARM7 Processor Core + GSM Signal Processing] ASIC

2) AD6535 : U202, Analog Baseband Codec

3) COMBO MEMORY(Flash ROM : U203, 256Mbit Flash Memory + 64Mbit SRAM)

4.1.2.2 Baseband Digital Signal Processing

AD6528D is a GSM core device containing ARM7 CPU core. AD6535 is 148 pin BGA package, consisting of terminal chips. The function and characteristics of clock are as follows:

1) Complete single chip GSM Processor
2) Channel codec sub-system
   - Channel coder and decoder
   - Interleaver and Deinterleaver
   - Encryption and Decryption
3) Control Processor Subsystem including
   - Parallel and serial Display interface
   - Keypad Interface
   - SIM Interface
   - Control of RADIO subsystem
   - Real Time Clock with Alarm

☞ Configuration by Function of AD6528D

1 Microprocessor Core

AD6528D has a built-in ARM7 microprocessor core, including microprocessor interrupt controller, timer/counter, and DMA controller. And besides, 32bit data path is included, and up to 8Mbyte addressing is enabled and can be extended up to 16Mbyte. Although external clock should be provided to operate the microprocessor, this core uses 26MHz VCTCXO to provide clock.

2 Input Clock

1) Main Clock(26 MHz):
   This is the clock needed for the microprocessor built in AD6528D to operate.
2) VC-TCXO(26MHz) , 32.768KHz Clock:
   This is the system reference clock to control SLEEP mode.
   This is the clock derived from 26MHz VC-TCXO clock, provided by RF part. It is the timing reference clock for GSM signal processing.

3 DSP Subsystem

This is a GSM signal processing part in GSM mode, consisting of speech transcoding and Channel equalization as follows:

1) Speech transcoding

In full rate, the DSP receives the speech data stream from VBC and encodes data from 104kbps to 13kbps. Using algorithm is Regular Pulse Excitation with Long Term Prediction (RPE-LTP).

2) Equalization

The Equalizer recovers and demodulates the received signal

The Equalizer establishes local timing and frequency references for mobile terminal as well as RSSI calculation.

The equlization algorithm is a version of Maximum Likelihood Sequency Estimation (MLSI) using Viterbi Algorithm.

☞ GSM Core and RF Interface

1) Transmitter:
   AD6535 VBC receive data at 270kbps and use an on chip lock-up table to perform GMSK modulation. A pair of 10bit matched differential DACs converts the modulated data and pass I and Q analog data to the transmit section of the radio system.
2) Receiver:
   The receiver I and Q signals are sampled by a pair of ADCs at 270kbps.
   The I and Q samples are transferred to the EGSMP through a dedicated receive path serial port.

4 RF Interface

This interfaces the RF part to control power amplifier, Tx LO buffer amplifier, VC-TCXO, and AGC-end on transmit/receive paths in the RF part.

1) Transmitter Interface:

This transmits TX_AGC signal to Tx AGC amplifier to adjust transmit power level and sends Ramp_DAC signal to the RF part to control power amplifier.

2) Receiver Interface:

This transmits RX_AGC signal to Rx AGC amp. to adjust receive path gain.

5 General Purpose ADC Support

The AD6535 includes a general purpose 10bit auxiliary ADC with four multiplexed input channel These are used for measurment of battery voltage ID , temperature and accessory ID.

6 USC(Universal System Connector) Interface

A Typical GSM handset requires serial connections to provide data during normal phone operation Manufacturing, testing and debugging.

7 General Purpose Interface

The AD6528D provides 32 interface pin for control of peripheral devices.
All GPIO pins start up as inputs. Additional purpose inputs and outputs are available under SW control.

8 Speech Transcoding

In full rate mode, the DSP receive the speech data stream from the VBC and encodes data from 104kbps to 13kbps.Using algorithm is Regular Pulse Exitation with Long Term Prediction as specified GSM Recommandation

9 Power Down Control Section

1) Idle Mode Control:

If IDLE/ signal turns ‘Low’, transmitter section becomes disabled.

2) Sleep Mode Control:

If IDLE/ and SLEEP/ signals turn ‘Low’, all the sections except for VC-TCXO circuit become disabled.

3) Receiver & Transmitter Mode Control:

If IDLE/ and SLEEP/ signals turn ‘High’, all the sections become enabled to perform transmit/receive operation.

4.1.3 Memory Part

Memory consists of COMBO (flash ROM & SRAM).

1 Flash ROM

Flash ROM has a capacity of 256Mbit(32MByte). The main programs of the terminal(call processing, user interface, and diagnostic task) and supplemental programs (NAM program and test program) are stored in the flash ROM. Even if the program version may be changed in the future, customers can download the program.

2 Static RAM

SRAM has a capacity of 64Mbit(8MByte) and stores system parameters, data buffer, and stack of each task in it.

3 Key Tone Generation

All alert signals are generated by the DSP and output to the EVBC.

These alert can be used for the earpiece.

4.1.4 Notification Part

The notification of incoming call is given by melody, vibrator.

1) Melody:

   This is a device sounding alert/melody tones.

   The melody datas are stored in flash memory (U203) And generated by Melody IC(U117).

2) Vibrator:

   This is a device enabling vibration. The vibrator data is stored in flash memory(U203)

   And generated by AD6535(U202).

4.1.5 Key Pad Part

To enable key operation to input information, the key matrix is configured using strobe signal of KEYPADROW(0-4) and 5 input ports of KEYPADCOL(0-4). Also, to use the key even at light, the backlight circuit is provided for LED 17s.

4.1.6 LCD Module(Display Part)

LCD module consists of LCD, controller, LED-Backlight, and LCD reflector.using dual LCD

Main LCD: 1S/W Icon x 1 lines[(128x3)x160] can be displayed on the LCD panel. 6 icons could be provided by S/W. Controller with English font built in has been used.

Sub LCD: 1S/W Icon x 1 lines[(128x3)x160] can be displayed on the LCD panel. 6 icons are provided. Controller with English font built in has been used.

LED-backlight Using illuminates the LCD panel, and LCD reflector enhances LCD display effect.

4.2 Radio Transceiver Section

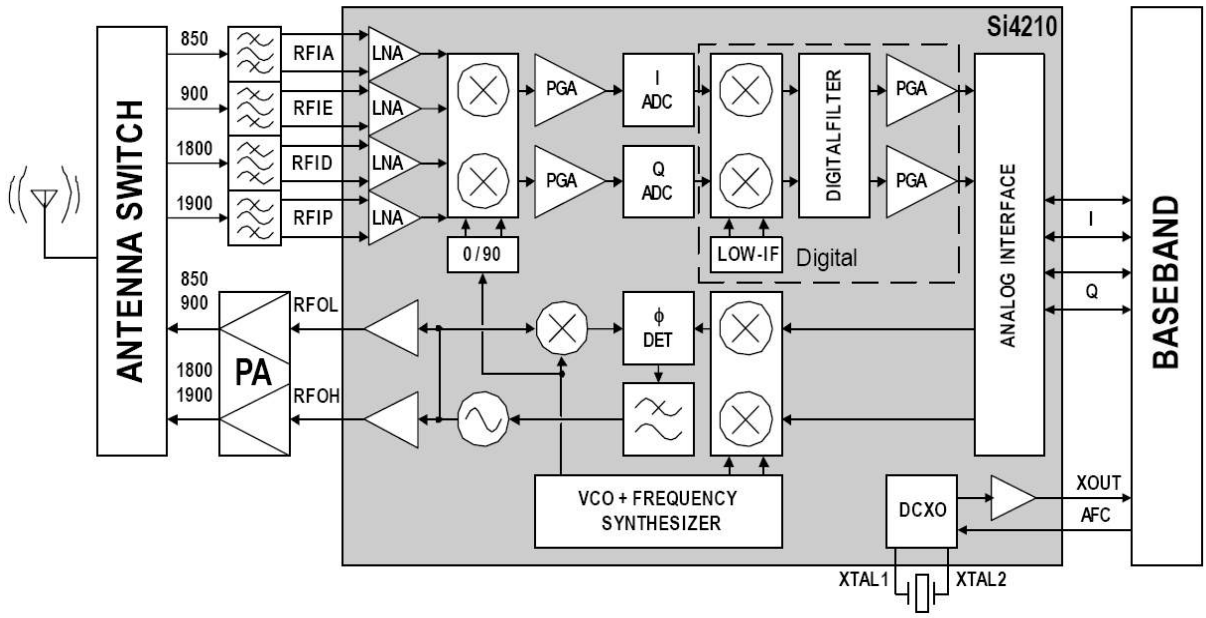


Fig.4-1. RF Transceiver block diagram

The PG-1810's RF Transceiver, which is AERO II (SI4210) transceiver is the industry's most integrated

RF front end for multi-band GSM/GPRS digital cellular handsets and wireless data modems.

The highly integrated solution eliminates the IF SAW filter, external low noise amplifiers (LNAs) for three bands, transmit and RF voltage controlled oscillator (VCO) modules, and more than 70 other discrete components found in conventional designs. The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduced complexity. The baseband interface is compatible with any supplier's baseband subsystem. The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifier, and uses an offset phase-locked loop (PLL) with a fully integrated transmit VCO. The frequency synthesizer uses Silicon Laboratories' proven technology, which includes integrated RF and IF VCOs, varactors, and loop filters.The unique integer-N PLL architecture produces a transient response that is superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. This fast transient response makes the AERO II (SI4210) transceiver well suited to GPRS multi-slot applications where channel switching and settling times are critical.

The following Figure shows of RF Transceiver PCB Layout

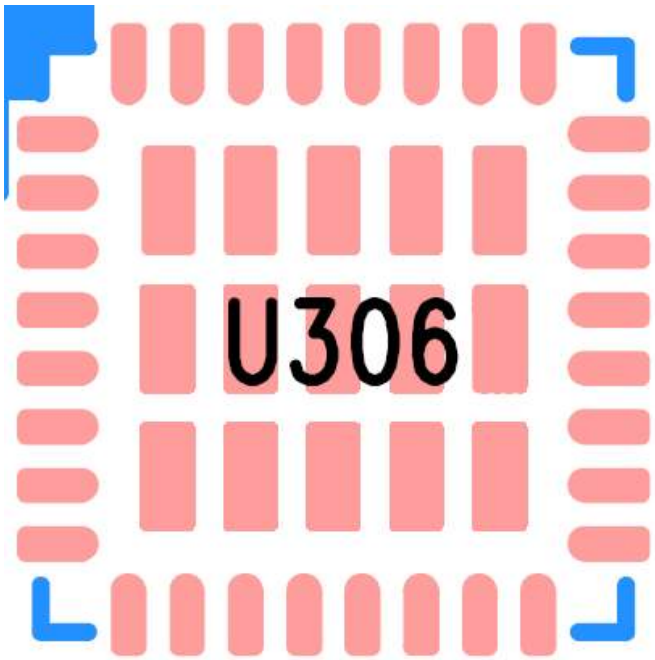


Fig.4-2. Top view of RF Transceiver PCB Layout

4.2.1 DC Distribution and Regulation Part

The battery voltage, in return, is applied to the logic part and RF part via LDO(Low Drop-Out) regulator. As several LDO regulators are used, power can be supplied for each necessary part efficiently. Audio/Logic parts use +2.8V. Si4210 RF Transceiver (U306) also use +2.8V DC voltage.

4.2.2 Transciever pin description

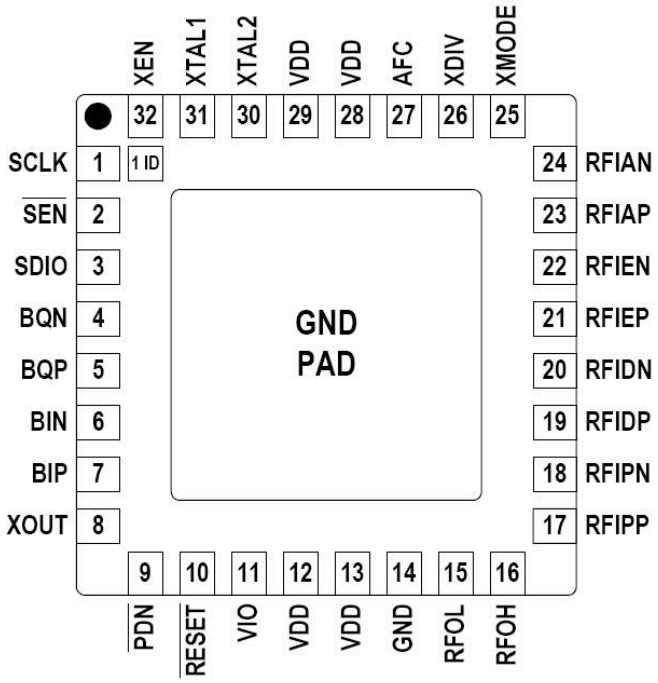


Fig.4-3. Top View of Si4210-GM

Pin Number(s)	Name	Description
1 ID	—	Pin 1 ID marker (bottom). No connect; leave floating
1	SCLK	Serial clock input.
2	$\overline{SEN}$	Serial enable input (active low).
3	SDIO	Serial data input/output.
4,5	BQP, BQN	Transmit/receive Q input/output (differential).
6,7	BIP, BIN	Transmit/receive I input/output (differential).
8	XOUT	Clock output to baseband.
9	$\overline{PDN}$	Powerdown input (active low).
10	$\overline{RESET}$	Reset pin (active low). May be no connect.
11	V_{IO}	Interface supply voltage.
12, 13, 28, 29	V_{DD}	Supply voltage.
14, PAD	GND	Ground. Connect to ground plane on PCB.
15	RFOL	GSM 850 and E-GSM 900 band transmit output to power amplifier.
16	RFOH	DCS 1800 and PCS 1900 band transmit output to power amplifier.
17,18	RFIPP, RFIPN	PCS 1900 band LNA input (differential).
19, 20	RFIDP, RFIDN	DCS 1800 band LNA input (differential).
21, 22	RFIEP, RFIEN	E-GSM 900 band LNA input (differential).
23, 24	RFIAP, RFIAN	GSM 850 band LNA input (differential).
25	XMODE	DCXO or VC-TCXO mode pin enable.
26	XDIV	XOUT frequency select input.
27	AFC	Baseband analog AFC input.
30, 31	XTAL2, XTAL1	Crystal output and input.
32	XEN	XOUT pin enable.

Table 4-1. Pin Description of Si4210-GM

4.2.3 Receiver Section

4.2.3.1 An Overview of Receive section

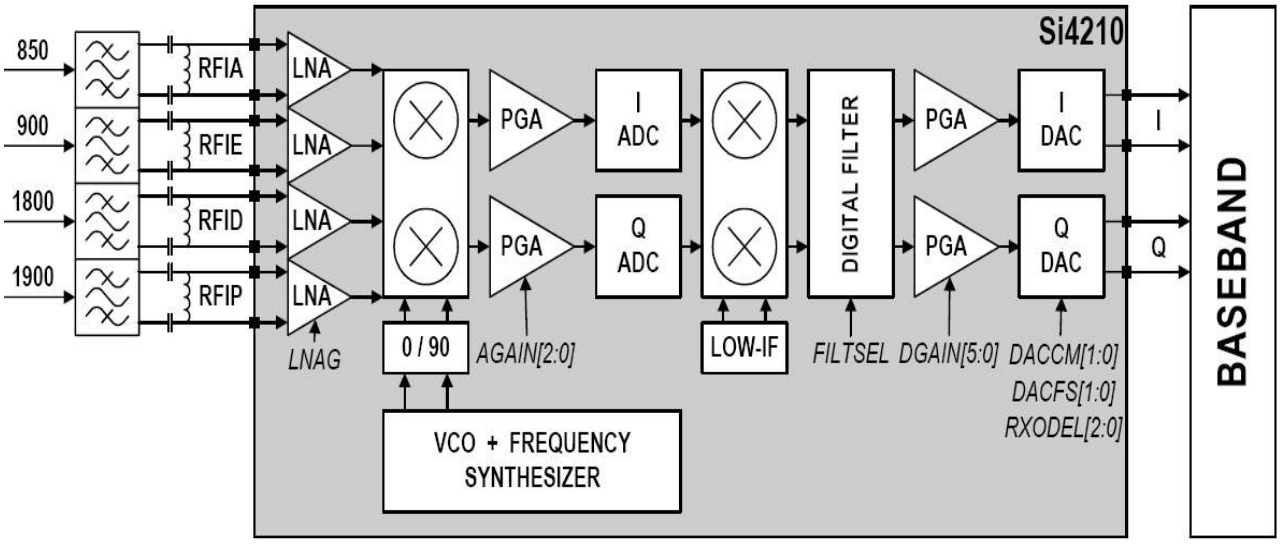


Fig.4-6. Receiver block diagram

PG-1810's Aero II transceiver uses a digital low-IF receiverar chitecture that allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters, and the IF SAW filter required in conventional superheterodyne architectures. Compared with direct-conversion architectures, the digital low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, second-order distortion of blockers (AM suppression), and device 1/f noise.

The digital low-IF receiver's immunity to dc offsets has the benefit of expanding part selection and improving manufacturing. At the front end, the common-mode balance requirements on the input SAW filters are relaxed, and the PCB board design is simplified. At the radio's opposite end, the BBIC is one of the handset's largest BOM contributors. It is not uncommon for a direct conversion solution to be compatible only with a BBIC from the same supplier in order to address the complex dc offset issues. However, since the Aero II transceiver has no requirement for BBIC support of complex dc offset compensation, it is able to interface to all of the industry leading baseband ICs.

The receive (RX) section integrates four differentialinput low noise amplifiers (LNAs) supporting the GSM 850 (869–894 MHz), E-GSM 900 (925–960 MHz), DCS 1800 (1805–1880 MHz), and PCS 1900 (1930– 1990 MHz) bands. The LNA inputs are matched to 150 or 200 Ω balanced-output SAW filters through external LC matching networks. The active LNA input is automatically selected by the ARFCN[9:0] bits and the BANDIND bit in Register 21h. If performing LNA swapping, the LNASWAP bit in Register 05h is also needed. The LNA gain is controlled with the LNAG bit in Register 20h. A quadrature image-reject mixer downconverts the RF signal to a low intermediate frequency (IF). The mixer output is amplified with an analog programmable gain amplifier (PGA) that is controlled with the AGAIN[2:0] bits in Register 20h. The quadrature IF signal is digitized with high resolution analog-to-digital converters (ADCs).

The ADC output is downconverted to baseband with a digital quadrature local oscillator signal. Digital decimation and FIR filters perform digital filtering, and remove ADC quantization noise, blockers, and reference interferers. The response of the FIR filter is programmable to a flat passband setting (FILTSEL = 0, Register 08h) and a linear phase setting (FILTSEL = 1, Register 08h). After filtering, the digital output is scaled with a PGA, which is controlled with the DGAIN[5:0] bits in Register 20h.

The LNAG, AGAIN[2:0], and DGAIN[5:0] register bits should be set to provide a constant amplitude signal to the baseband receive inputs.

Digital-to-analog converters (DACs) drive differential I and Q analog signals onto the BIP, BIN, BQP, and BQN pins to interface to standard analog-input baseband ICs. The receive DACs are updated at 1.083 MHz and have a first-order reconstruction filter with a 1 MHz bandwidth. No special processing is required in the baseband for dc offset compensation. The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). The common mode level at the receive I and Q outputs is programmable with the DACCM[1:0] bits, and the fullscale level is programmable with the DACFS[1:0] bits in Register 05h.

PG-1810's Aero II LNA inputs may be swapped. The low-band LNA inputs, RFIA and RFIE, are interchangeable and may be used to receive either the GSM 850 or E-GSM 900 band. The high-band inputs, RFID and RFIP, are interchangeable and may be used to receive either the DCS 1800 or PCS 1900 band. This flexibility enables radio designers to use one PCB layout for a phone design with only a bill of materials and software change to address different regions.

For normal operation, the LNA swap bit should be set to zero; this is the default setting. In this default mode, the native pin inputs and LNA are used for the corresponding frequency band. As an example, the RFIA inputs and GSM 850 LNA are used for GSM 850 operation.

To implement LNA swapping with the Aero II transceiver, the LNA swap bit in register 05h is used. The LNA swap bit should then be set to one. In LNA swapping mode, the non-native pin inputs and LNA are used for the frequency band. As an example, the RFIA inputs and GSM 850 LNA are used for E-GSM 900 operation.

4.2.3.2 Receiver Part

Antenna Swithch Module with SAW Filter : U301

FEM (Front End Module) consists of Tx filter, having an antenna port, and dual configuration with the transmitting path isolated from the receiving path, and Rx saw filter. A signal receives from the antenna of frequency band which is 881.5±12.5MHz for GSM850 bands, 1842.5±37.5 MHz for DCS bands, and 1960±30 MHz for PCS bands and transmits it to the saw filter for each band. The Tx filter passes through the output signals of frequency band that is 836.5MHz ±12.5MHz for GSM850 bands, 1747.5±37.5 MHz for DCS bnads, and 1880 ±30 MHz for PCS bands from the power amplifier and transmits it to the antenna. The maximum insertion loss is about 1.5 dB for the receiving bands at 25^{o} C and about 1.5 dB for the transmitting bands at 25^{o} C.

SAW filter consist of the GSM850 band signals which range 881.5±12.5MHz, the DCS band signals which range 1842.5±37.5, and the PCS bands that cover 1960±30MHz. it degrade other band signals with high passing loss of 30~60 dB and maximum insertion loss is 2.6 dB

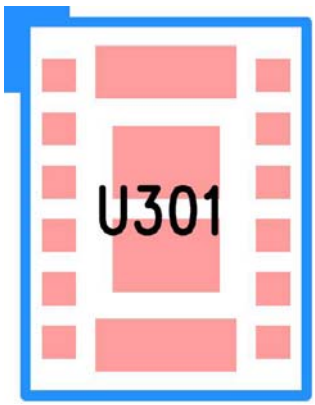


Fig.4-7. Receiver part PCB Layout

4.2.4 Transmit Section

4.2.4.1 An Overview of Transmit Section

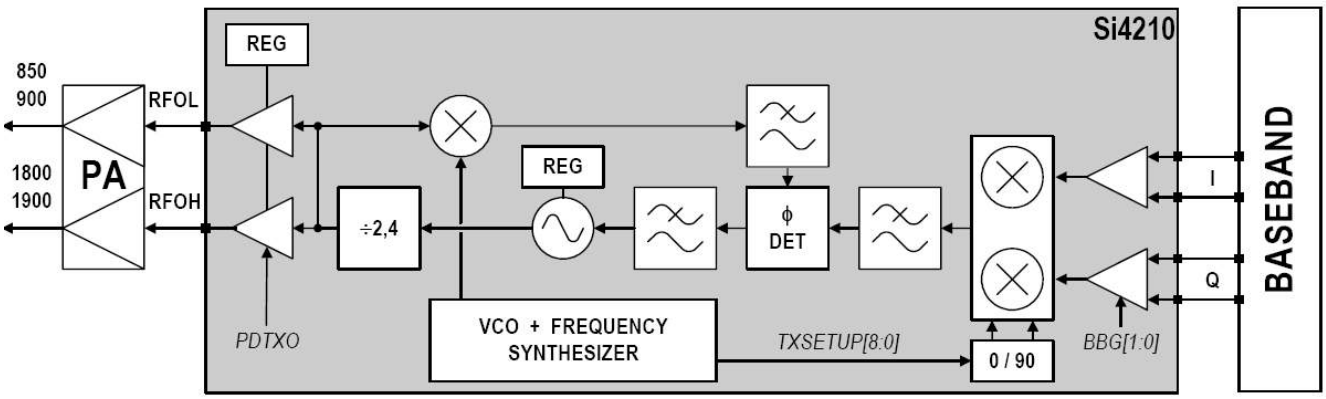


Fig.4-8. Transmitter block diagram

The transmit section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two output buffers that can drive an external power amplifier (PA). One output is for the GSM 850 (824 – 849 MHz) and E-GSM 900 (880–915 MHz) bands and one output is for the DCS 1800 (1710–1785 MHz) and PCS 1900 (1850–1910 MHz) bands.

The OPLL requires no external filtering to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power. The output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA. Additionally, the TXVCO benefits from isolation provided by the transmit output buffers. This significantly minimizes any load pull effects and eliminates the need for off-chip isolation networks.

A quadrature mixer upconverts the differential in-phase (BIP, BIN) and quadrature (BQP, BQN) baseband signals to an intermediate frequency (IF) that is filtered and which is used as the reference input to the OPLL. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs.

The transmit I/Q interface must have a non-zero input no later than 94 quarter bits after PDN is asserted for proper operation. If the baseband is unable to provide a sufficient TX I/Q non-zero input preamble, then the CWDUR bits in Register 05h can be used to provide a preamble extension.

The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). In transmit mode, the BIP, BIN, BQP, and BQN pins provide the analog I/Q input from the baseband subsystem. The full-scale level at the baseband input pins is programmable with the BBG[1:0] bits in Register 05h. The transmit output path is automatically selected by the ARFCN[9:0] bits and the BANDIND bits in Register 21h. As an option for multislot applications, direct control of the output transmit buffers during a burst is offered through the PDTXO bit in Register 23h.

4.2.4.2 Transmitter Part

A. 6dB attenuators : U304, U305

These passive components are adopted for PAM to operate in a stable output power.

B. Antenna Switch Module With SAW Filter : U301

These filters pass through the signals of which frequency band of 824~849MHz, 1710MHz~1785MHz, 1850MHz~1910MHz which is the transmit frequency of GSM850, DCS, PCS system terminal, and it suppresses other images and spurious frequencies when the terminal transmits GMSK modulated frequencies.

C. Power AMP Module(PAM) : U303

This device amplifies signals ahead of transmiting them through the antenna to provide a sufficient RF power. It has amplification factor of 28dB and efficiency of about 53% typically in GSM band and amplification of 27dB and efficiency of about 53% typically DCS/PCS band.

D. RF Switch connector : J301

RF Switch connector used to test Mainboard's RF characteristics and to calibrate.

E. Antenna: Antenna Contact Plate : INT301

This device enables signals to be transmitted and received from BTS by Um interface.

External Antenna can be contacted with Mainboard through Antenna Contact Plate.

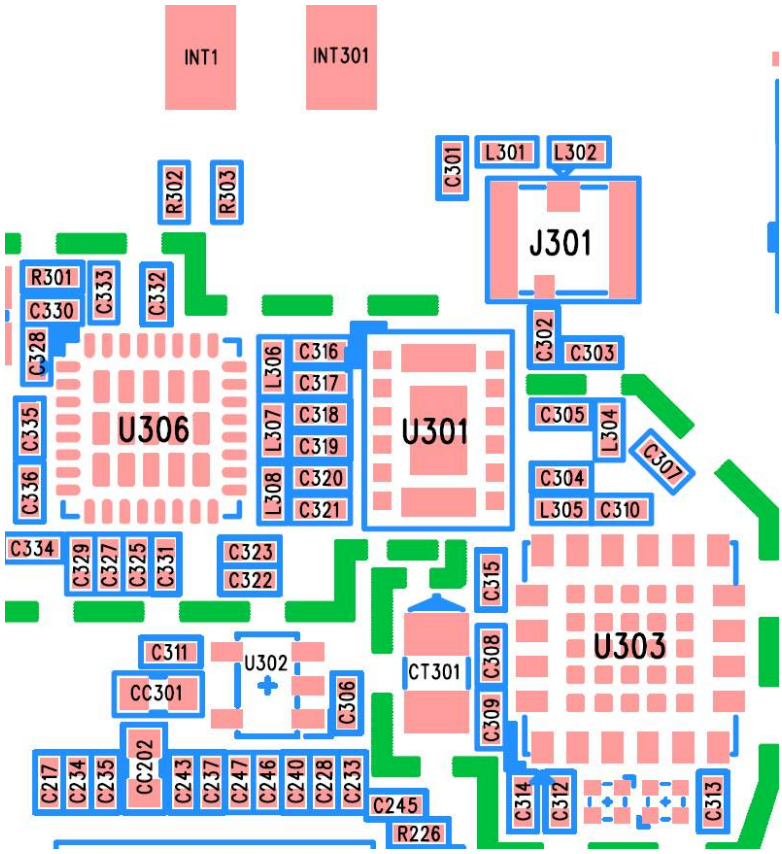


Fig.4-9. Transmit part PCB Layout

4.2.5 Offset PLL

4.2.5.1 An Overview of Offset PLL

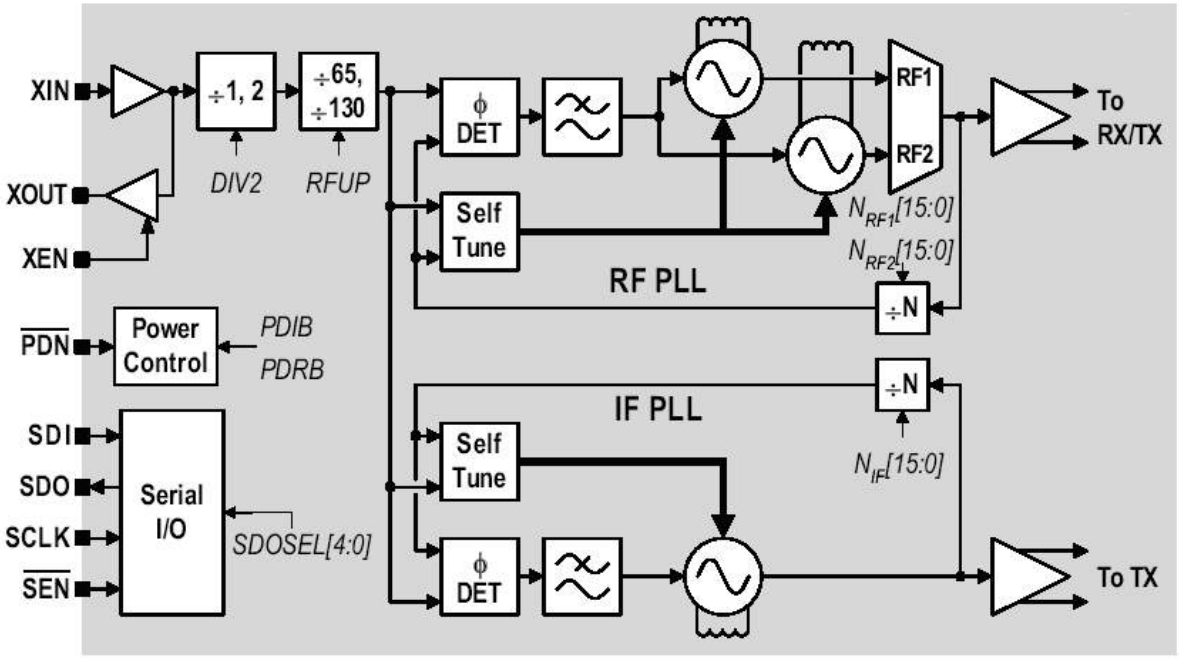


Fig.4-10. Si4210 Frequency Synthesizer Block Diagram

The Aero II transceiver integrates two complete PLLs including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and the RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode. All VCO tuning inductors are also integrated.

The IF and RF output frequencies are set by programming the N-Divider registers, NRF1, NRF2 and NIF. Programming the N-Divider register for either RF1 or RF2 automatically selects the proper VCO. The output frequency of each PLL is as follows:

$$fOUT = N \times f\phi$$

The DIV2 bit in register 31h controls a programmable divider at the XIN pin to allow either a 13 or 26 MHz reference frequency. For receive mode, the RF1 PLL phase detector update rate ($f\phi$) should be programmed $f\phi$ = 100 kHz for DCS 1800 or PCS 1900 bands, and $f\phi$ = 200 kHz for GSM 850 and E-GSM 900 bands. For transmit mode, the RF2 and IF PLL phase detector update rates are always $f\phi$ =200 kHz.

4.2.5.2 VC-TCXO(Voltage Controlled Temperature Compensated Crystal Oscillator): U307

This is the mobile station's reference frequency source. Its frequency is 26MHz, this signal is applied to the XOUT Buffer in Si4210 and the XOUT Buffer provides the 26MHz system reference clock.

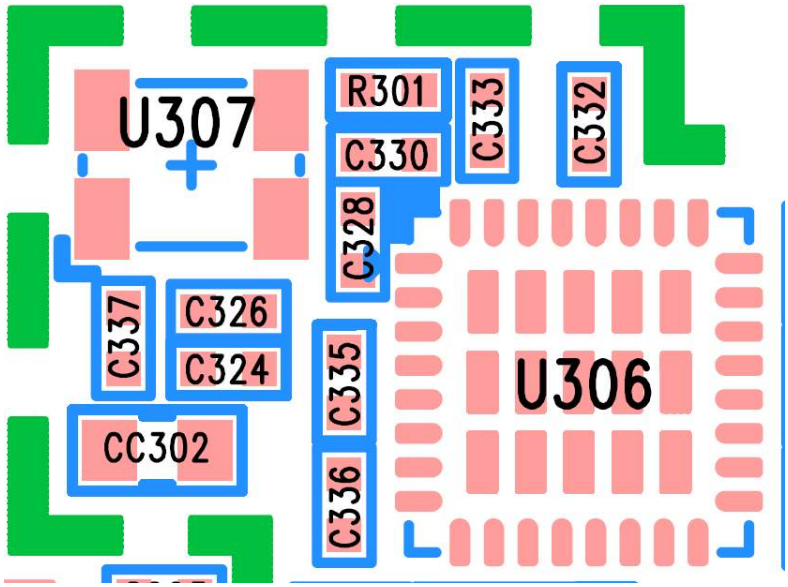


Fig.4-11. Top view of VCTCXO part on the PCB artwork

Section 5. Alignment Procedure

5.1 Recommended Test Equipment

Model No.	Description	Maker	Remark
E5515C	GSM Mobile Station Test Set	Agilent Technologies	
8593E	Spectrum Analyzer	Hewlett Packard	
TDS 3054B	Oscilloscope	Tektronix	
FLUKE 87	Digital Multimeter	Fluke	
E3630A	DC Power Supply	Hewlett Packard	
Others	Accessory		Interface Connectors RF Connectors

5.2 Connection of Test Equipment

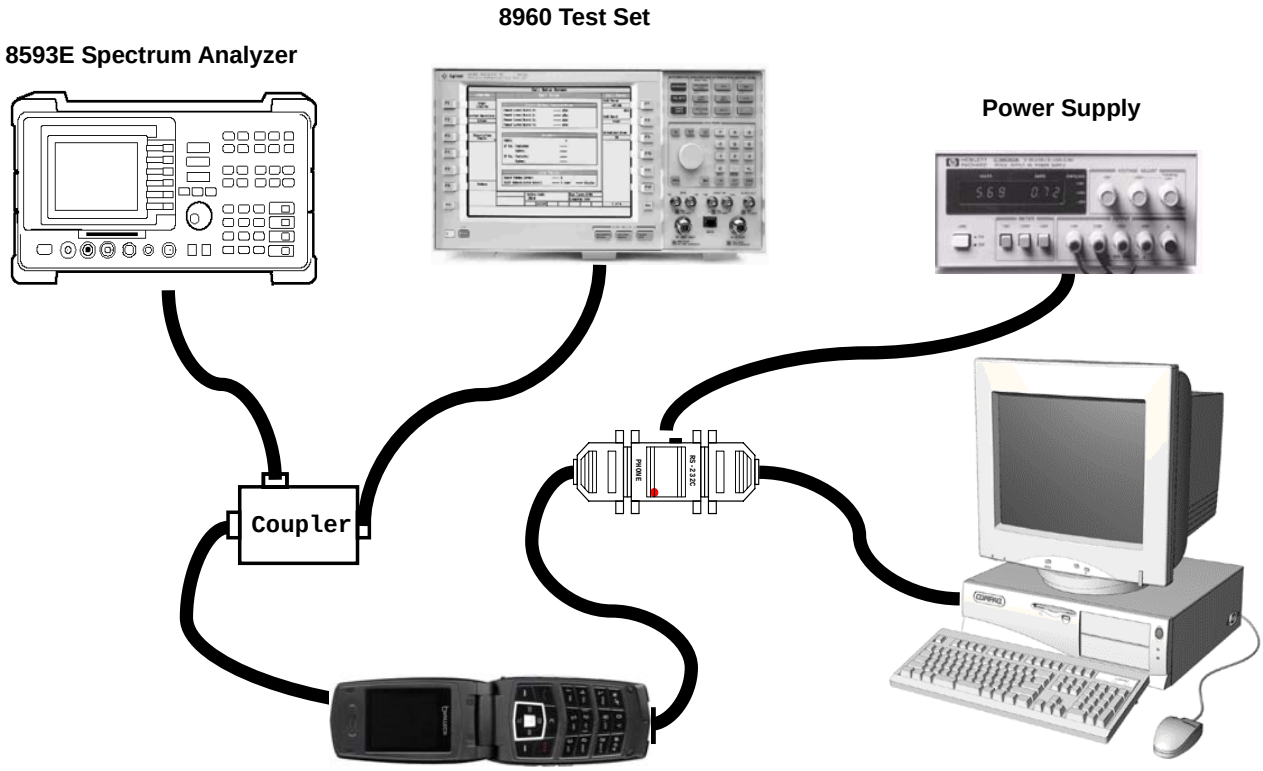
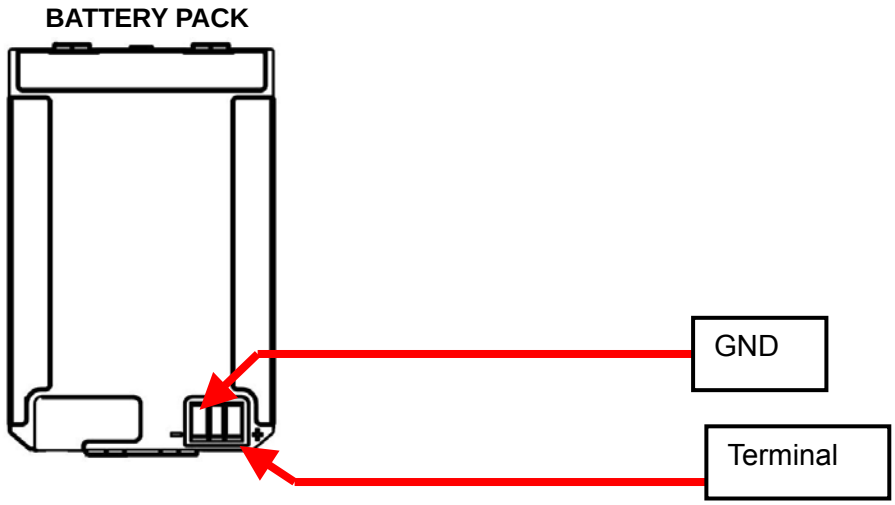


Fig.5-1. Test Set Configuration

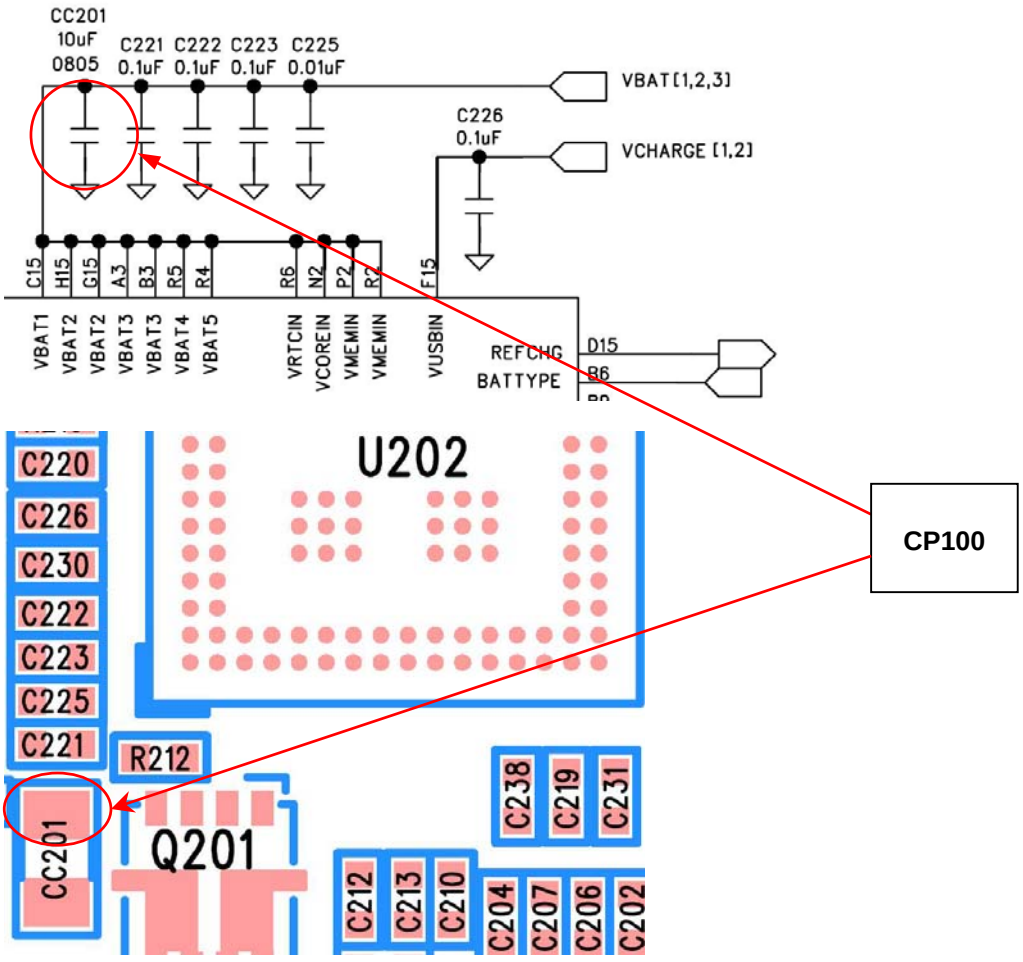
SECTION 6. Equipment Repair Procedure

6.1.1 Power CHECK

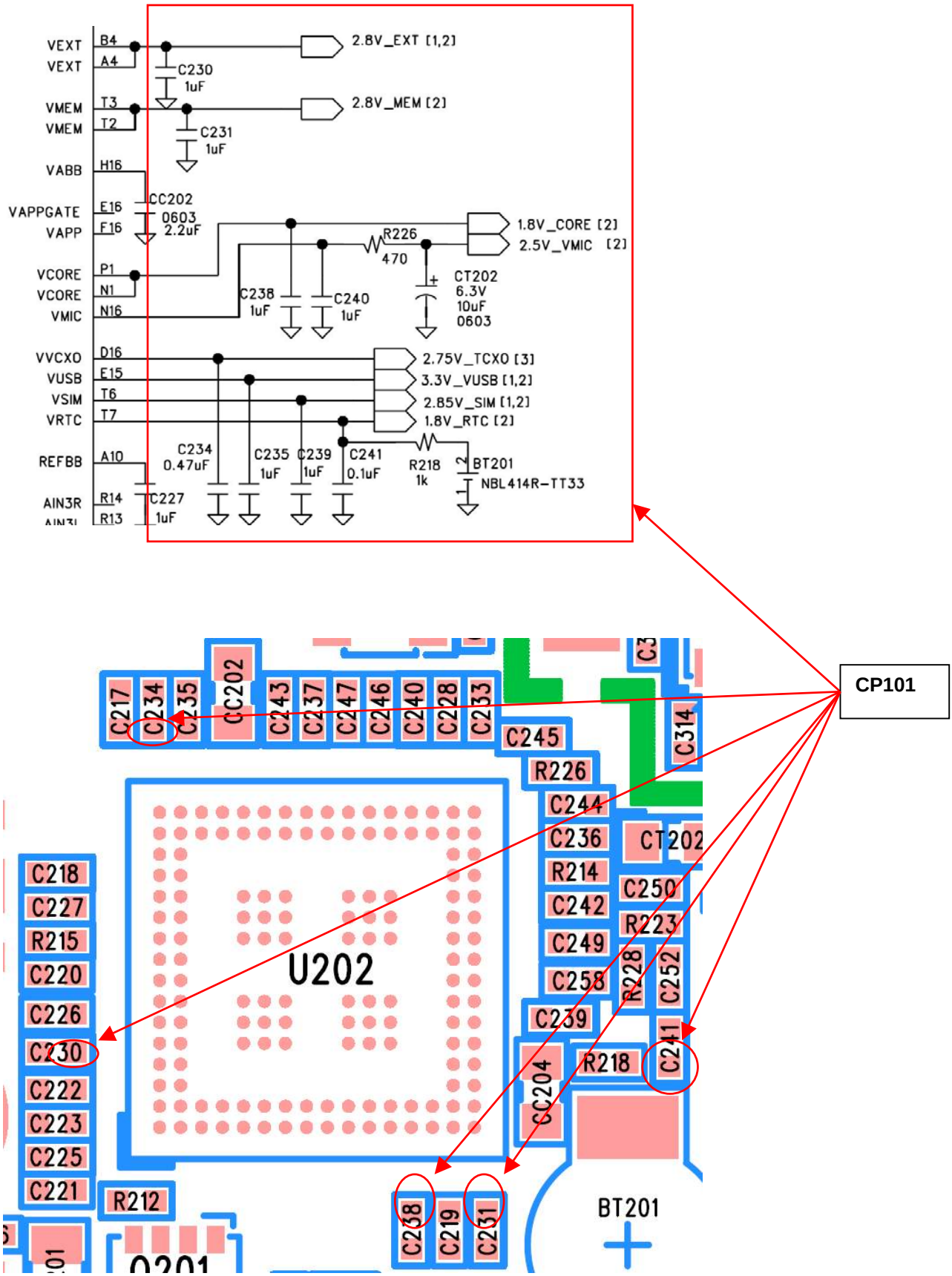
1. Check battery power : 3.5V~4.2V.



2. Check to see if U202. CC201 pin voltage is same with battery power : CP100

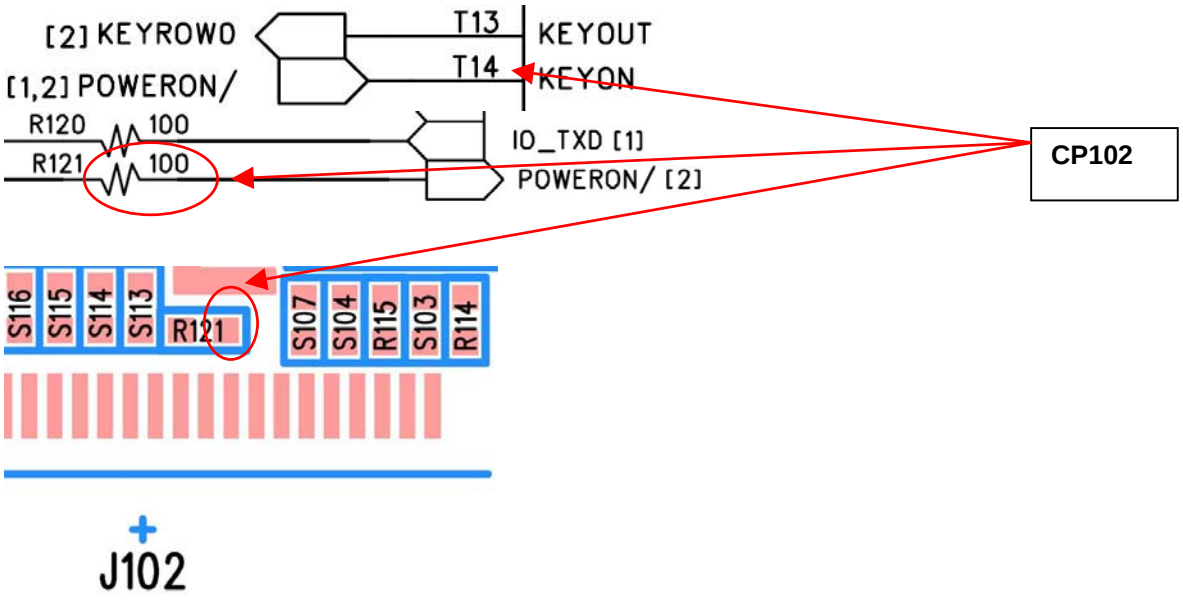


3. Check to see if U202. A4_B4,T2_T3,P1_N1,D16 and T7 pin is 2.8V, 2.8V,1.8V, 2.75V and 1.8V : CP101



4. Check to see if U202.T14 and R121 pin becomes to 0V : CP102

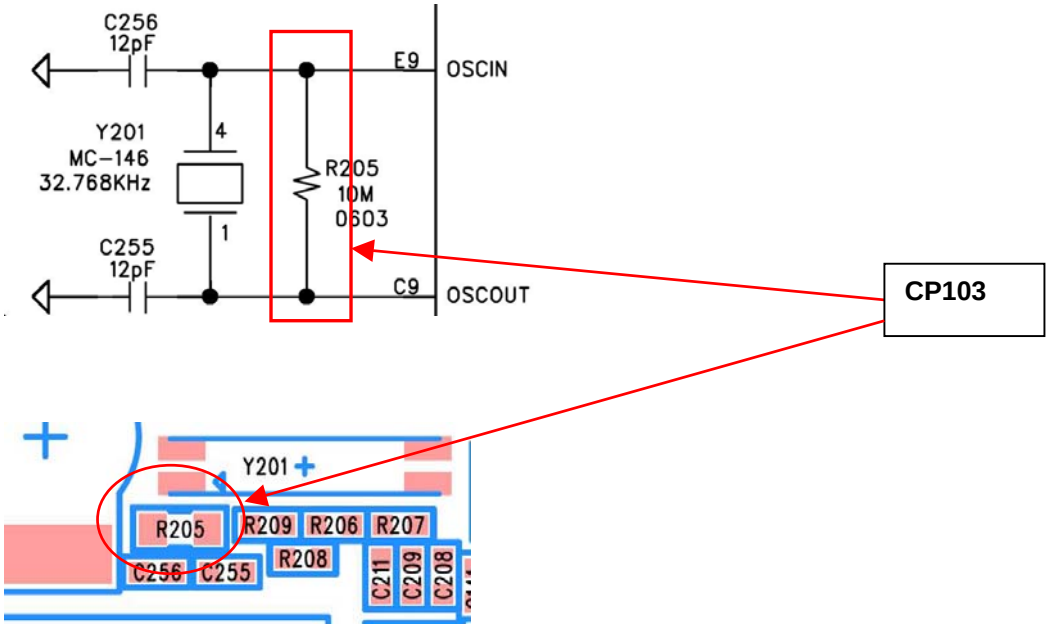
Pressing “END” key to turn on equipment.



6.1.2 Oscillation CHECK

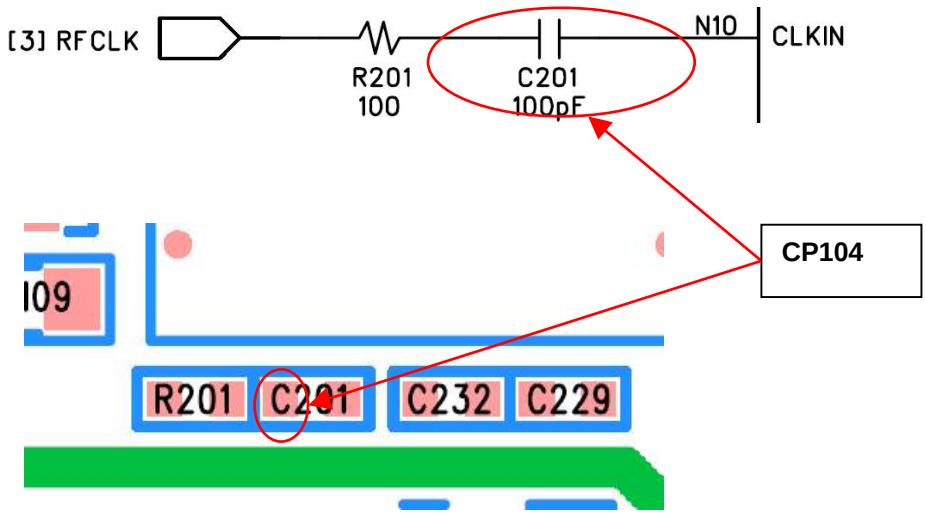
1. Check to see if U201. A3 and B3 pin is oscillated(32.768KHz) : CP103

NO → Check R205 and then replace X1



2. Check to see if U201.N10 and C201 pin Master Clock(26MHz). : CP104

NO → Check C1.2 pin and then check the PCB pattern, soldering



6.1.3 KEYPAD LED Not in Operation

1. Check to see if U121. 6 pin is around 2.8V : CP105

   NO → Check U201.

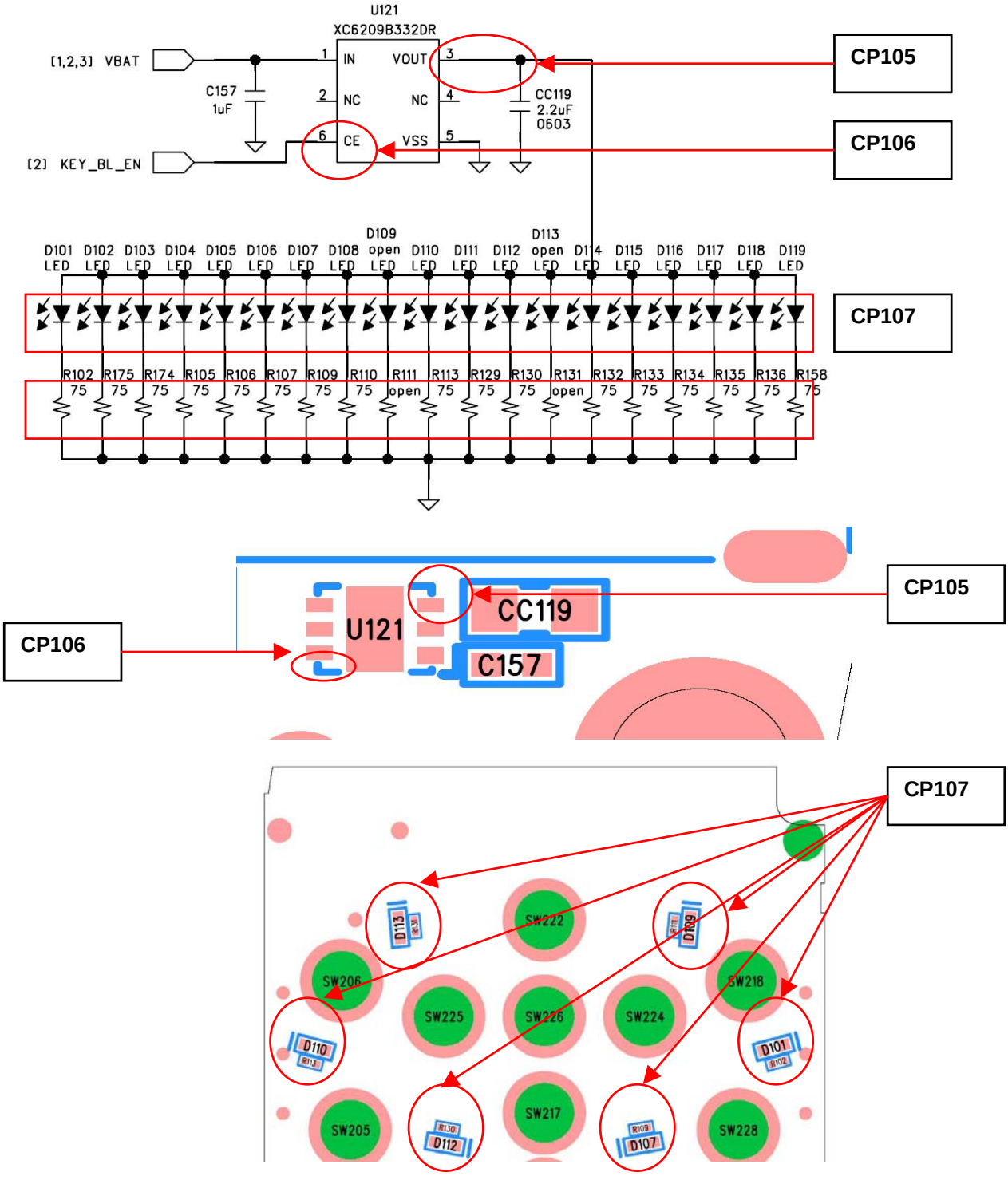
2. Check to see if U121. 3 pin or CC119 are around 3.3V : CP106

   NO → Check to see if U121. 1 pin is around : 3.5V ~ 4.2V .

   NO → Replace U121.

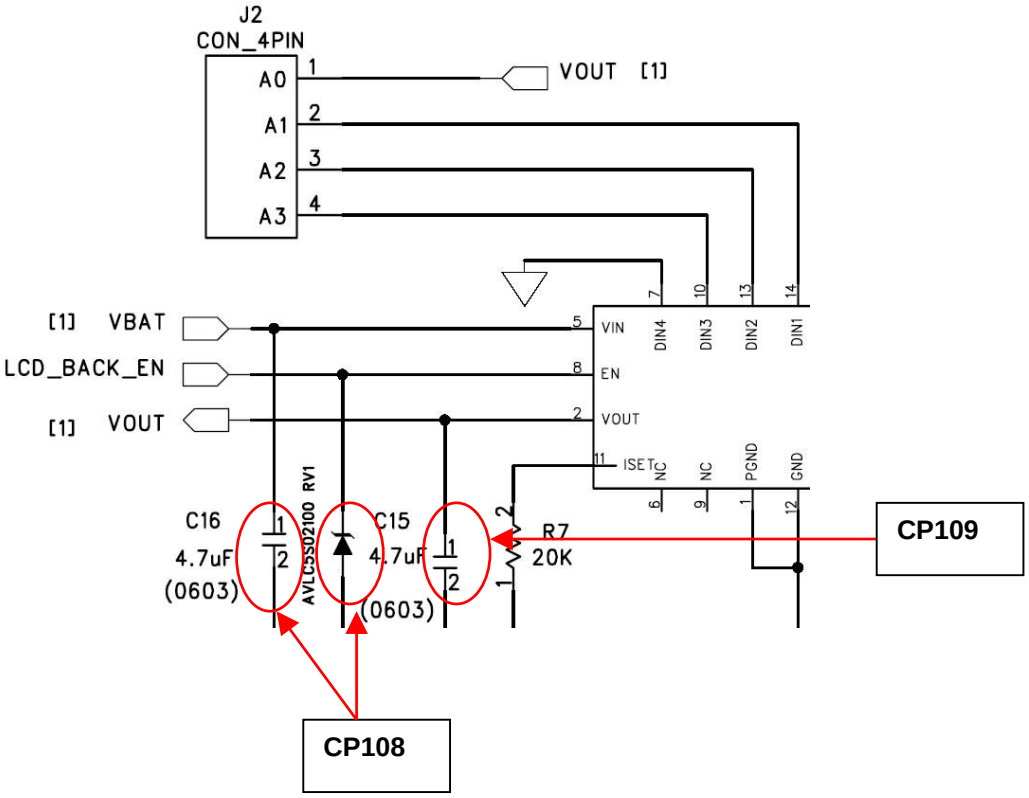
3. Check to see if D101~119 or around resistor are well operated by multimeter : CP107

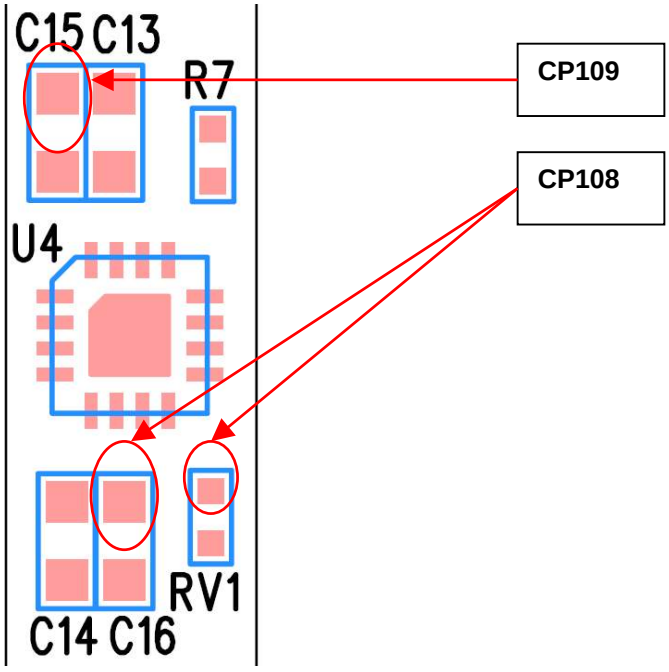
   NO → Replace the LEDs or resistor.



6.1.4 LCD Backlight Not in Operation (White)

1. Check to see if RV1's Voltage (On LCD Module) is 2.8V and
   C16's Voltage (On LCD Module) is 3.5V~4.2V : CP108
   Check to see if RV1's Voltage (On LCD Module) is 4V : CP109
   NO → Replace U4 (On LCD Module)
   Replace LCD Module.

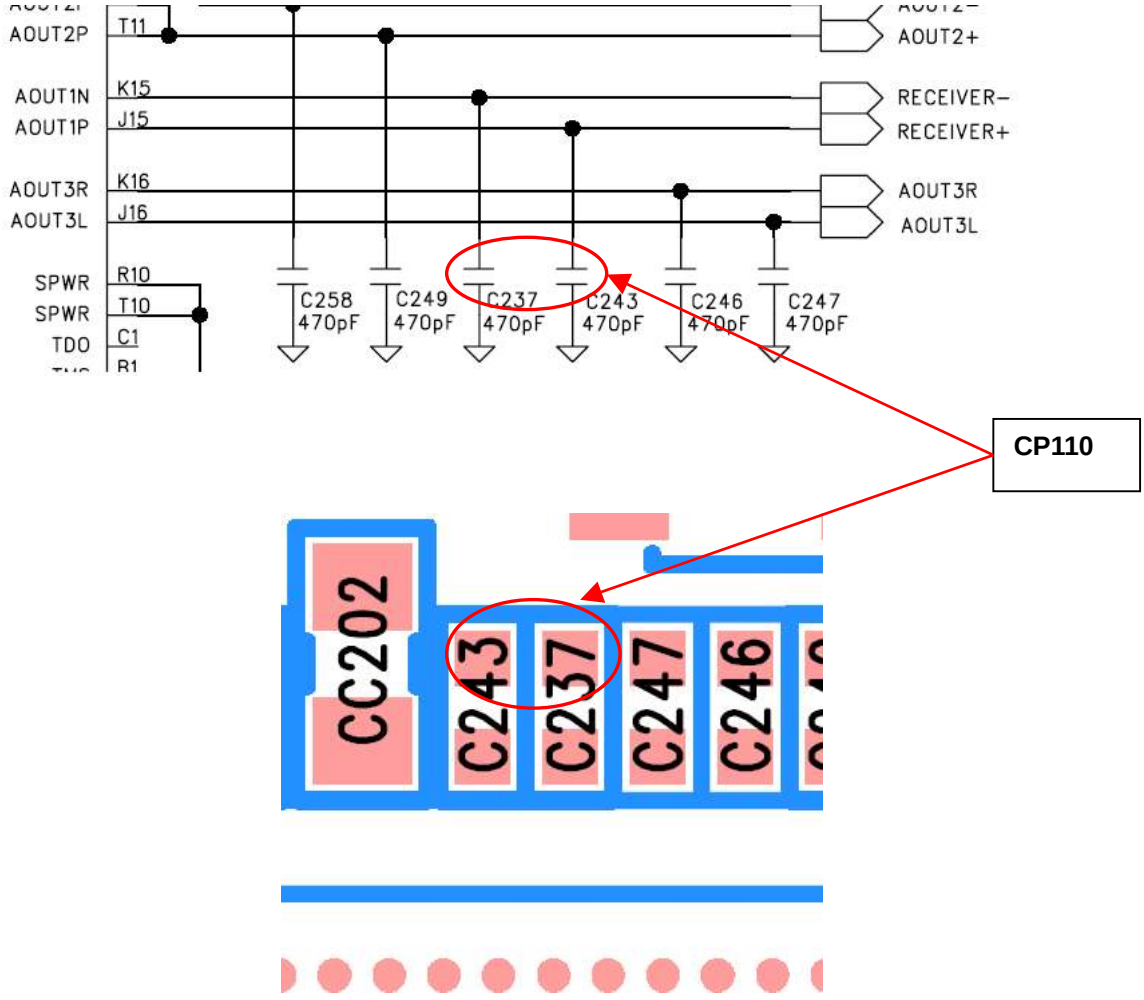




6.2 Audio Part (Earpiece, Speaker, Hands-free Earphone, Microphone, Hands-free Mic)

6.2.1 No receiving tone heard (Ear-piece)

1. Check C243, U202.J15(R219) and K15(R220) pins, C237 (Ear Signal) for waveform : CP110
   NO → Replace U202, and C243, C237.
2. Check to see Earpice and Mani FPCB
   If you find out any defect, you replace them



6.2.2 Melody or MP3 is not ringing

1. Check to see U117.D7, E1, J3 are 1.8V : CP 111

   NO → Check to see U201 or U114 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see L102, U302.C8 pin is Vbatt and C1, E8, H3 pin, CC106 are 2.8V : CP 112

   NO → Check to see U201 and U302 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

3. Check to see U117.E2 pin's input Clock (26MHz) : CP113

   NO → Check to see U116 and U307 cold solder, broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

4. Check to see U117.B6, A65 pin's output and C164, C166 (20 ~ 2000Hz) : CP114

   NO → Check to see U117 cold solder, broken,short to the other PCB pattern or Not.

   If you find out any defect, you replace it

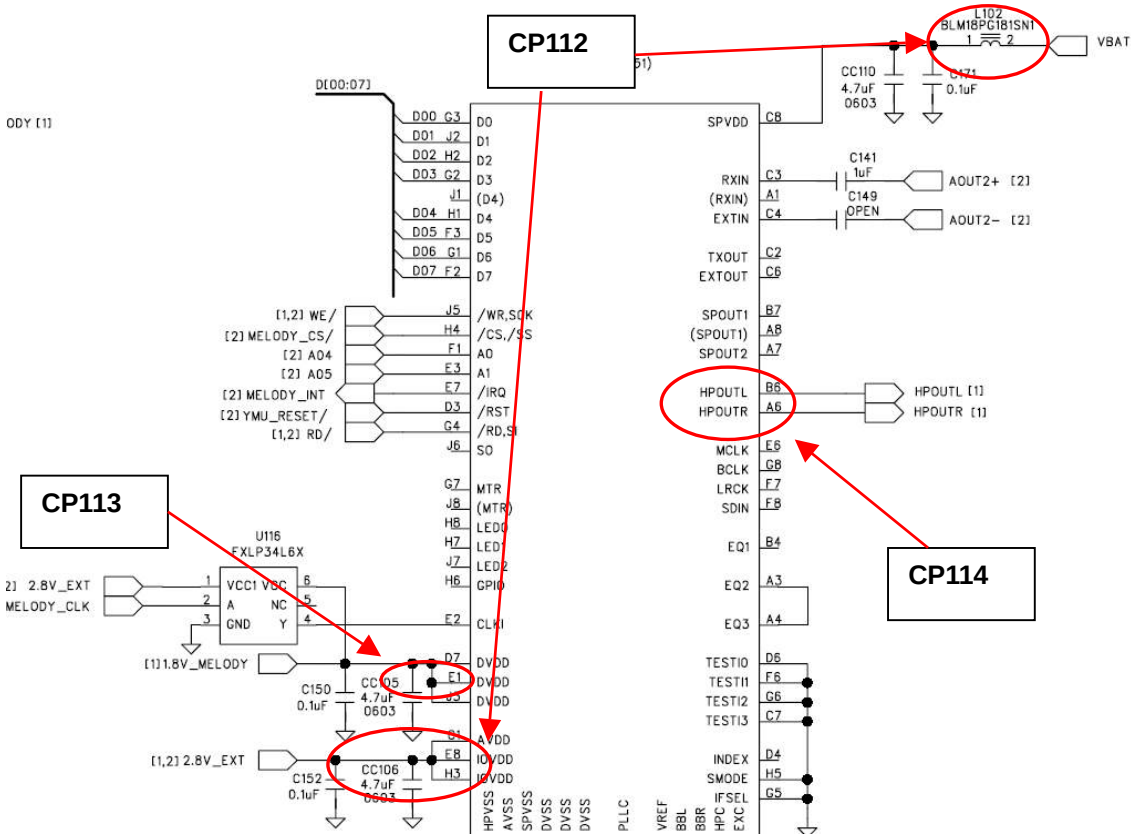
5. Check to see U107 and U108.A1, B3 pin's output (20 ~ 2000Hz) : CP115

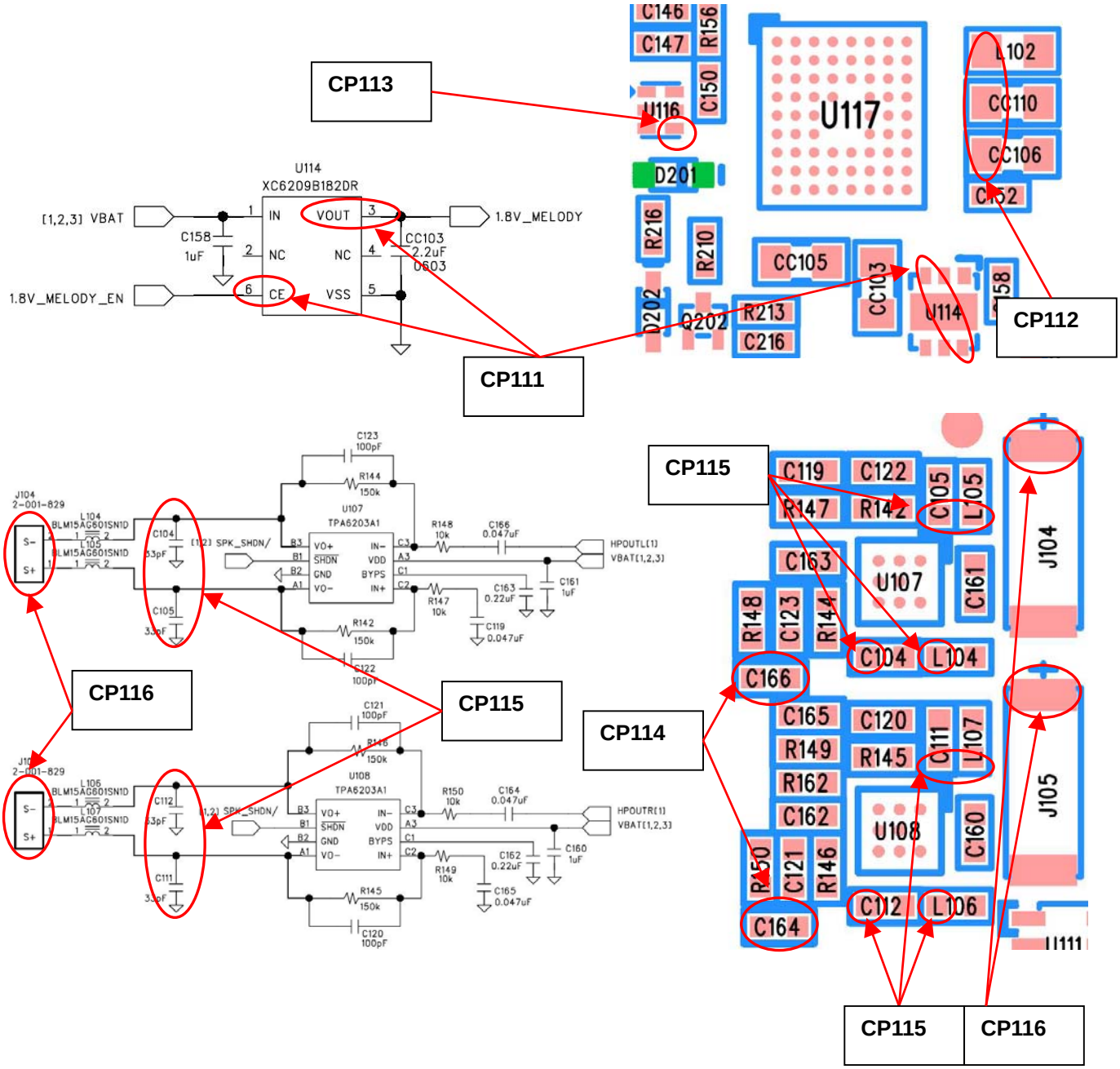
   NO → Check to see U107 and U108 cold solder, broken,short to the other PCB pattern or Not.

   If you find out any defect, you replace it

6. Check to listen to sound : CP116

   NO → Check to see Speaker cold solder, broken,short to the other PCB pattern or Not.




CP113
U114
XC6209B182DR
[1,2,3] VBAT
1.8V_MELODY_EN
1.8V_MELODY
C158
1uF
CC103
2.2uF
0603
IN
VOUT
NC
NC
CE
VSS
CP111
U117
U116
D201
R216
R210
D202
Q202
R213
C216
CC105
CC103
U114
CP112
C146
C147
R156
C150
L102
CC110
CC106
C152
C123
100pF
R144
150k
U107
TPA6203A1
R148
10k
C166
0.047uF
C104
33pF
C105
33pF
[1,2] SPK_SHDN/
HPOUTL[1]
VBAT[1,2,3]
R147
10k
C163
0.22uF
C161
1uF
C119
0.047uF
R142
150k
C122
100pF
CP115
CP116
CP114
C121
100pF
R146
150k
U108
TPA6203A1
R150
10k
C164
0.047uF
C112
33pF
C111
33pF
HPOUTR[1]
VBAT[1,2,3]
R149
10k
C162
0.22uF
C160
1uF
C165
0.047uF
R145
150k
C120
100pF
C119
C122
R147
R142
C105
L105
C163
U107
C161
R148
C123
R144
C104
L104
C166
C165
C120
R149
R145
C111
U107
R162
C162
U108
C160
R150
C121
R146
C112
L106
C164
J104
J105
U111
CP115
CP116

6.2.3 No Receivng tone and melody or MP3 heard (Hands-free Earphone)

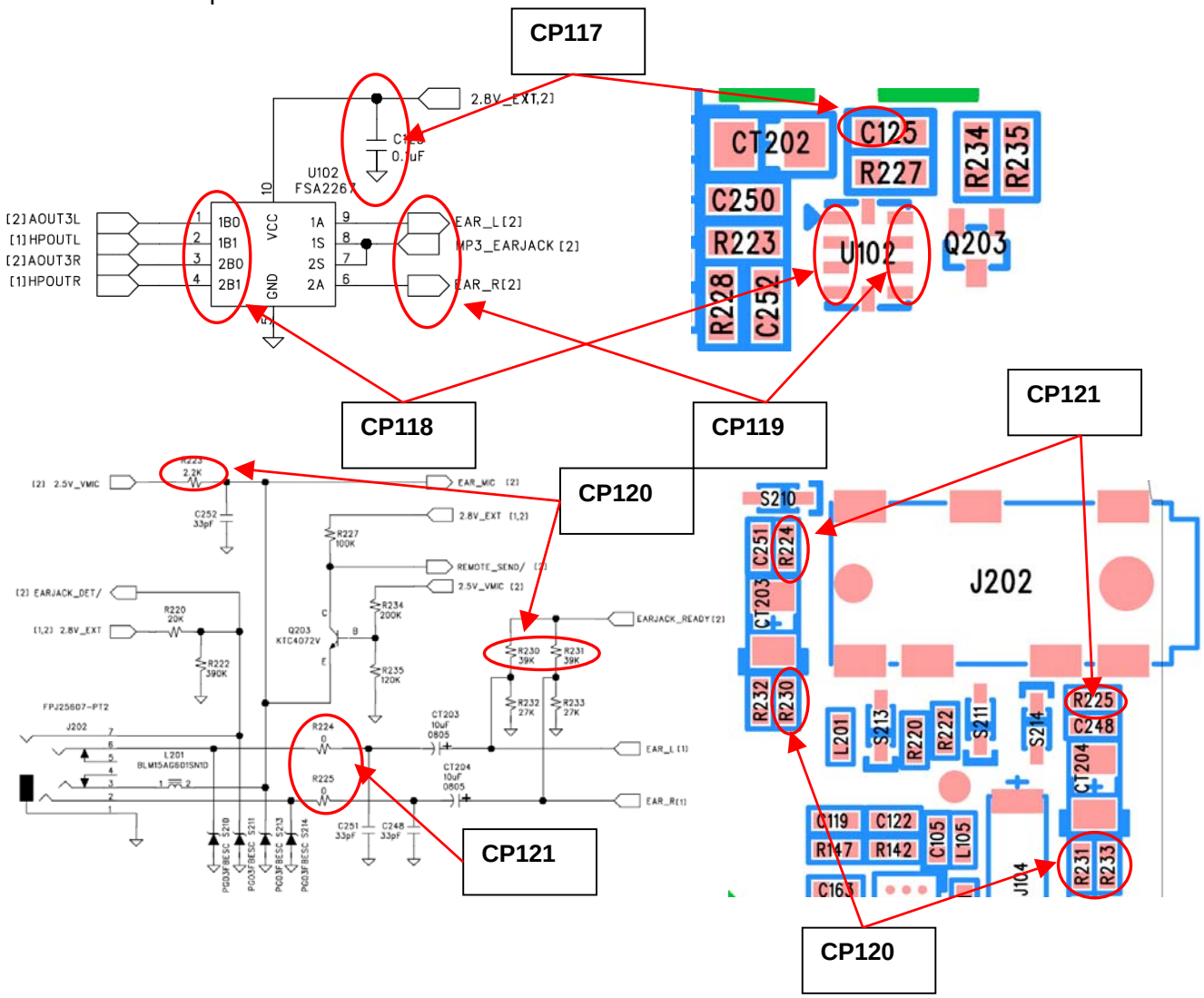
Repeat CP 110 ~ 114

1. Check to see if U102.10 and C125 pins are 2.8V : CP117
2. Check U102.1, 2, 3, 4 pin for waveform : CP118

   NO → Check that U201 or U117 is cold solder, broken, short to the other PCB pattern or not.
3. Check U102.5, 9 pin for waveform : CP119

   NO → Check that U102 is cold solder, broken, short to the other PCB pattern or not.
4. Check R233 and R230, R231 is around 2.8V : CP120
5. Check R224 and R225 pin for waveform : CP121

   NO → Check that some R and C are cold solder, broken, short to the other PCB pattern or not.



6.2.4 Hook Switch not working

1. Check to see if R227 is 2.8V and Q203.B pin is around 1.56V : CP122

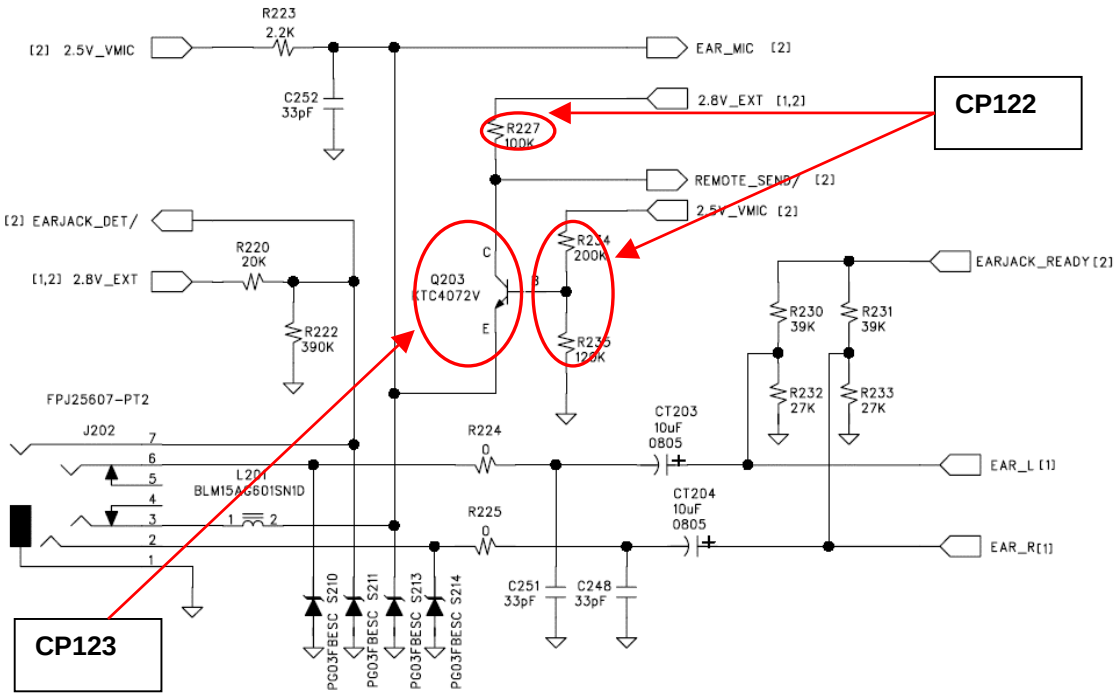
NO → Check that U201, R227, Q203, R234, R235 are cold solder, broken, short to the other PCB pattern or not.

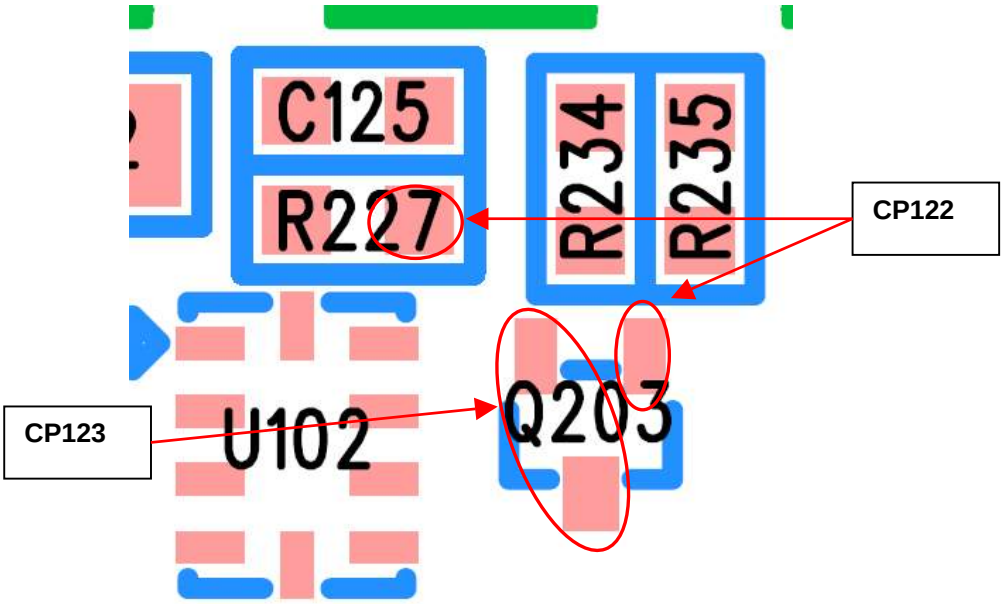
If you find out any defect, you replace it

2. Check to see if Q203 .E and C pin are 0V during pressing Hook Switch : CP123

NO → Check that Q203 is cold solder, broken, short to the other PCB pattern or not

If you find out any defect, you replace it





6.2.5 Side Tone Not transmitted (Mic)

Repeat 6-2-1 No receiving tone heard.(Ear-piece)

1. Check to see if C250, R228 voltage is around 2.5V : CP124
2. Check to see if Mic + pin(S216, C257) is around 1.5V : CP125

NO → Check that S216, C257, C250 and R228 are cold solder, broken, short to the other PCB pattern or not

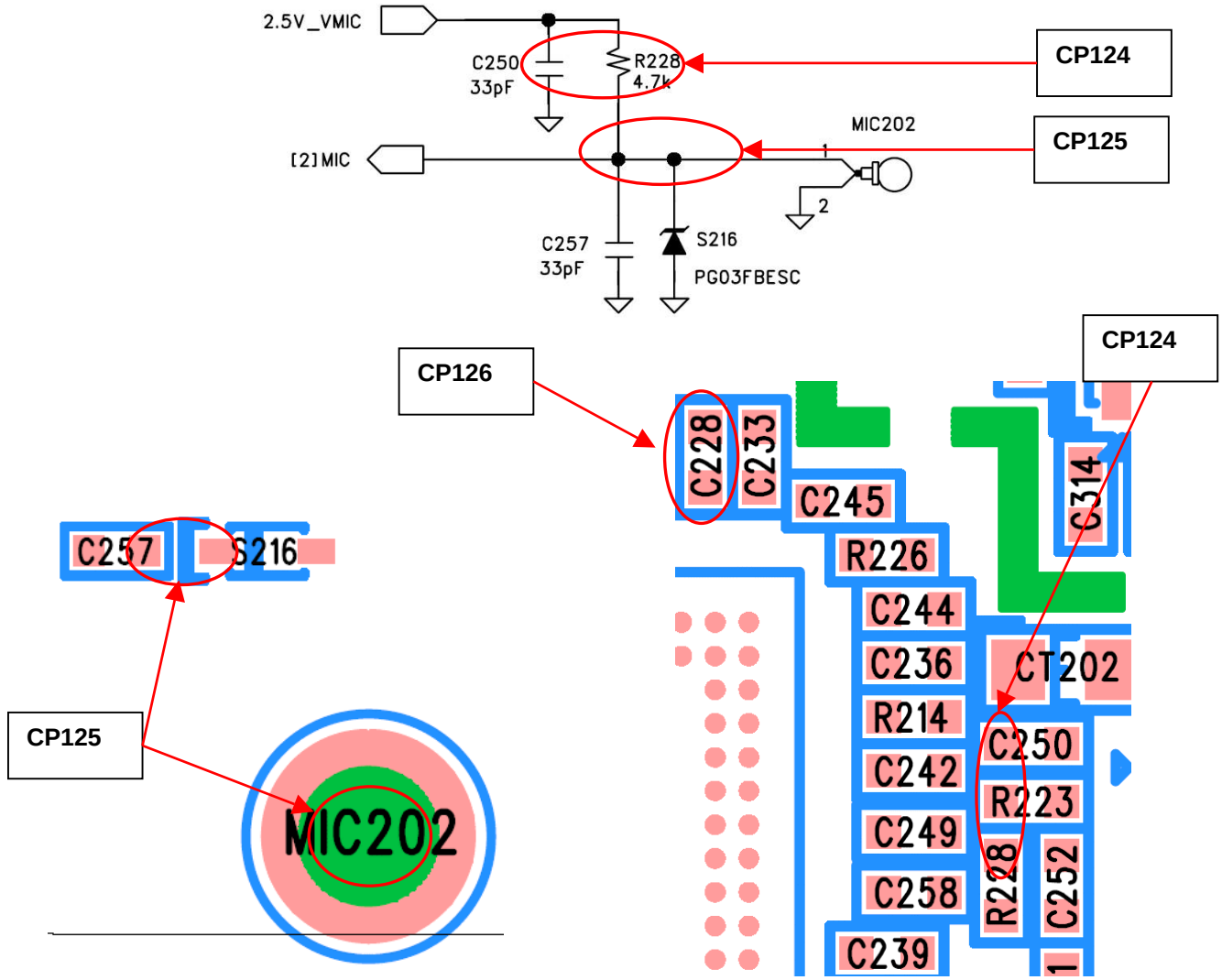
If you find out any defective part, you replace it.

Set to HP8960 to connect a call and tell to mic.

2. Check U201.P16 or C228 pin for wave form : CP126

NO→ Check that U201 is cold solder, broken, short to the other PCB pattern or not or Replace MIC

If you find out any defective part, you replace it.



6.2.6 Side Tone Not transmitted (Hands-free Mic)

Repeat 6-2-2 No receiving tone heard.(Hands-free Earphone).

1. Check that if R223 and C252 pin's voltage is around 1.77V when the hands-set is connected:

   CP127 (If the hands-set is not connected that Voltage is around 0V.)

   NO → Check to see U202.N16 or R223, C252 cold solder, broken, short to the other PCB pattern or not.

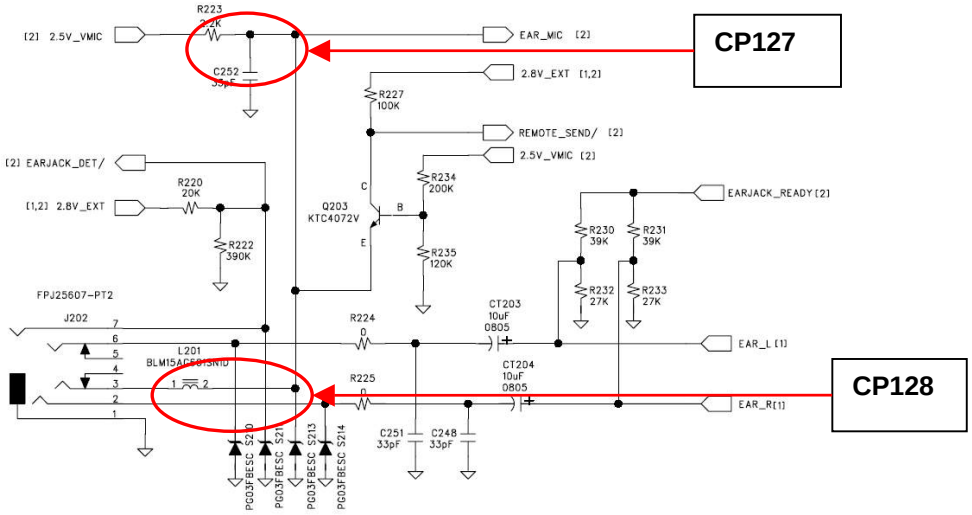
   If you find out any defective part, you replace it.

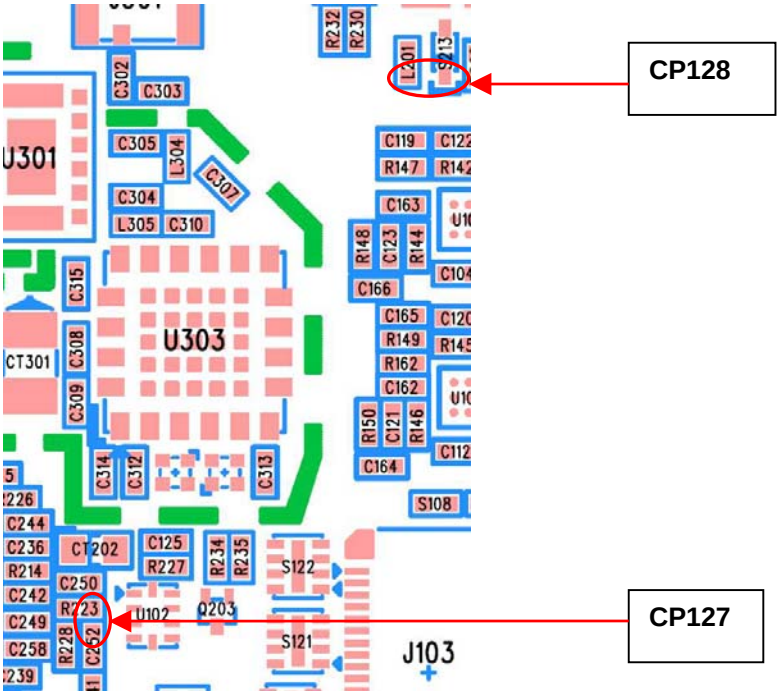
Set to HP8960 to connect a call and tell to Hands-free mic.

2. Check to seeL201 and S213 pins for wave form : CP128

   NO→ Check that U201 or L201 are cold solder, broken, short to the other PCB pattern or not or Replace MIC

   If you find out any defective part, you replace it.





6.2.7 Vibrator not working

1. Check to see if U111.2 pin is 2.8V : CP129

   NO → Check to see U201

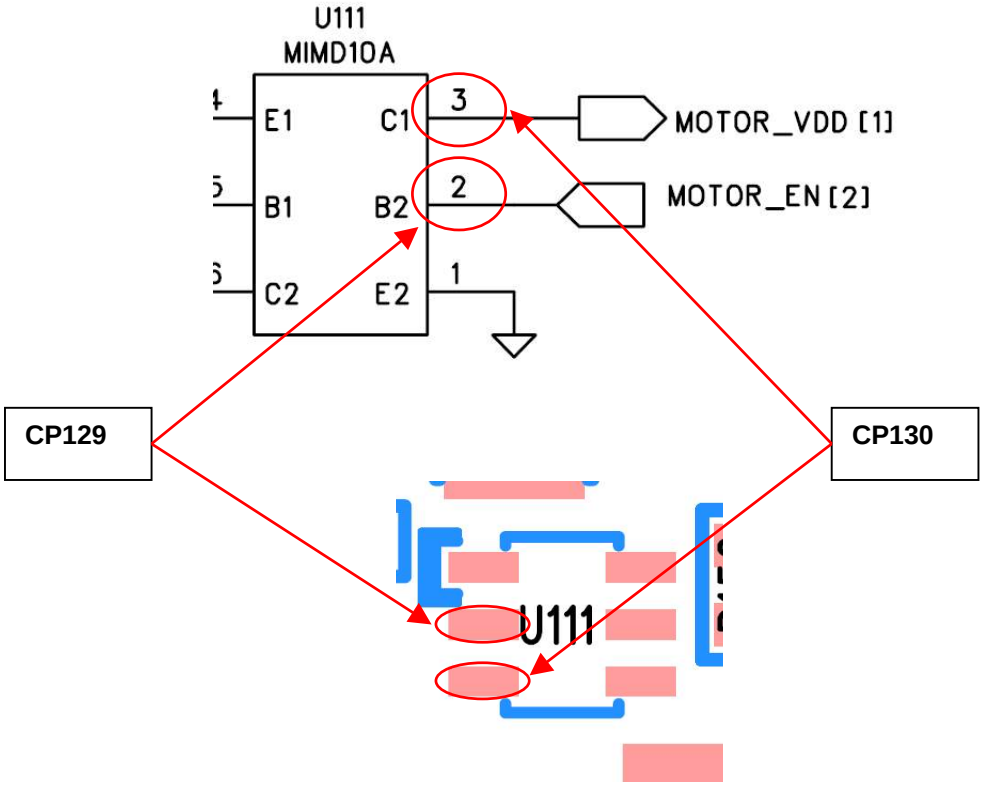
2. Check to see if U111.3 pin is 3.5 ~ 4.2V : CP130

   NO → Check to see U111 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

3. Check to see Vibrator and Mani FPCB

   If you find out any defect, you replace them



6.3 SIM and mini SD memory part

6.3.1 SIM error

1. Check to see if U109.17 pin is around 2.85V : CP131

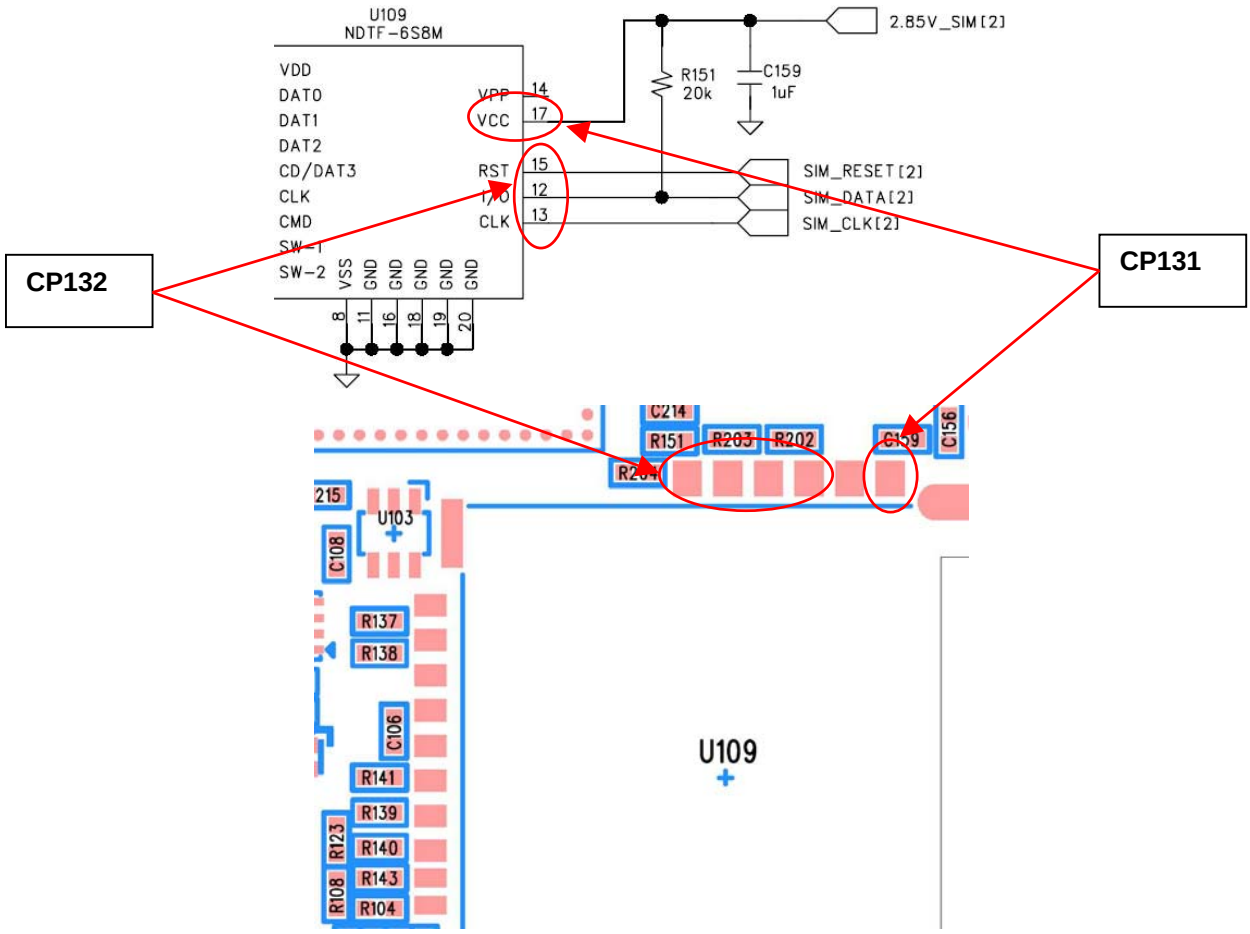
NO → Check to see U202.T6 pin and C239 cold solder, broken, short to the other PCB pattern or not.

If you find out any defect, you replace it

2.Check to see U109.12, 13, and 15 pin for wave form : CP132

NO → Check to see U109 , R151 and C159 cold solder, broken, short to the other PCB pattern or not.

If you find out any defect, you replace it



6.3.2 Mini SD memory error

1. Check to see if J103.6 pin is around 2.8V : CP133

   NO → Check to see U202.B4 and A4 pin cold solder, broken, short to the other PCB pattern or not.

   If you find out any defect, you replace it

2. Check to see if J103.1 pin is around GND : CP134

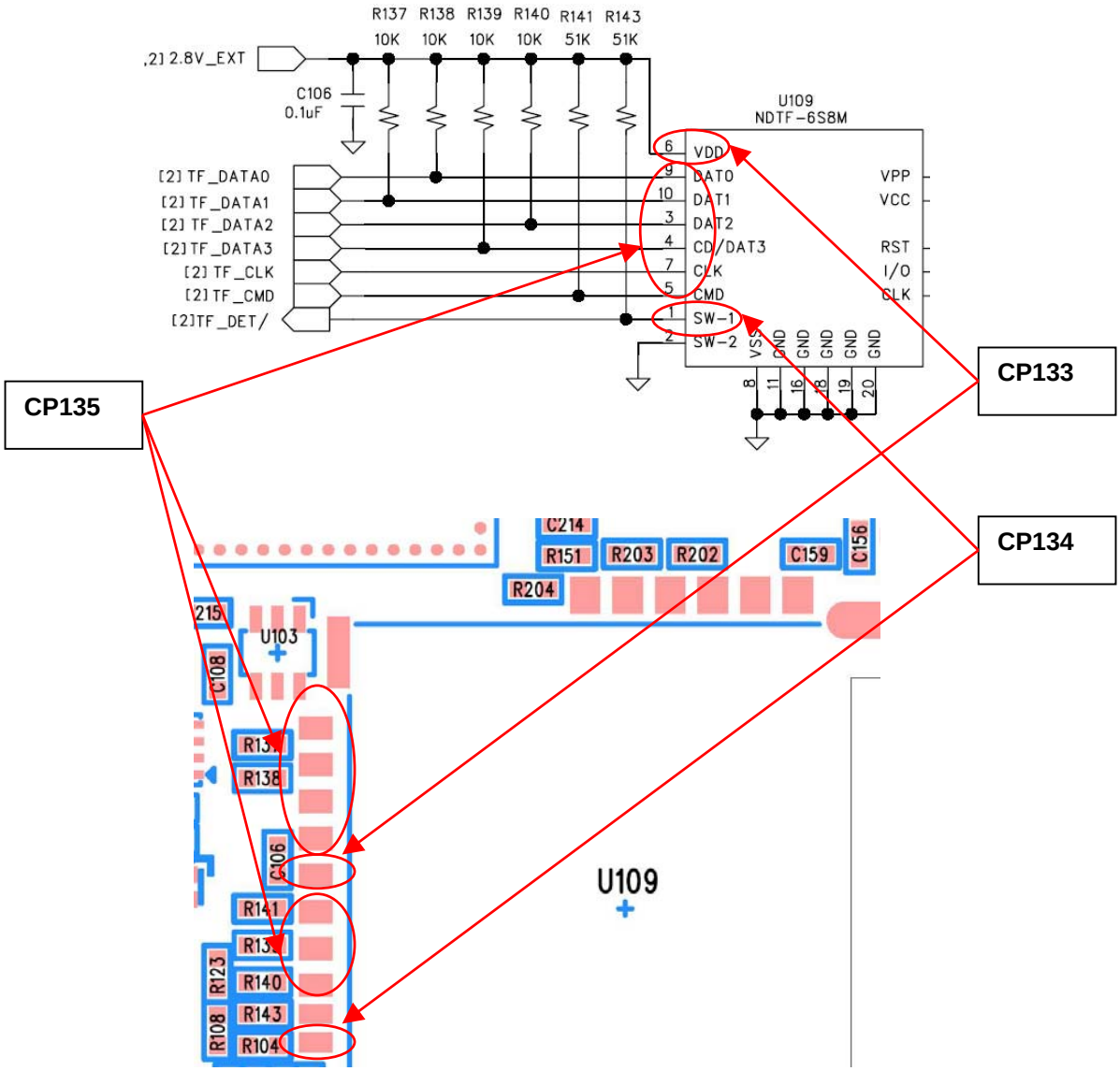
   NO → Check to see U109 and R143 cold solder, broken, short to the other PCB pattern or not.

   If you find out any defect, you replace it

3. Check to see J103.7, 5, 9, 10, 3 and 4 for wave form : CP135

   NO → Check to see U109, R137 , R138, R139, R140, R141 and R143 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it



6.4 Charger part

6.4.1 Charging error

Insert adaptor into I/O jack and Battery.

1. Check to see if Q103.1, 5, 8, 9, 4 and Q201.1, 2 pin are 5.2V : CP136

   NO → Check to see J102.23, 24 pin and Q103 cold solder, broken, short to the other PCB pattern or not.

   If you find out any defect, you replace it.

2. Check to see Q201.3, 4, 7 and 8 are low (0V) : CP137

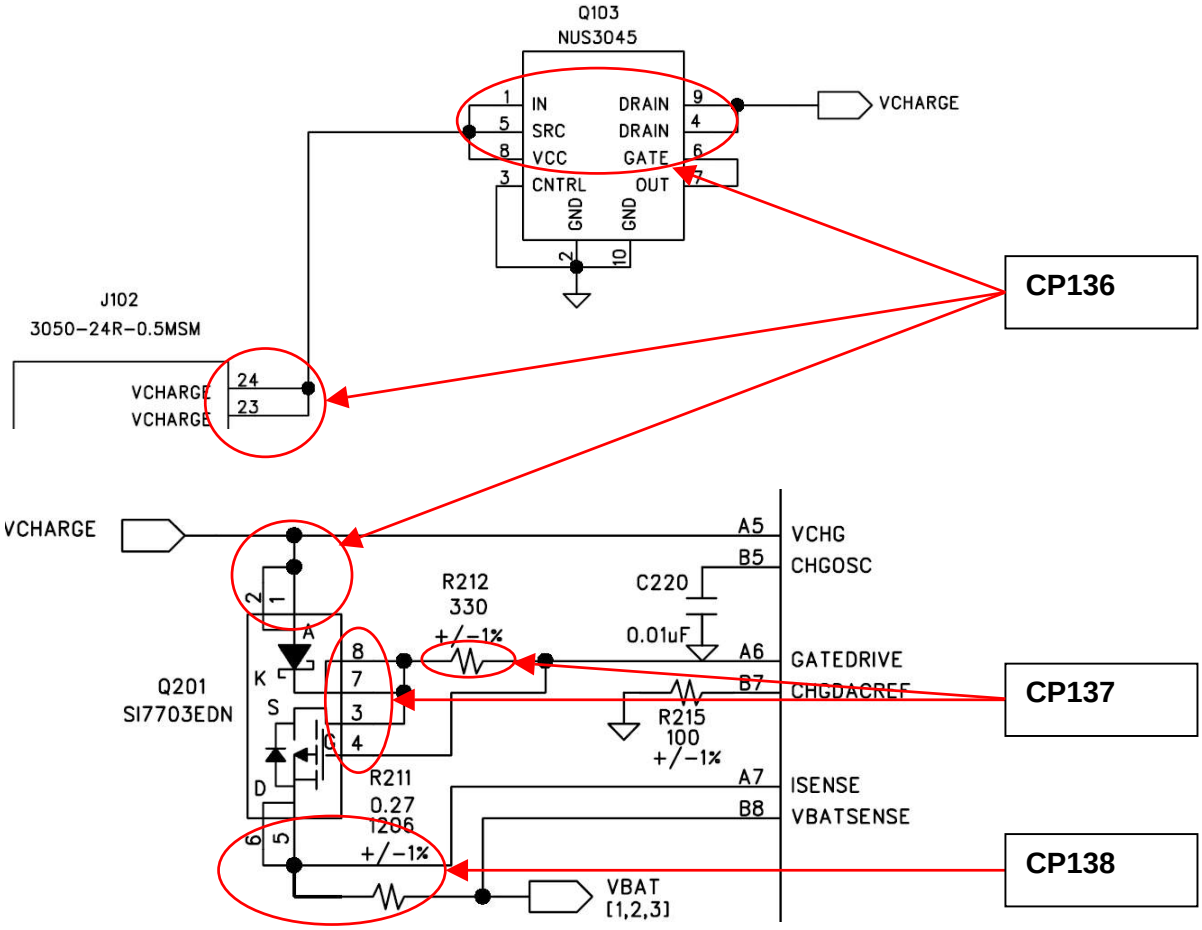
   NO → Check to see U202 and R121 cold solder, broken, short to the other PCB pattern or not

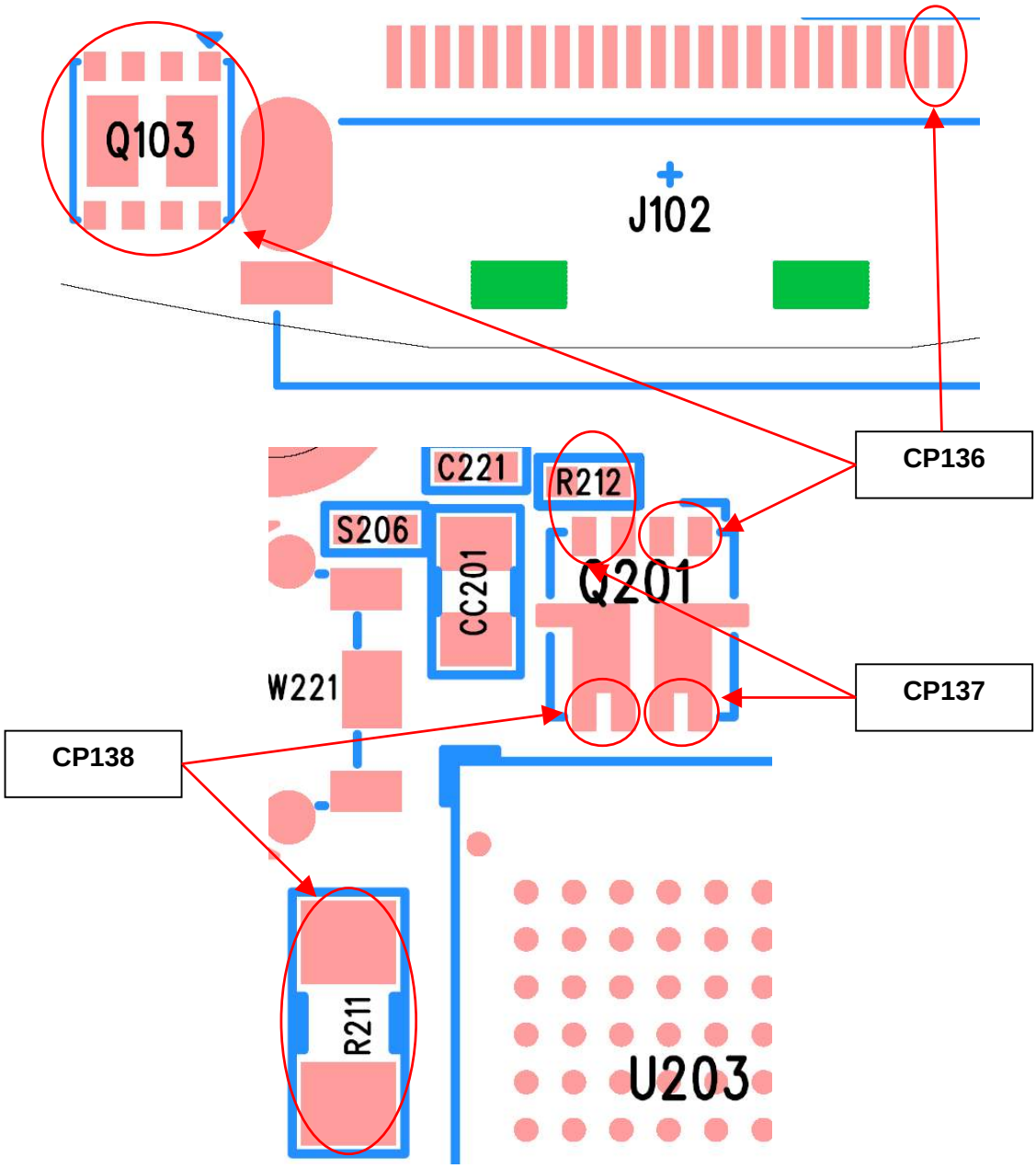
   If you find out any defect, you replace it.

3. Check to see if Q201.5, 6 pin and R211 voltage are 3.5V ~ 4.2 : CP138

   NO → Check to see Q201 and R211 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it.




Q103
J102
CP136
C221
R212
S206
CC201
Q201
W221
CP137
CP138
R211
U203

6.5 Camera Sensor Part

6.5.1 Camera Preview error (All items are On LCD Module)

1. Check to see if J1 and J01 connet correct

   NO → replace the J1 and J01

2. Check to see if U3.6 pin is around 2.8V : CP139

   NO → Check to see U1 cold solder, broken, short to the other PCB pattern or not.

   If you find out any defect, you replace it.

3. Check to see if U3.3 pin and L2 are around 2.8V : CP140

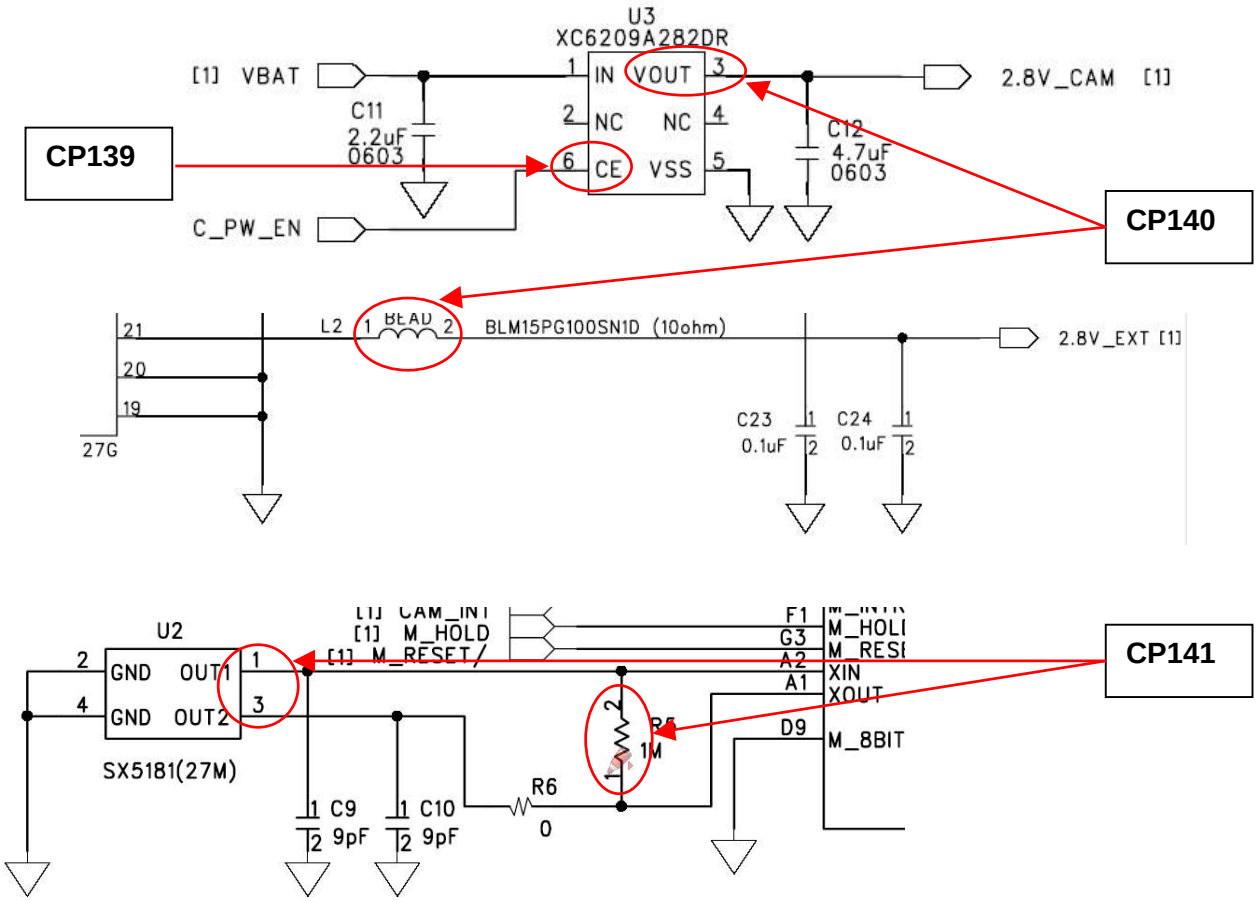
   NO → Check to see U3, L2 and C24 cold solder, broken, short to the other PCB pattern or not.

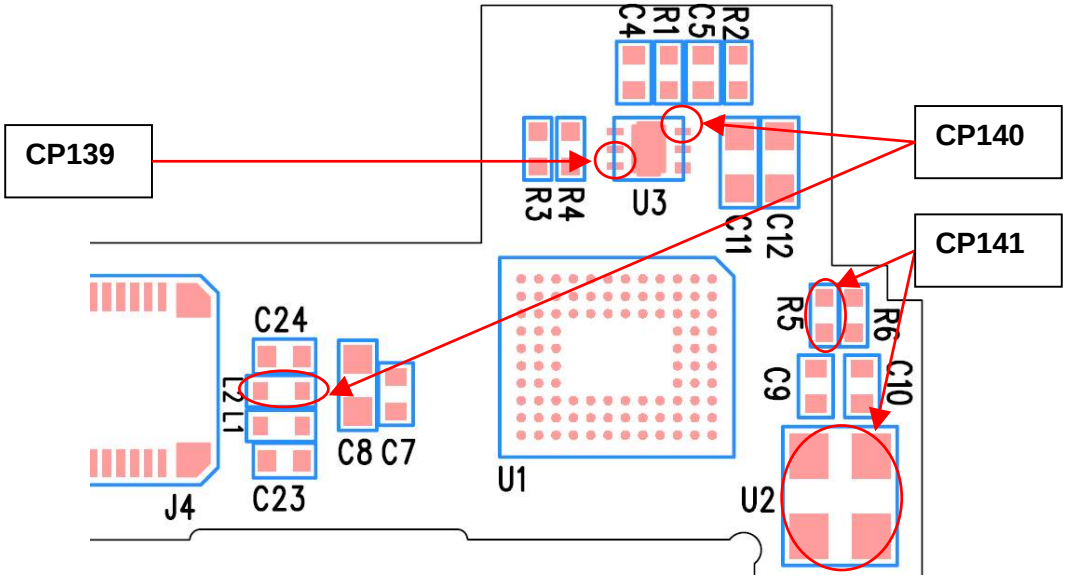
   If you find out any defect, you replace it.

4. Check to see if U2.1, 3 pin is oscillated (27MHz) : CP141

   NO NO → Check to see U2, C9, C10 and R5 cold solder, broken, short to the other PCB pattern or not.

   If you find out any defect, you replace it.




CP139
CP140
CP141
C4
R1
C5
R2
R3
R4
U3
C11
C12
C24
L2
L1
C8
C7
C23
J4
U1
R5
R6
C9
C10
U2

6.6 Bluetooth

1. Check to see U118.6 pin is 2.8V : CP 142

   NO → Check to see U201 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see U118.3 pin and CC109 voltage are 2.8V : CP 143

   NO → Check to see U118 and CC109 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

3. Check To see Audio Gateway is enabled.Check to see if U113.8,9 and U115.8,9 pin are low and U113.2 pin(PCM CLK), U110.4 pin(PCM SYNC) : CP144

   NO → Check to see cold solder, broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

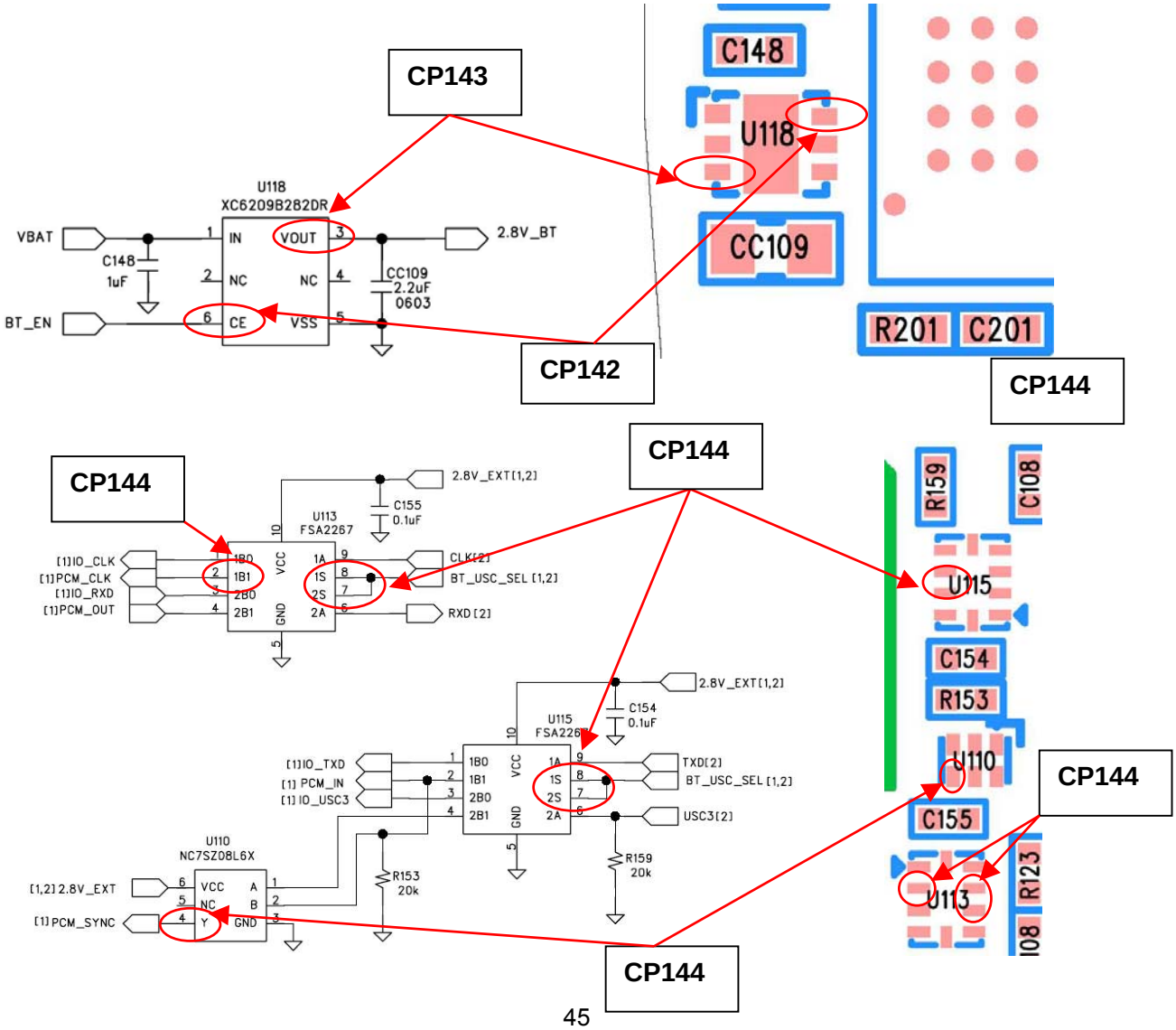
4. Check to see R157 Clock (32.768KHz) : CP145

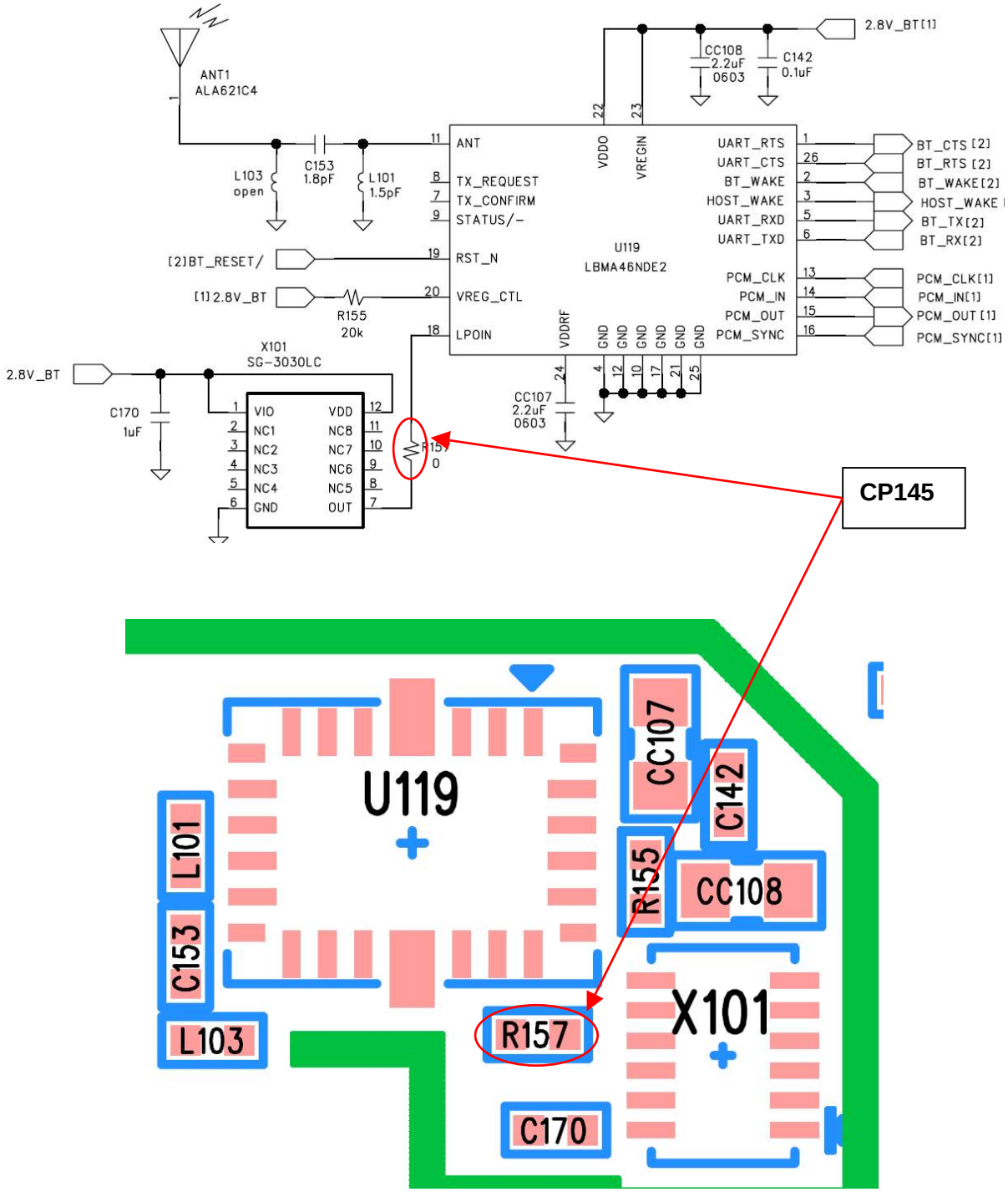
   NO → Check to see X101 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

5. Check to see U119 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it




ANT1
ALA621C4
L103
open
C153
1.8pF
L101
1.5pF
CC108
2.2uF
0603
C142
0.1uF
2.8V_BT[1]
U119
LBMA46NDE2
ANT
TX_REQUEST
TX_CONFIRM
STATUS/-
RST_N
VREG_CTL
LPOIN
VDDO
VREGIN
VDDRF
UART_RTS
UART_CTS
BT_WAKE
HOST_WAKE
UART_RXD
UART_TXD
PCM_CLK
PCM_IN
PCM_OUT
PCM_SYNC
BT_CTS [2]
BT_RTS [2]
BT_WAKE[2]
HOST_WAKE
BT_TX[2]
BT_RX[2]
PCM_CLK[1]
PCM_IN[1]
PCM_OUT [1]
PCM_SYNC[1]
[2]BT_RESET/
[1]2.8V_BT
R155
20k
X101
SG-3030LC
2.8V_BT
C170
1uF
VIO
NC1
NC2
NC3
NC4
GND
VDD
NC8
NC7
NC6
NC5
OUT
R157
0
CC107
2.2uF
0603
CP145
U119
CC107
C142
L101
R155
CC108
C153
X101
L103
R157
C170

6.7 RF Part

6.7.1 Test conditions

1. Test condition 1 : VBAT = 3.8V during all tests

2. Test condition 2 : Traffic channel :GSM850 Band
   Tx mode
   Ch190
   Power Level : 13

3. Test condition 3 : Traffic channel : DCS Band
   Tx mode
   Ch698
   Power Level : 10

4. Test condition 4 : Traffic channel :GSM850 Band
   Rx mode
   Ch190
   Input power : -70dBm

5. Test condition 5 : Traffic channel : DCS Band
   Rx mode
   Ch698
   Input power : -70dBm
6. Test condition 5 : Traffic channel : PCS Band
   Tx mode
   Ch662
   Input power : -70dBm
7. RF power values are measured using 50Ω coaxial cable.

6.7.2 Power Supply Check Point _ TEST CONDITION 1

1. Check to see U302.3 and 5 pin's Voltage are 2.8V : CP 146

   NO → Check to see U201 and U302 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see U307.1 pin's Voltage is around 0.5 ~ 1.5V and U307.4 pin Voltage is 2.75V : CP 147

   NO → Check to see U202 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

3. Check to see U307.3 pin's output Clock (26MHz) : CP148

   NO → Check to see U307 cold solder, broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

4. Check to see C325, C331 and C332 and U306.11, 12, 13, 28, 29 pin's Voltage are 2.8V : CP149

   NO → Check to see U302, C325, C331 and C332 cold solder, broken,short to the other PCB pattern or

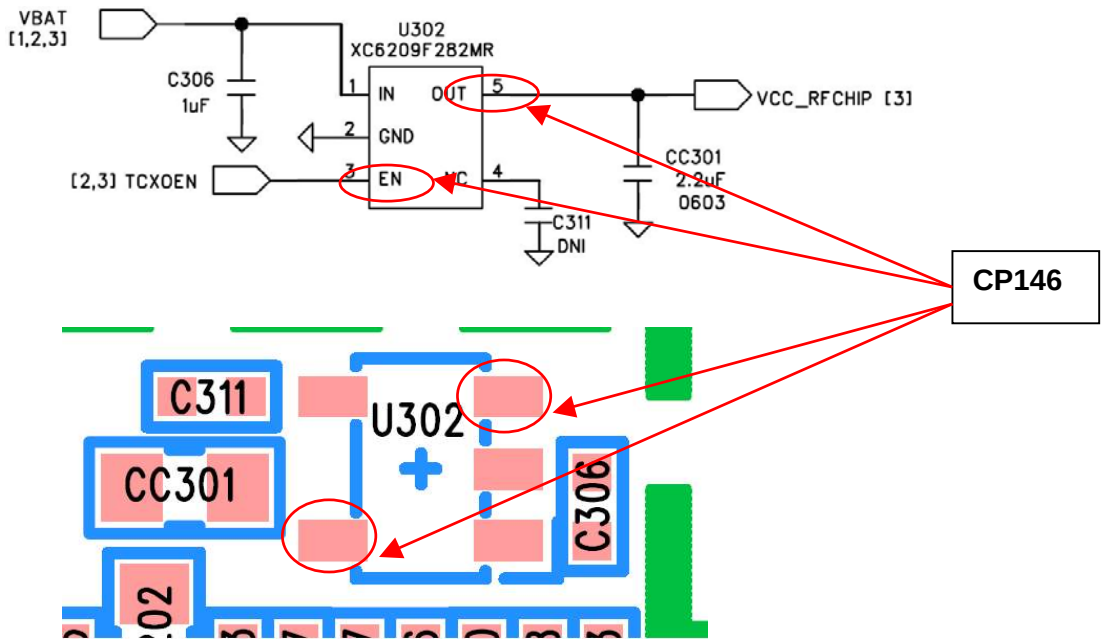
   Not.

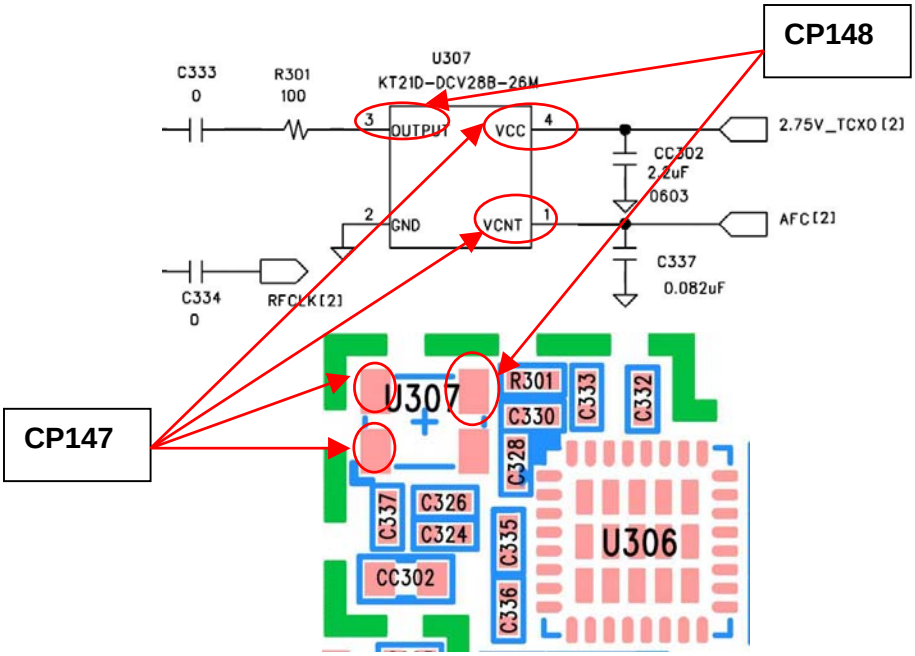
   If you find out any defect, you replace it

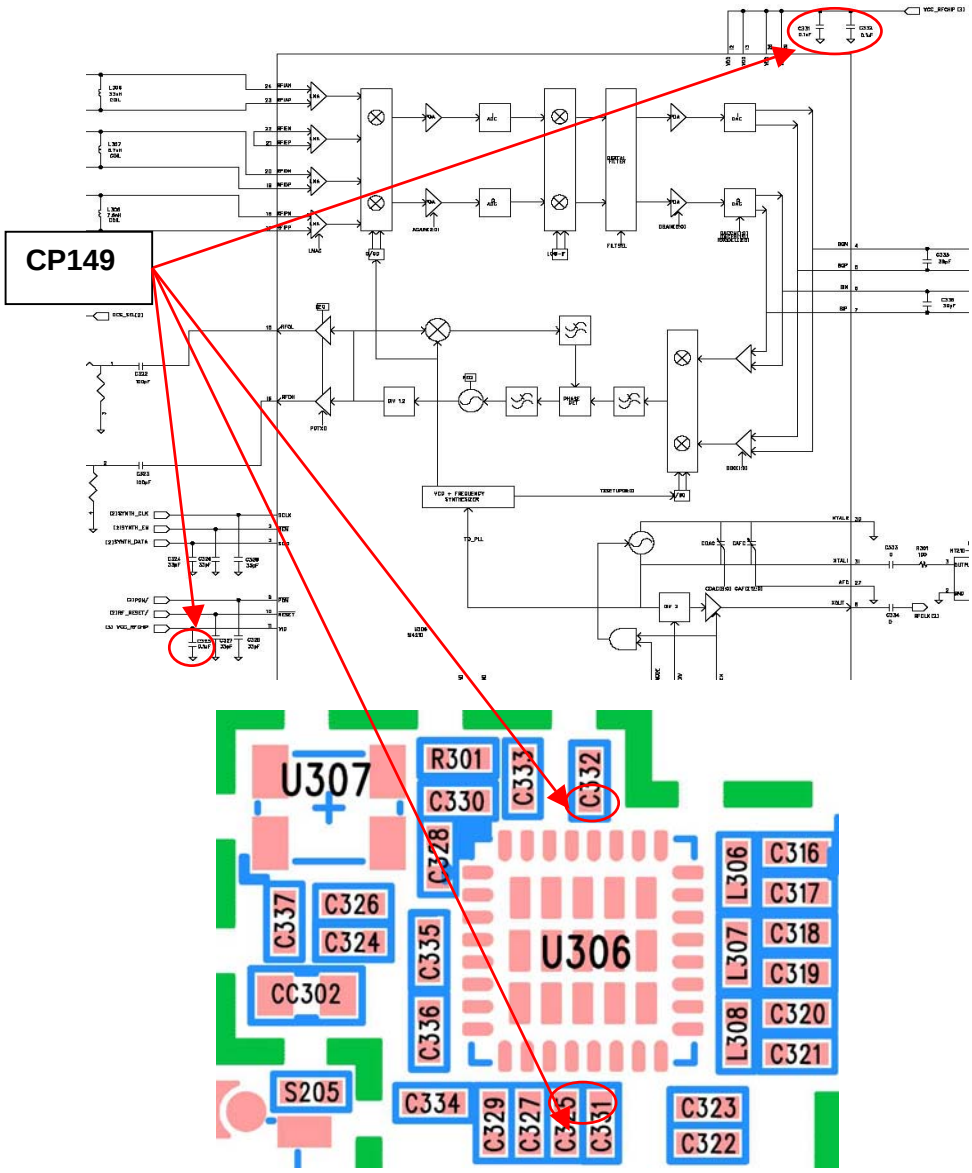
5. Check to see CC301 and U303.2, 6, 17 pin's Voltage are 3.5V ~ 4.2V : CP150

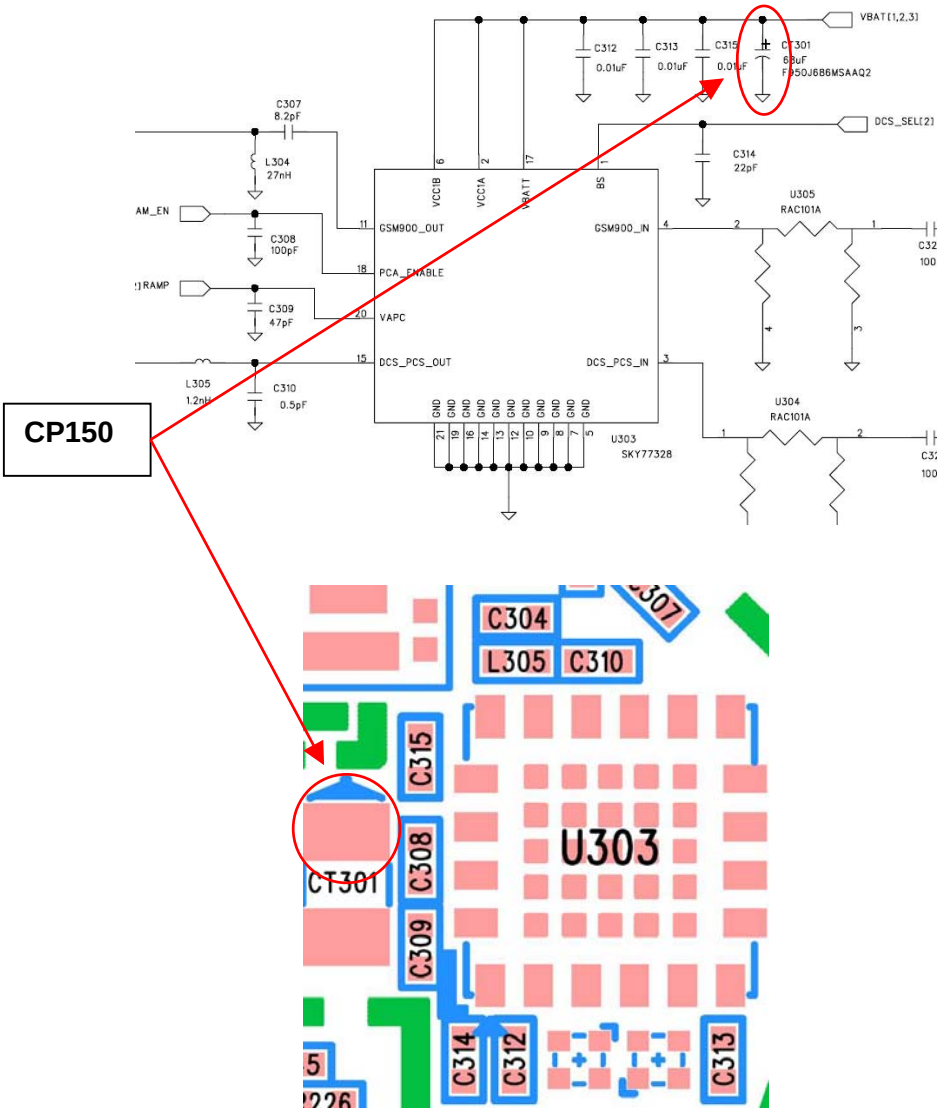
   NO → Check to see CC301 and U303 cold solder, broken,short to the other PCB pattern or not

   If you find out any defect, you replace it




CP148
U307
KT21D-DCV28B-26M
C333
0
R301
100
OUTPUT
VCC
2.75V_TCXO [2]
CC302
2.2uF
0603
GND
VCNT
AFC [2]
C337
0.082uF
C334
0
RFCLK [2]
CP147
U307
R301
C330
C333
C332
C328
C337
C326
C324
C335
U306
CC302
C336


CP149
U307
R301
C330
C333
C332
C328
C337
C326
C324
C335
U306
L306
L307
L308
C316
C317
C318
C319
C320
C321
CC302
C336
S205
C334
C329
C327
C323
C322


CP150
VBAT[1,2,3]
C312
0.01uF
C313
0.01uF
C315
0.01uF
CT301
68uF
F950J686MSAAQ2
DCS_SEL[2]
C314
22pF
C307
8.2pF
L304
27nH
AM_EN
C308
100pF
RAMP
C309
47pF
L305
1.2nH
C310
0.5pF
VCC1B
VCC1A
VBATT
BS
GSM900_OUT
PCA_ENABLE
VAPC
DCS_PCS_OUT
GSM900_IN
DCS_PCS_IN
GND
U303
SKY77328
U305
RAC101A
U304
RAC101A
C304
L305
C310
C315
C308
C309
C314
C312
C313
U303
CT301

6.7.3 RF Transceiver _ TEST CONDITION 2, 3, 4, 5, 6, 7

1. Check to see C333 and U302.31 pin's Clock are 26MHz : CP151

   NO → Check to see U307 and U302 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see C324, C326, C238 and U302.1, 2, 3 pin's signal : CP 152

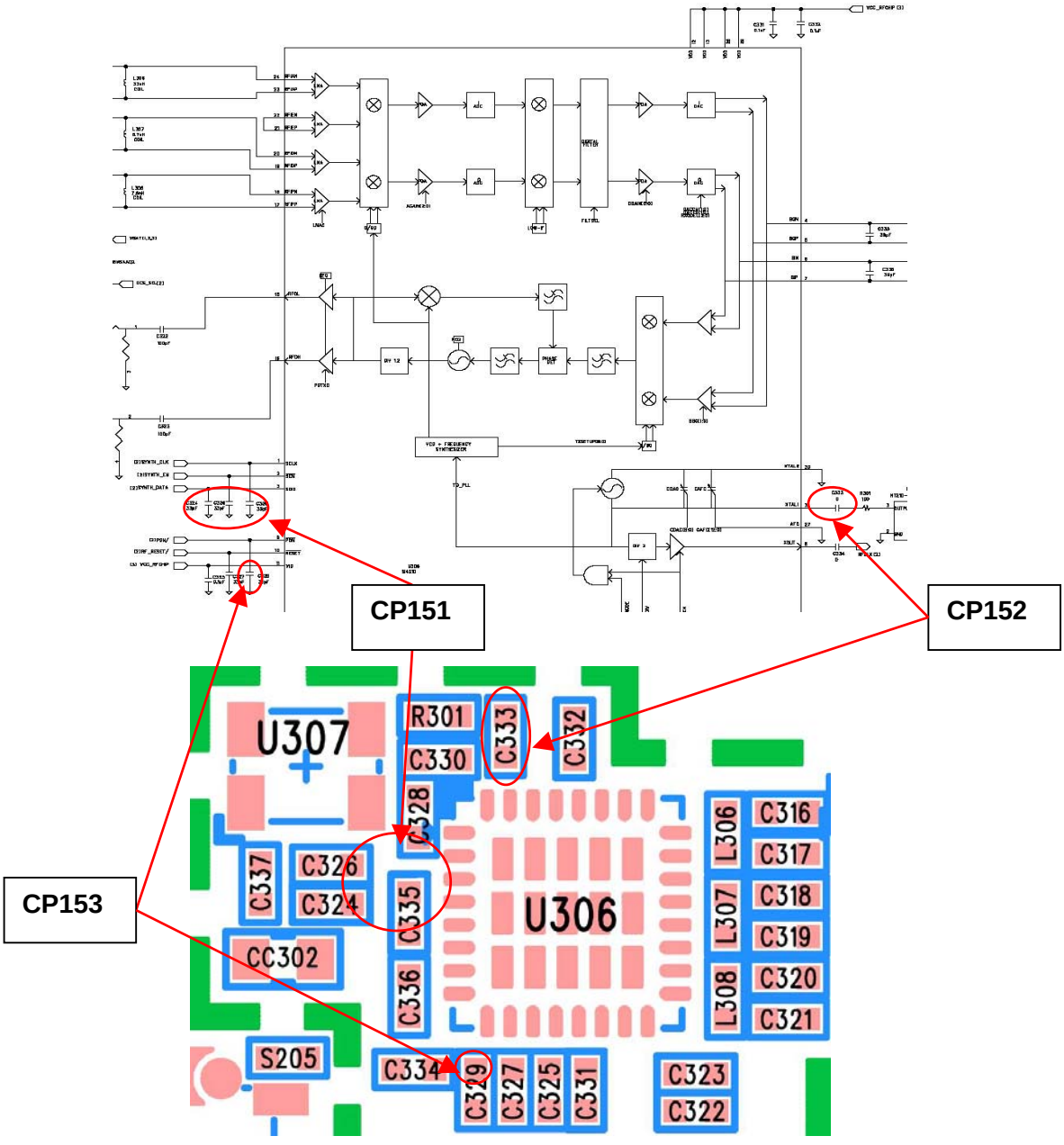
   NO → Check to see U201, U302 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

3. Check to see C329 and U307.9 pin's Voltage is Low (GND) : CP153

   NO → Check to see U201, U302 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it



6.7.4 Power Amplifier Module_ TEST CONDITION 2, 3, 4, 5, 6, 7

1. Check to see U303.3 and 4 pin's input power around 3 dBm : CP154

   NO → Check to see U306, U305 and U304 cold solder,broken,short to the other PCB pattern or not

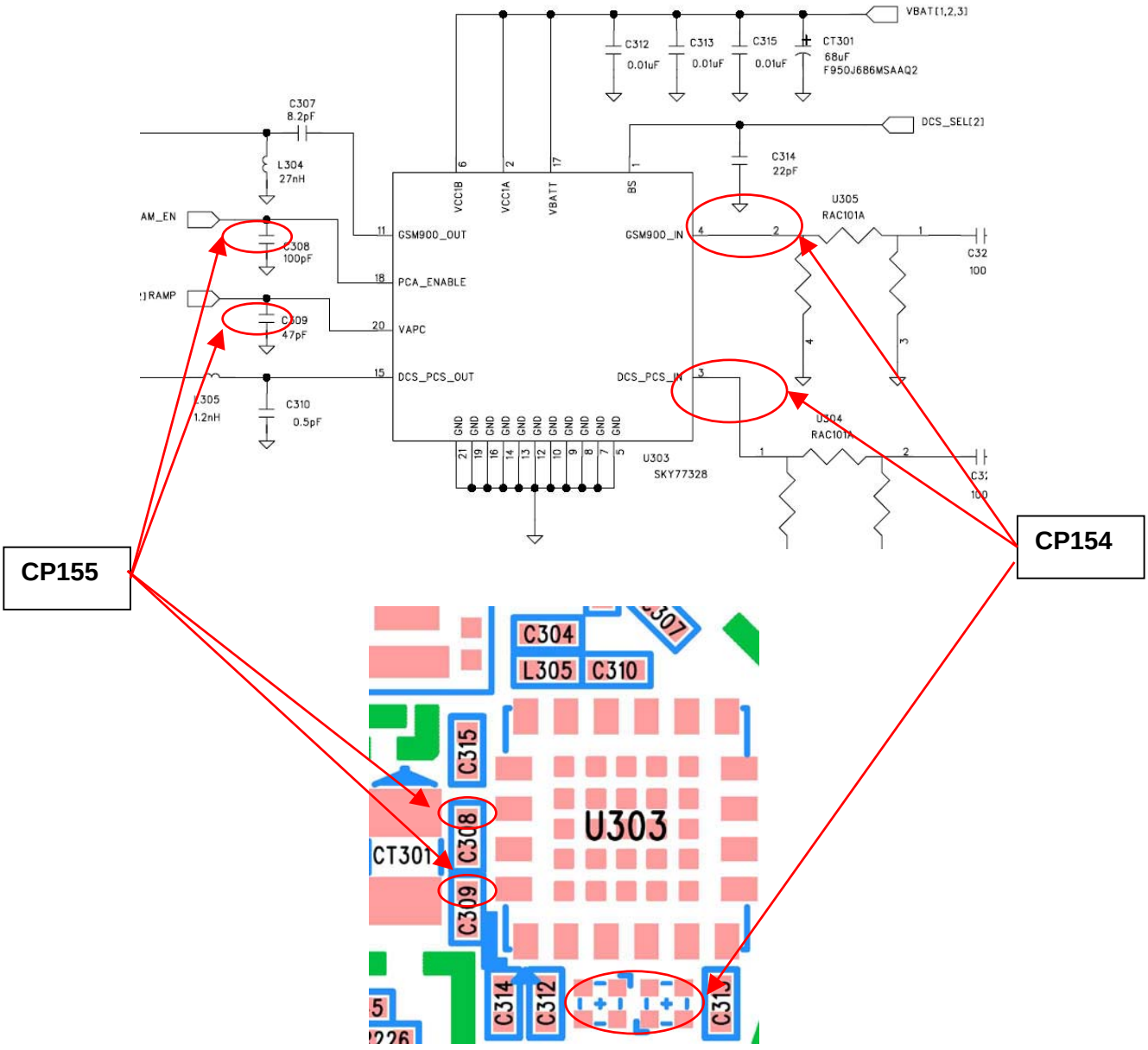
   If you find out any defect, you replace it

2. Check to see C308, U303.18 pin's Voltage (2.8 V) and C309, U303.20 pin Voltage (0~1.3V) : CP 155

   NO → Check to see U201, U303, C308 and C309 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

- C314 and U303.1 pin's voltage are Low(GND), PCS/DCS mode is operating. Else EGSM/GSM850 mode is operating



6.7.5 Antenna Switch Module with SAW Filter _ TEST CONDITION 2, 3, 4, 5, 6, 7

6.7.5.1. **RX Parat**

1. Check to see U301.9 and 11 pin's Voltage are GND : CP 156

   NO → Check to see C304, C305, U201 and U301 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see U301.13 pin's power and one's power of EGSM(U301.1, 2pin), DCS(U301.3,4 pin), PCS(U301.5, 6pin) is same : CP 157

   NO → Check to see U301 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

6.7.5.2. **TX Parat**

1. Check to see U301.9 and 11 pin's Voltage are 2.8V : CP 156

   NO → Check to see C304, C305, U201 and U301 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see U301.13 pin's power is around 30dBm : CP 158

   NO → Check to see U202 cold solder,broken,short to the other PCB pattern or not

   If you find out any defect, you replace it