PANTECH

PG-1210 Service Manual

(GSM Cellular Phone)

Pantech Co., Ltd., Korea

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1st Edition

For Use by Authorized Service/Maintenance Personal Only

Documents to Receive This Addendum:

PG-1210 Maintenance/Repair/Operating Manual

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SECTION 1. Introduction

1.1 An Introduction of GSM Digital Cellular Mobile Communication System

GSM (Global System for Mobile communication) concluded that digital technology working in the Time Division Multiple Access (TDMA) mode would provide the optimum solution for the future system. Specifically , a TDMA system has the following advantage

- ► Offers a possibility of channel splitting and advanced speech coding ,resulting in improved spectrum efficiency.
- ► Offers much greater variety of service than the analog
- ► Allows considerable improvements to be made with regards to the protection of information.

The GSM system is basically designed as a combination of three major subsystem;
The network subsystem, the radio subsystem, and the operation support system.
The functional architecture of a GSM system can be divided into the Mobile Station (MS), the Base Station (BS), and the Network Subsystem (NS). The MS is carried by the subscriber, the BS subsystem controls the radio link with the MS and the NS performs the switching of calls between the mobile and other fixed or mobile network users as well as mobility management. The MS and the BS subsystem communicate across the Um interface also known as radio link
The specifications relating to MS are as follows:

- TS 100 607-1 : Digital cellular telecommunication system(Phase2+)Mobile Station (MS) Conformance specification Part1:Conformance specification

1.2 Frequency Allocation and Its Use

- Transmit frequency band : 824MHz ~ 849MHz(For GSM850) , 1710MHz ~1785MHz(For DCS), 1850MHz ~1910MHz(For PCS)
- Receive frequency band: 869MHz ~ 894MHz(For GSM850), 1805MHz ~ 1880MHz(For DCS), 1930MHz ~ 1990MHz(For PCS)
- Channel spacing : 200 KHz
- ARFCN(Absolute Radio Frequency Channel Number) : 128~251 (For GSM850), 512~885 (For DCS), 512~810 (For PCS)
- Transmit-receive frequency spacing: 45 MHz(For GSM850), 95MHz(For DCS), 80MHz(For PCS)
- Frequency band and Channel Arrangement

For GSM850 Band Fl(n)=824.2+0.2*(n-128) 128 ≤n≤ 251 Fu(n)=Fl(n)+45
824 MHz ~849 MHz : Mobile Transmit,Base receive
869 MHz ~894 MHz : Base Transmit, Mobile receive
For DCS Fl(n)=1710.2+0.2*(n-512) 512≤n≤885 Fu(n)=Fl(n)+95
1710 MHz ~ 1785 MHz : Mobile Transmit,Base receive
1805 MHz ~ 1880 MHz : Base Transmit, Mobile receive
For PCS Band Fl(n)=1850.2+0.2*(n-512) 512 ≤n≤ 810 Fu(n)=Fl(n)+80
1850 MHz ~1910 MHz : Mobile Transmit,Base receive

1930 MHz ~1990 MHz : Base Transmit, Mobile receive
** Fl(n)= frequency value of the carrier , Fu(n)= corresponding frequency value in upper band

1.3 Item Name and Usage

PG-1210, GSM digital cell phone, is a mobile communication terminal for personal use. It has a 850MHz, 1800MHz and 1900MHz frequency band and adopts GSM850, DCS and PCS mode having excellent spectrum efficiency, economy, and portability.

This product is GSM Cellular type portable phone, adopting 1-cell Li-ion battery and power saving circuit to maximize its operation time. Also, it is equipped with an internal antenna and its color LCD with font built in enables both Spanish and English text service. And power control(basic feature of GSM), security feature, voice symbol feature, and variable data rate feature are used appropriately to ensure its best performance. This product consists of a handset, battery pack, and travel charger.

1.4 Characteristics

1) All the active devices of PG-1210 are made of semiconductors to ensure excellent performance and semi-permanent use.

2) Surface mounting device (SMD) is used to ensure high reliability, compactness and lightness.

3) PG-1210 adopts the Silab's Aero II RF transceiver, which is a complete RF front end for multi-band GSM and GPRS wireless communications.

4) PG-1210 is designed to perform excellently even in the worst environment

Section 2. Electrical Specifications

2.1 General GSM850 / DCS / PCS Band

Mobile Transmit Frequency	824MHz~849MHz / 1710MHz ~ 1785MHz / 1850MHz ~1910MHz
Mobile Receive Frequency	869MHz~894MHz / 1805MHz~1880MHz / 1930MHz ~1990MHz
The Number of Time Slot	8
The Number of Channels	124 / 374 / 299
Channel Spacing	200 kHz
Power Supply	Rechargeable Li-Ion Battery 3.7V/730mAH(850mAH)
Operating Temperature	-10℃ ~ +55℃
Dimension	69(H) ×43(W) ×18.35(D) mm (SLIM)
Weight	About 71 g

2.2 Transmitter GSM850 / DCS / PCS Band

Maximum Output Power	33±2 / 30±2 / 30±2dBm
Frequency Error	±90Hz / ±180Hz
Phase Error	RMS < 5°, PEAK < 20°
Minimum Output Power	5±5 / 0±5 / 0±5dBm
Power Control	5~19 / 0~15 / 0~15 (2 dB Step)
Output RF Spectrum	TS 100 910V6.2.0
Switching Transient	TS 100 910V6.2.0
Intermodulation attenuation	
Conducted Spurious Emissions	Idle Mode GSM850 -57dBm 9KHz~824M / 849MHz~1GHz -59dBm 824MHz~849MHz -47dBm 1GHz ~ 12.75GHz DCS -57dBm 9kHz ~ 1GHz -53dBm 1.710GHz ~ 1.785GHz -47dBm 1GHz ~ 1.710GHz / 1.785GHz ~ 12.75GHz PCS -57dbm 9kHz ~ 1GHz -53dBm 1.850GHz ~ 1.910GHz -47dBm 1GHz ~ 1.850GHz / 1.910GHz ~ 12.75GHz
	Allocated Channel -36dBm 9KHz~ 1GHz -30dBm 1GHz~ 12.75GHz

2.3 Receiver

Reference Sensitivity	-102dBm	
For Adjacent interference	C/Ic	9 dB
For Adjacent(200KHz) interference	C/Ia1	-9 dB
For Adjacent(400KHz) interference	C/Ia2	-41 dB
For Adjacent(600KHz) interference	C/Ia3	-49 dB

Section 3 Operation

3.1 Name of each part

3.2 Display(Dual LCD)

Parameter	Projected Actual(MAIN LCD)
Display	Color CSTN LCD with white LED back lighting 1.8” 65k colors Pixels : 128*160 pixels Character : (font size :12/14/16) 8characters x 10lines(max)
Driver	S6B33B9 (SAMSUNG Electronics.)
Module Dimen.	36(W) x 48.2(H) x 5.2(D) mm
Effective Area	27.26(W) x 34.07(H) mm (1.8 inch)
Number of Pixel	128(W) x RGB(W)x 160(H) pixel
Pixel pitch	71(W) x 213(H) um

Parameter	Projected Actual(SUB LCD)
Display	Color CSTN LCD with white LED back lighting 1.0” 65k colors Pixels : 96 x 64 Character : 6characters x 4lines(max)
Module Dimen.	36(W) x 48.2(H) x 5.2(D) mm
Effective Area	22.96(W) x 16.48(H) mm (1.0 inch)
Number of Pixel	96(W) x RGB(W) x 64(H) pixel
Pixel pitch	70(W) x 210(H) um

3.3 Keypad

	Market Goal	Projected Actual	Comments
English Keypad	0-9, *,# Send (Color) End/Pwr (Color) Up, Down, WAP Soft1, Soft2, CLR Camera * Key: Vib. Mode # Key: Auto Lock 0/+Key: international 2 Volume Keys	0-9, *,# Send (Color) End/Pwr (Color) Up, Down, WAP Soft1, Soft2, CLR Camera * Key: Vib. Mode # Key: Auto Lock 0/+ Key: International 2 Volume Keys	Meets Goal. (Industrial design sample required) Meets Goal Keys for VR and Lock International Volume up/down

3.4.Camera Module

Product Name	LT7660FIG-CRT-PG1200/1210 (05P015)
Effective pixel array	640 x 480
Unit Pixel size	3.3um x 3.3um
Module size	7.9mm x 7.9mm x 5.1mm
Operating voltage	2.8V
Weight	0.5g or below

Section 4. Theory of Operation

4.1 Logic Section

4.1.1 DC Distribution and Regulation Part

Applying battery voltage and pressing "END" key on the key pad short-circuits "Ground" and " $\overline{\text{PowerON}}$". AD6537B(U201) control that power manage regarding power on/off in handset Pressing POWERKEY on the key pad is active on the handset.
This will turn on all the LDOs, when $\overline{\text{PowerON}}$ is held low. The power of RF Tx power amplifier is supplied directly by the battery.

4.1.2 Logic part

4.1.2.1 Summary

The logic part consists of AD6527 ARM7 microprocessor-combined DBB(Digital BaseBand) GSM-ASIC, COMBO(flash ROM & SRAM), AD6537B ABB(Analog BaseBand) Chip. AD6527 is GSM-ASIC chipset implemented for GSM terminal's system control and baseband digital signal processing.

Major parts used in the logic part are as follows:

1) AD6527 : U101, [ARM7 Processor Core + DBB GSM Signal Processing] ASIC
2) AD6537B : U201, Analog Baseband Processor (Power management + Voice Codec)
3) COMBO MEMORY(Flash ROM : U509, 256Mbit Flash Memory + 64Mbit SRAM)

4.1.2.2 Baseband Digital Signal Processing

AD6527 is a GSM core device containing ARM7 CPU core. AD6527 is 204 pin LFBGA (mini-BGA) package, consisting of terminal chips. The function and characteristics of clock are as follows:

1) Complete single chip GSM Processor
2) Channel codec sub-system
   - Channel coder and decoder
   - Interleaver and Deinterleaver
   - Encryption and Decryption
3) Control Processor Subsystem including
   - Parallel and serial Display interface
   - Keypad Interface
   - SIM Interface
   - Control of RADIO subsystem
   - Real Time Clock with Alarm

☞ Configuration by Function of AD6527

1 Microprocessor Core

AD6527 has a built-in ARM7 microprocessor core, including microprocessor interrupt controller, timer/counter, and DMA controller. And besides, 32bit data path is included, and up to 8Mbyte addressing is enabled and can be extended up to 16Mbyte. Although external clock should be provided to operate the microprocessor, this core uses 13MHz VCTCXO to provide clock.

2 Input Clock

1) Main Clock(13 MHz):

This is the clock needed for the microprocessor built in AD6527 to operate.

2) VC-TCXO(26 MHz) , 32.768KHz Clock:

This is the system reference clock to control SLEEP mode.

This is the clock derived from 26MHz VC-TCXO clock, provided by RF part. It is the timing reference clock for GSM signal processing.

3 DSP Subsystem

This is a GSM signal processing part in GSM mode, consisting of speech transcoding and Channel equalization as follows:

1) Speech transcoding

In full rate, the DSP receives the speech data stream from VBC and encodes data from 104kbps to 13kbps. Using algorithm is Regular Pulse Excitation with Long Term Prediction (RPE-LTP).

2) Equalization

The Equalizer recovers and demodulates the received signal

The Equalizer establishes local timing and frequency references for mobile terminal as well as RSSI calculation.

The equlization algorithm is a version of Maximum Likelihood Sequency Estimation(MLSI) using Viterbi Algorithm.

☞ GSM Core and RF Interface

1) Transmitter:

AD6537B ABB receive data at 270kbps and use an on chip lock-up table to perform GMSK modulation. A pair of 10bit matched differential DACs convert the modulated data and pass I and Q analog data to the transmit section of the radio system.

2) Receiver:

The receiver I and Q signals are sampled by a pair of ADCs at 270kbps.

The I and Q samples are transferred to the ABB through a dedicated receive path serial port.

4 RF Interface

This interfaces the RF part to control power amplifier, Tx LO buffer amplifier, VC-TCXO, and AGC-end on transmit/receive paths in the RF part.

1) Transmitter Interface:

This sends Ramp_DAC signal to the RF part to control power amplifier.

2) Receiver Interface:

This transmits RX_AGC signal to Rx AGC amp. to adjust receive path gain.

5 General Purpose ADC Support

The AD6537B includes a general purpose 10bit auxiliary ADC with four multiplexed input channel These are used for measurment of battery voltage ID , temperature and accessory ID.

6 USC(Universal System Connector) Interface

A Typical GSM handset requires serial connections to provide data during normal phone operation manufacturing,testing and debugging.

7 General Purpose Interface

The AD6527 provides 32 interface pin for control of peripheral devices.
All GPIO pins start up as inputs. Additional purpose inputs and outputs are available under SW control.

8 Speech Transcoding

In full rate mode, the DSP receive the speech data stream from the ABB and encodes data from 104kbps to 13kbps.Using algorithm is Regular Pulse Exitation with Long Term Prediction as specified GSM Recommandation

9 Power Down Control Section

1) Idle Mode Control:

If IDLE/ signal turns 'Low', transmitter section becomes disabled.

2) Sleep Mode Control:

If IDLE/ and SLEEP/ signals turn 'Low', all the sections except for VC-TCXO circuit become disabled.

3) Receiver & Transmitter Mode Control:

If IDLE/ and SLEEP/ signals turn 'High', all the sections become enabled to perform transmit/receive operation.

4.1.3 Memory Part

Memory consists of COMBO (flash ROM & SRAM).

1 Flash ROM

Flash ROM has a capacity of 256Mbit(32MByte). The main programs of the terminal(call processing, user interface, and diagnostic task) and supplemental programs (NAM program and test program) are stored in the flash ROM. Even if the program version may be changed in the future, customers can download the program.

2 Static RAM

SRAM has a capacity of 64Mbit(8MByte) and stores system parameters, data buffer, and stack of each task in it.

3 Key Tone Generation

All alert signals are generated by the DSP and output to the ABB audio output.

These alert can be used for the earpiece.

4.1.4 Notification Part

The notification of incoming call is given by melody, vibrator.

1) Melody:

   This is a device sounding alert/melody tones.

   The melody datas are stored in flash memory (U509) And generated by Melody IC(U301).

2) Vibrator:

   This is a device enabling vibration. The vibrator data is stored in flash memory(U509)

   And generated by K18(GPIO_3)pin.

4.1.5 Key Pad Part

To enable key operation to input information, the key matrix is configured using strobe signal of KEYPADROW(0-4) and 5 output ports of KEYPADCOL(0-4). Also, to use the key even at light, the backlight circuit is provided for LED 12s.

4.1.6 LCD Module(Display Part)

LCD module consists of LCD, controller, LED-Backlight, Indicator and Vibrator Driver IC.

LCD: 1S/W Icon x 1 lines[(128x3)x160] can be displayed on the LCD panel. 6 icons could be provided by S/W. Controller with English font built in has been used.

LED-backlight Using illuminates the LCD panel, and LCD reflector enhances LCD display effect.

4.1.7 CAMERA Module

Camera Module is activated by keypad sw125.

4.2 Radio Transceiver Section

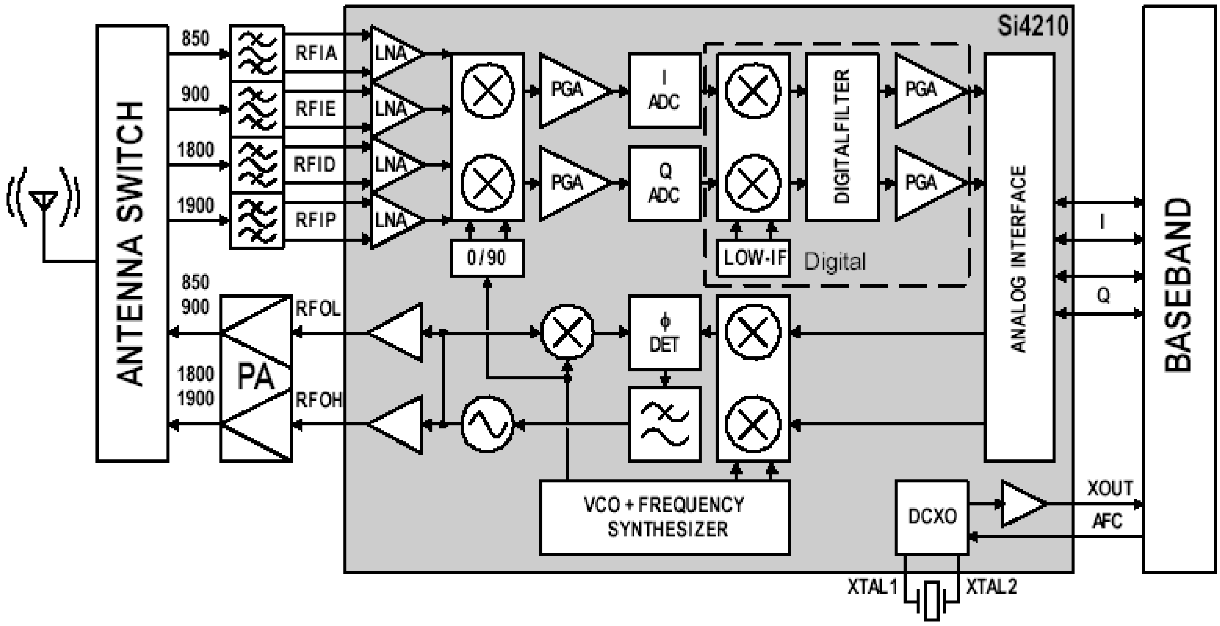


Fig.4-1. RF Transceiver block diagram

The PG-1210's RF Transceiver, which is Aero II, is the industry's most integrated RF front end for multi-band GSM/GPRS digital cellular handsets and wireless data modems. The high-level of integration obtained through patented and proven design architectures, fine line CMOS process technology, and high-performance quad flat no-lead (QFN) technology results in a transceiver solution with industry-leading performance, the smallest form factor, the fewest number of components, the smallest solution footprint, and the lowest bill of materials (BOM) in the industry. A quad-band RF front end using the Aero II transceiver can be implemented with 19 components in less than 1 cm^2 of board area. This level of integration is an enabling force in lowering the cost, simplifying the design and manufacturing, and shrinking the form factor in next-generation GSM/GPRS voice and data terminals. The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering higher performance, lower solution cost, and reduced complexity. The baseband interface is compatible with any supplier's baseband The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifier, and uses an offset phase-locked loop (OPLL) with a The frequency synthesizer uses Silicon Laboratories' proven technology that includes an integrated RF VCO, loop filter, and varactor. The unique integer-N PLL architecture produces a transient response superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. This fast transient response makes the Aero II transceiver well suited to GPRS multi-slot applications where channel switching The analog baseband interface is used with conventional GSM baseband ICs (BBIC). The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface. A standard three-wire serial interface is used to control the transceiver.

While conventional solutions use SiGe, BiCMOS, or other bipolar process technologies, the Aero II transceiver is Silicon Laboratories' third-generation transceiver to be implemented in a 100% CMOS process. Silicon Laboratories' focus on RF and analog mixed-signal CMOS design creates innovation in integration, space savings, and fabrication cost. This further extends the cost savings and extensive manufacturing capacity of CMOS to the GSM/GPRS market.

4.2.1 DC Distribution and Regulation Part

The battery voltage, in return, is applied to the logic part and RF part via LDO(Low Drop-Out) regulator. As several LDO regulators are used, power can be supplied for each necessary part efficiently. Audio/Logic parts use +2.8V. Si4210 RF Transceiver also use +2.8V DC voltage. SKY77325 Power Amplifier (U505) use battery voltage.

4.2.3 Receiver Section

4.2.3.1 An Overview of Receive section

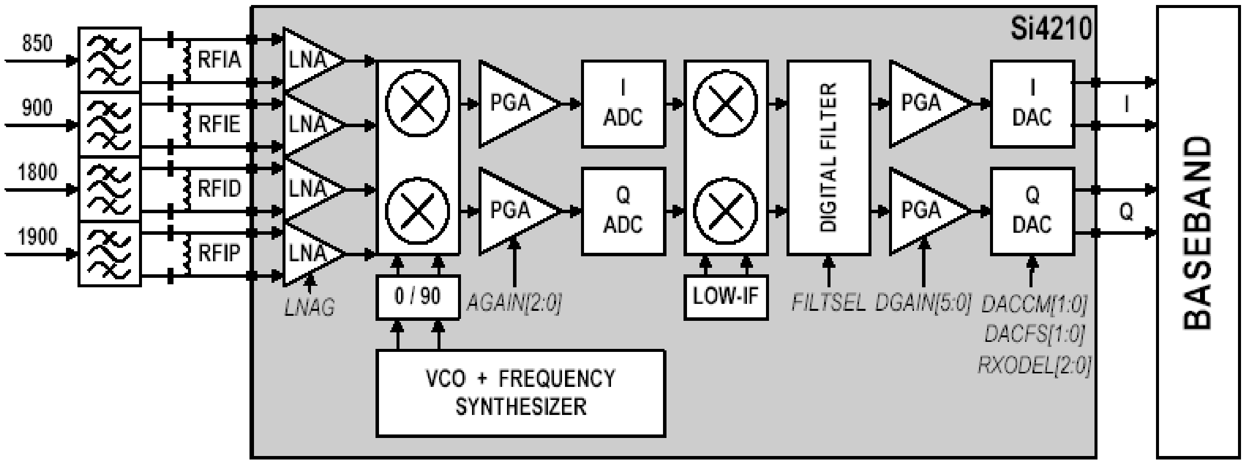


Fig.4-6. Receiver block diagram

The PG-1210's Aero II transceiver uses a digital low-IF receiver architecture that allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters, and the IF SAW filter required in conventional superheterodyne architectures. Compared with direct-conversion architectures, the digital low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, second-order distortion of blockers (AM suppression), and device 1/f noise.

The digital low-IF receiver's immunity to dc offsets has the benefit of expanding part selection and improving manufacturing. At the front end, the common-mode balance requirements on the input SAW filters are relaxed, and the PCB board design is simplified. At the radio's opposite end, the BBIC is one of the handset's largest BOM contributors. It is not uncommon for a direct conversion solution to be compatible only with a BBIC from the same supplier in order to address the complex dc offset issues. However, since the Aero II transceiver has no requirement for BBIC support of complex dc offset compensation, it is able to interface to all of the industry leading baseband ICs.

The receive (RX) section integrates four differentialinput low noise amplifiers (LNAs) supporting the GSM 850 (869–894 MHz), E-GSM 900 (925–960 MHz), DCS 1800 (1805–1880 MHz), and PCS 1900 (1930–1990 MHz) bands. The LNA gain is controlled with the LNAG bit.

A quadrature image-reject mixer downconverts the RF signal to a low intermediate frequency (IF). The mixer output is amplified with an analog programmable gain amplifier (PGA) that is controlled with the AGAIN bits. The quadrature IF signal is digitized with high resolution analog-to-digital converters (ADCs).

The ADC output is downconverted to baseband with a digital quadrature local oscillator signal. Digital decimation and FIR filters perform digital filtering, and remove ADC quantization noise, blockers, and reference interferers. The response of the FIR filter is programmable to a flat passband setting and a linear phase setting. After filtering, the digital output is scaled with a PGA, which is controlled with the DGAIN bits.

The LNAG, AGAIN, and DGAIN register bits should be set to provide a constant amplitude signal to the baseband receive inputs.

Digital-to-analog converters (DACs) drive differential I and Q analog signals onto the BIP, BIN, BQP, and BQN pins to interface to standard analog-input baseband ICs.

The receive DACs are updated at 1.083 MHz and have a first-order reconstruction filter with a 1 MHz bandwidth. No special processing is required in the baseband for dc offset compensation. The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). The common mode level at the receive I and Q outputs is programmable with the DACCM bits, and the fullscale level is programmable with the DACFS bits.

4.2.3.2 Receiver Part

ASM (Antenna Switch Module)

ASM consists of Tx filter, having an antenna port, and dual configuration with the transmitting path isolated from the receiving path. A signal receives from the antenna of frequency band which is 881.5±12.5MHz for GSM850 bands, 1842.5±37.5 MHz for DCS bands, and 1960±30 MHz for PCS bands and transmits it to the saw filter for each band. The Tx filter passes through the output signals of frequency band that is 836.5MHz ±12.5MHz for GSM850 bands, 1747.5±37.5 MHz for DCS bnads, and 1880 ±30 MHz for PCS bands from the power amplifier and transmits it to the antenna. The maximum insertion loss is about 1.5 dB for the receiving bands at 25^{o}C and about 1.5 dB for the transmitting bands at 25^{o}C.

SAW Filter (BPF / Band select filter)

The **F501** filter is for the GSM850 band signals which range 881.5±12.5MHz with low insertion loss. the **F502** filter is for the DCS band signals which range 1842.5±37.5 with low inserton loss.

And **F503** filter passes the PCS bands that cover 1960±30MHz. These filters degrade other band signals with high passing loss of 30~60 dB. The EGSM, DCS, and PCS's maximum insertion loss is 2.6 dB

4.2.4 Transmit Section

4.2.4.1 An Overview of Transmit Section

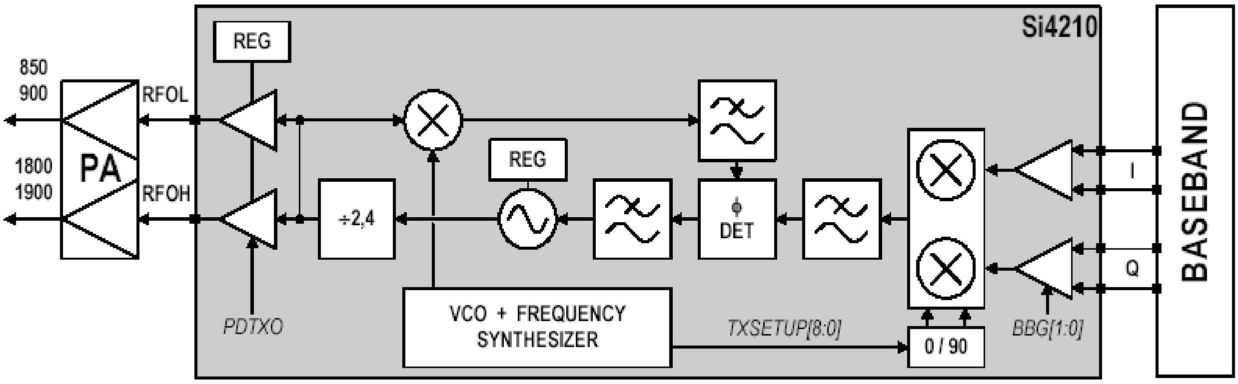


Fig.4-8. Transmitter block diagram

The transmit section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two 50 Ω output buffers that can drive an external power amplifier (PA). One output is for the GSM 850 (824–849 MHz) and E-GSM 900 (880–915 MHz) bands and one output is for the DCS 1800 (1710–1785 MHz) and PCS 1900 (1850–1910 MHz) bands.

The OPLL requires no external filtering to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power. The output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA. Additionally, the TXVCO benefits from isolation provided by the transmit output buffers. This significantly minimizes any load pull effects and eliminates the need for off-chip isolation networks.

A quadrature mixer upconverts the differential in-phase (BIP, BIN) and quadrature (BQP, BQN) baseband signals to an intermediate frequency (IF) that is filtered and which is used as the reference input to the OPLL. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs.

The transmit I/Q interface must have a non-zero input no later than 94 quarter bits after PDN is asserted for proper operation. If the baseband is unable to provide a sufficient TX I/Q non-zero input preamble, then the CWDUR bits can be used to provide a preamble extension.

The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). In transmit mode, the BIP, BIN, BQP, and BQN pins provide the analog I/Q input from the baseband subsystem. The full-scale level at the baseband input pins is programmable with the BBG[1:0] bits. The I and Q signals are automatically swapped within the Aero II transceiver when switching bands. The transmit output path is automatically selected by the ARFCN bits and the BANDIND bits.

4.2.4.2 Transmitter Part

A. 3 dB attenuator

These passive components are adopted for PAM to operate in a stable output power.

B. ASM (Antenna Switch Module / built in LPF)

These filters pass through the signals of which frequency band of 824~849MHz, 1710MHz~1785MHz, 1850MHz~1910MHz which is the transmit frequency of GSM850, DCS, PCS system terminal, and it suppresses other images and spurious frequencies when the terminal transmits GMSK modulated frequencies.

C. Power AMP Module(PAM)

This device amplifies signals ahead of transmiting them through the antenna to provide a sufficient RF power. It has amplification factor of 28dB and efficiency of about 49% typically in GSM850 band and amplification of 20dB and efficiency of about 53% typically in DCS/PCS band.

4.2.5 VC-TCXO(Voltage Controlled Temperature Compensated Crystal Oscillator)

This is the mobile station’s reference frequency source. Its frequency is 26MHz, this signal is applied to the XOUT Buffer in Si4210 and the XOUT Buffer provides the 13MHz system reference clock.

Section 5. Alignment Procedure

5.1 Recommended Test Equipment

Model No.	Description	Maker	Remark
8960	GSM Mobile Station Test Set	Agilent Technologies	
8593E	Spectrum Analyzer	Hewlett Packard	
TDS 340A	Oscilloscope	Tektronix	
FLUKE 87	Digital Multimeter	Fluke	
E3630A	DC Power Supply	Hewlett Packard	
Others	Accessory		Interface Connectors RF Connectors

5.2 Connection of Test Equipment

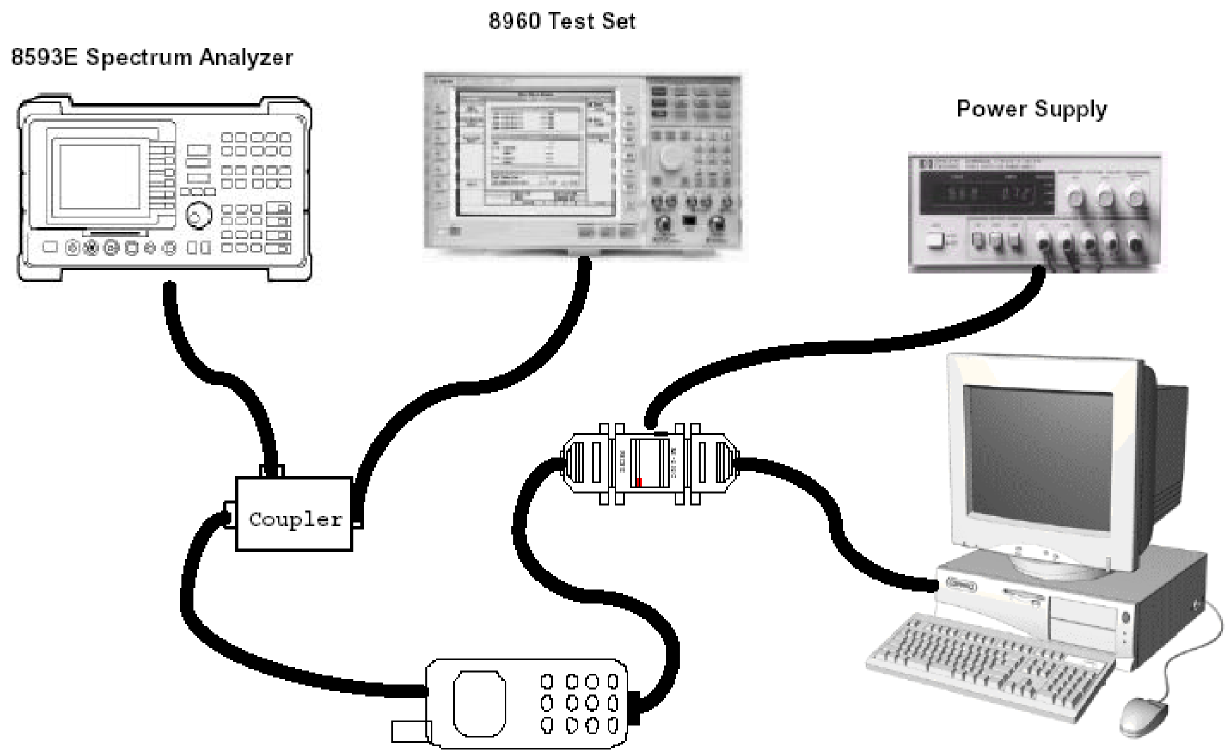


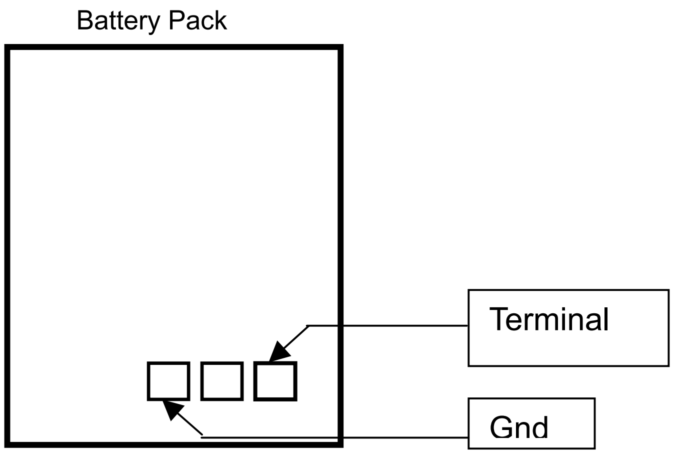
Fig.5-1. Test Set Configuration

SECTION 6. Equipment Repair Procedure

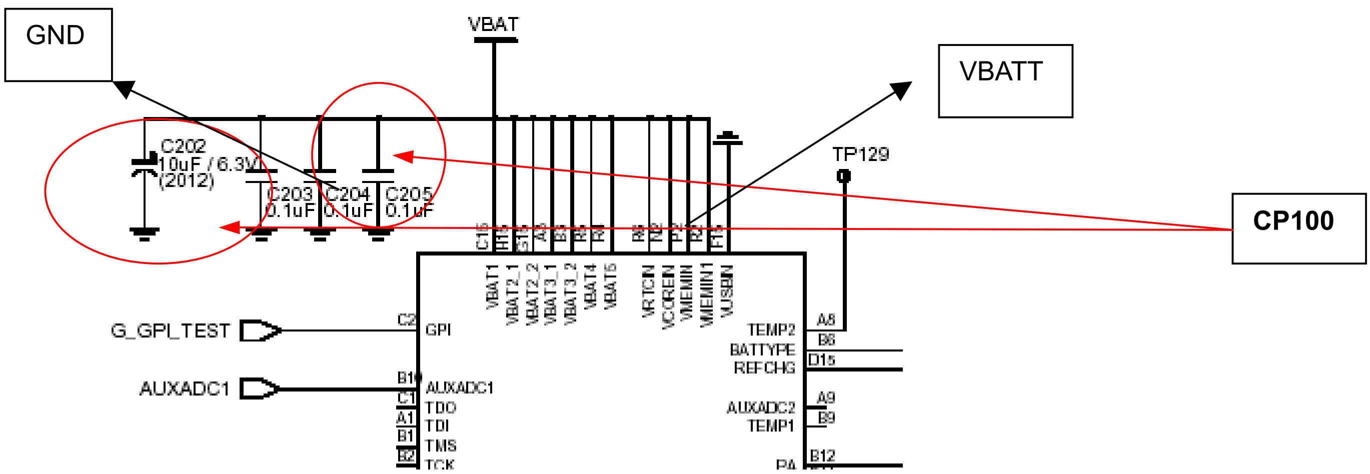
6.1 No Power On with battery Applied.

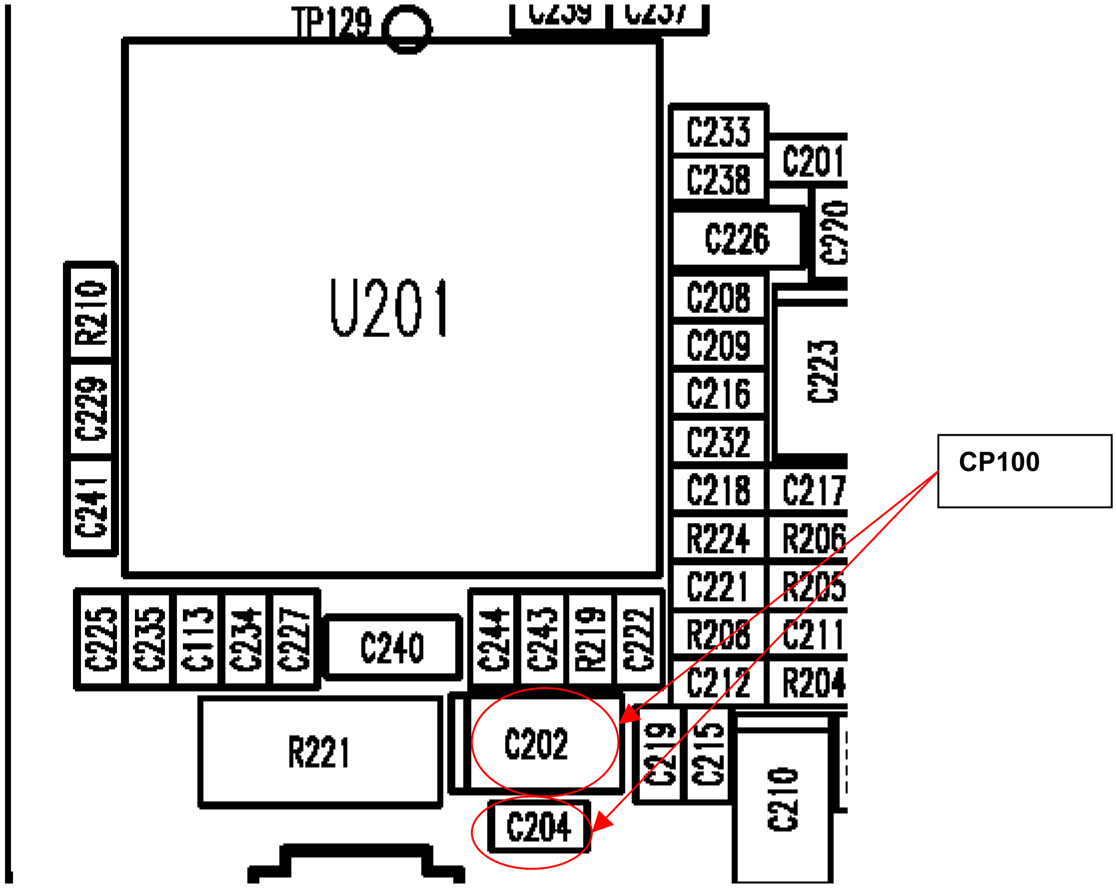
6.1.1 Power CHECK

1. Check battery power : 3.5V~4.2V.



2. Check to see if C202.1 or C205 pin voltage is same with battery power : CP100





3. Check to see if U408.5,6 and R221 pin is same with battery power : CP101

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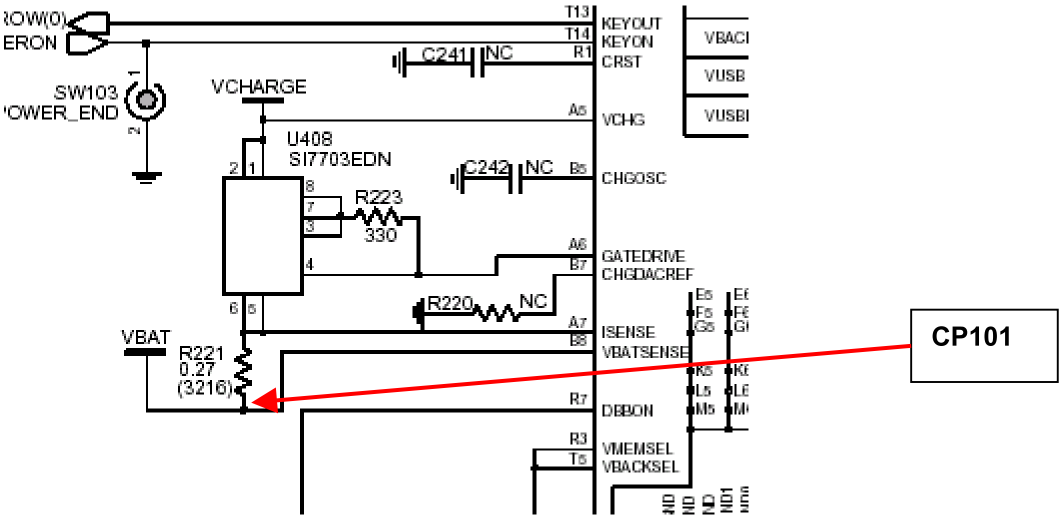
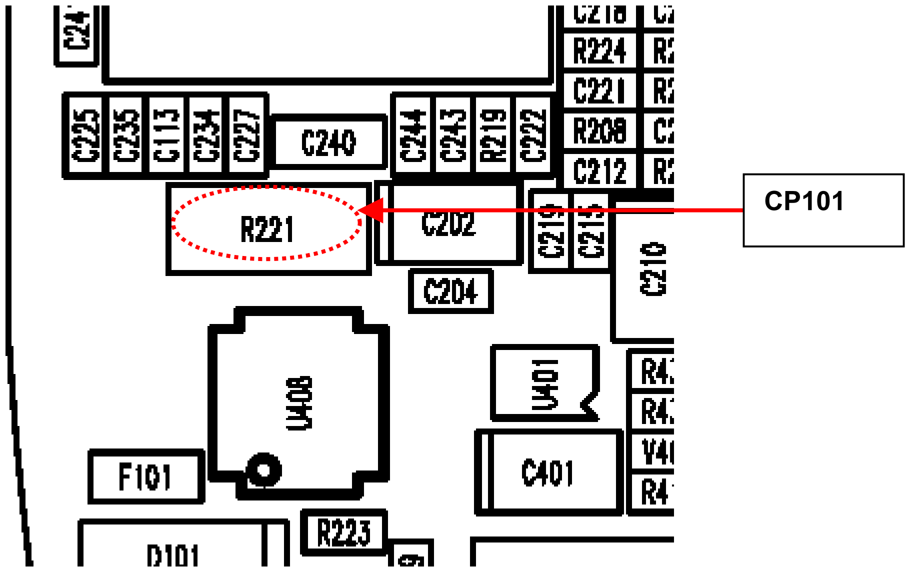
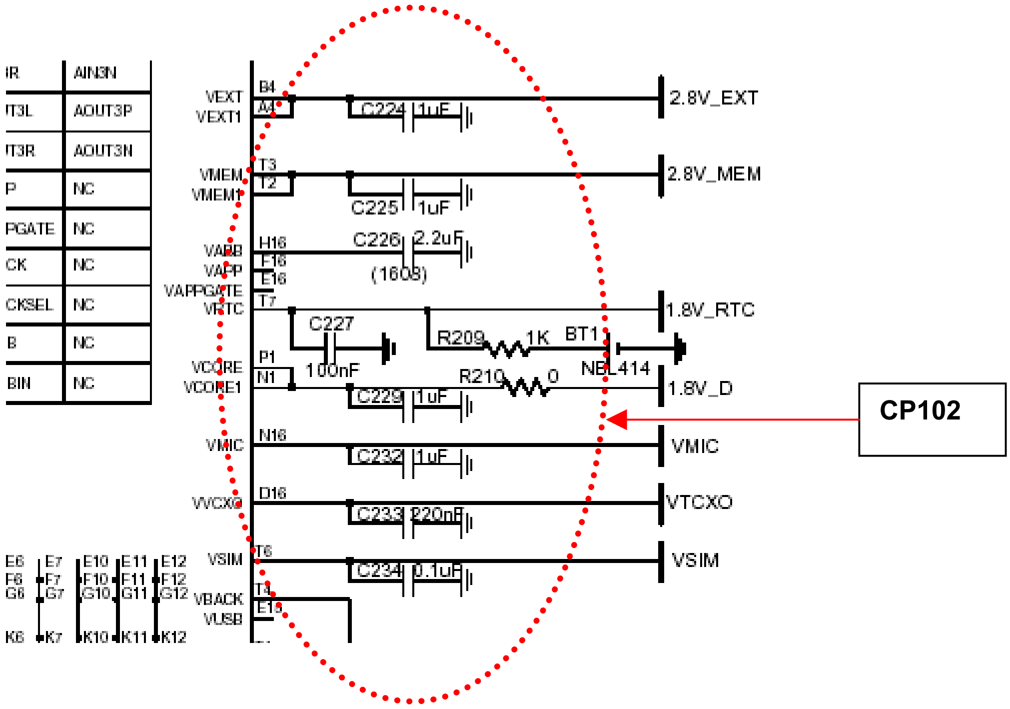


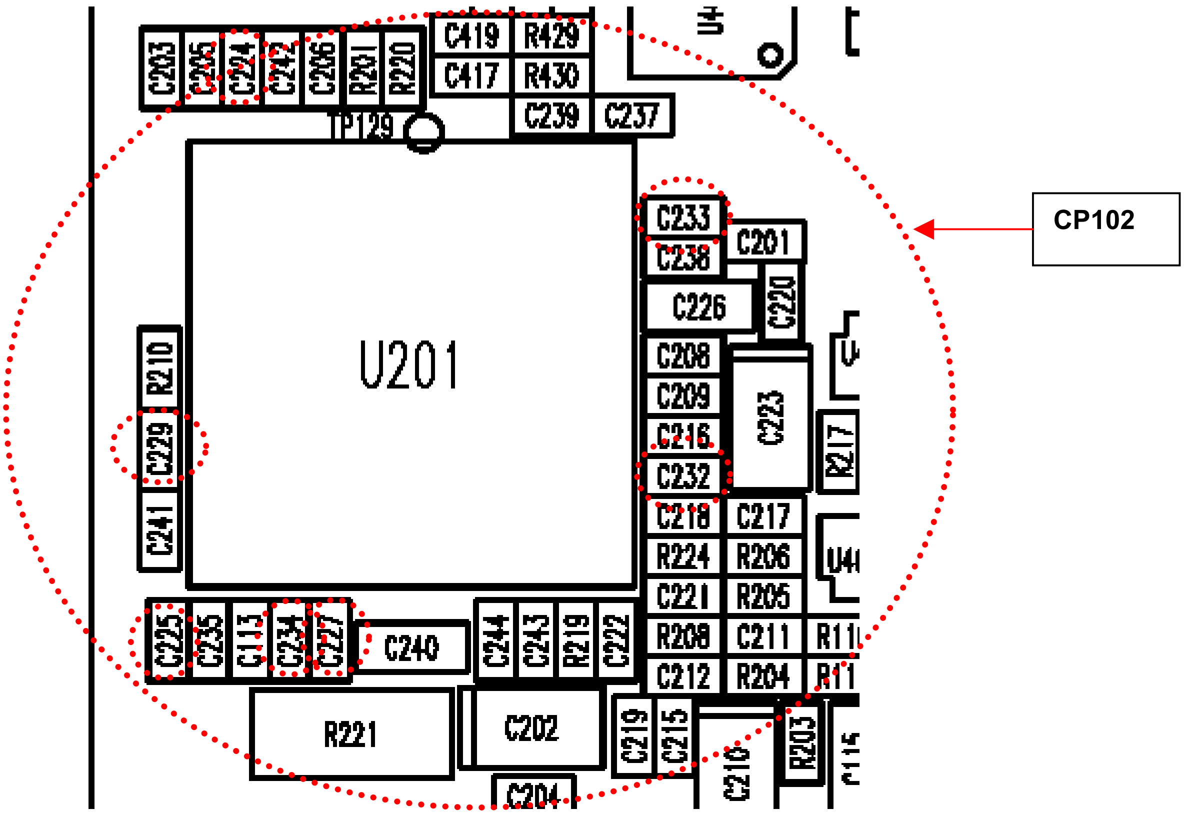
VCHARGE
SW103
U408
SI7703EDN
R223
330
C241
NC
C242
NC
R220
NC
VBAT
R221
0.27
(3216)
KEYOUT
KEYON
CRST
VCHG
CHGOSC
GATEDRIVE
CHGDACREF
ISENSE
VBATSENSE
DBBON
VMEMSEL
VBACKSEL
VUSB
CP101



R224
C221
R208
C212
C225
C235
C113
C234
C227
C240
C244
C243
R219
C222
R221
C202
C204
C210
U408
U401
C401
F101
R223
D101
CP101

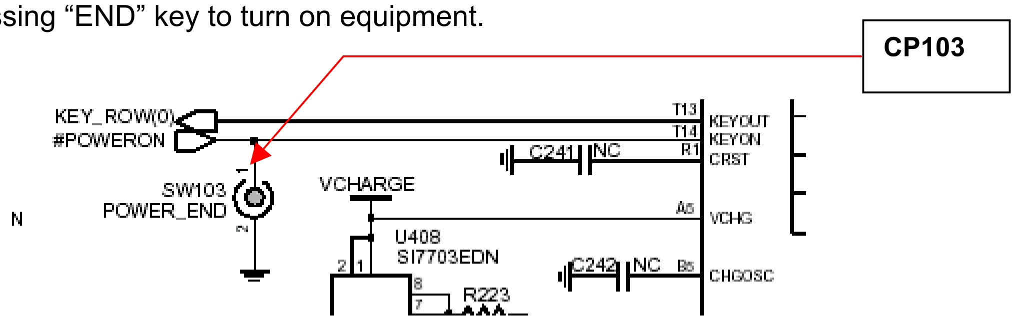
4. Check to see if U201 and C224, C225, C227, C229, C232, C233, C234 pin is 2.8V_EXT, 2.8V_MEM, 1.8V_RTC, 1.8V_D, VMIC, VTCXO, VSIM, : CP102



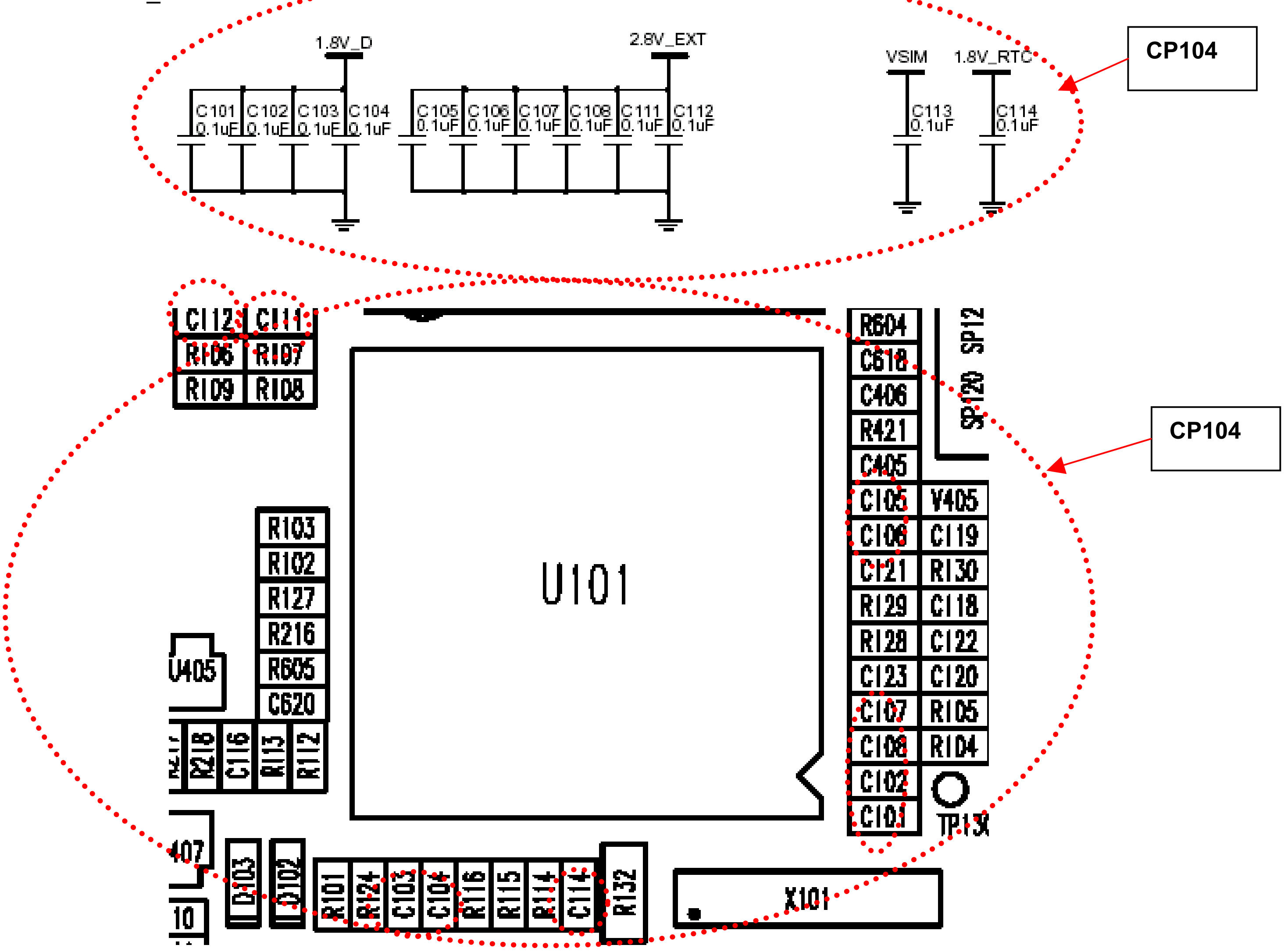


6. Check to see if U201.T14 pin becomes to 0V : CP103

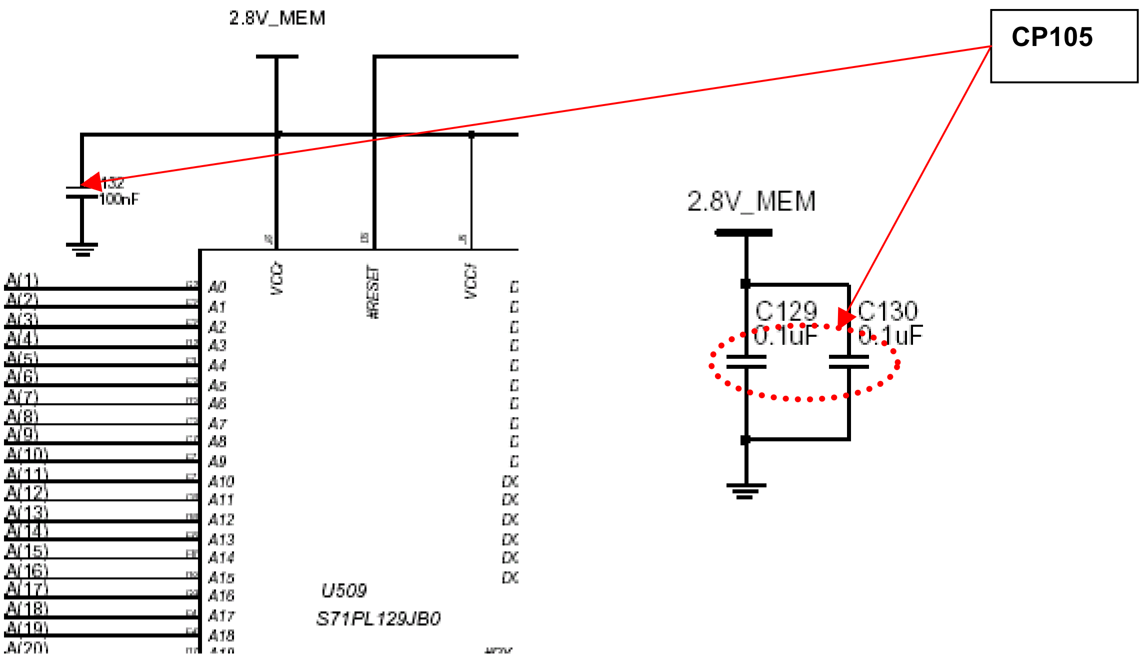
Pressing “END” key to turn on equipment.

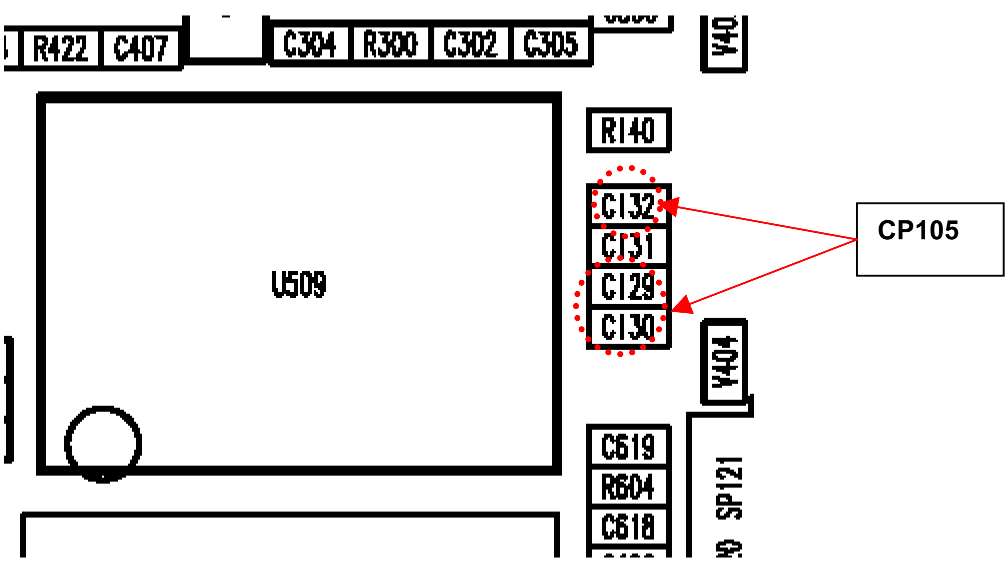


7. Check to see if C101,C102,,, C105,C106,,C108,C111,C112, C113,C114, is 1.8V_D, 2.8V_EXT, VSIM, 1.8V_RTC : CP104



8.Check to see if U509 and C132,C129,R130 is 2.8V_MEM : CP105

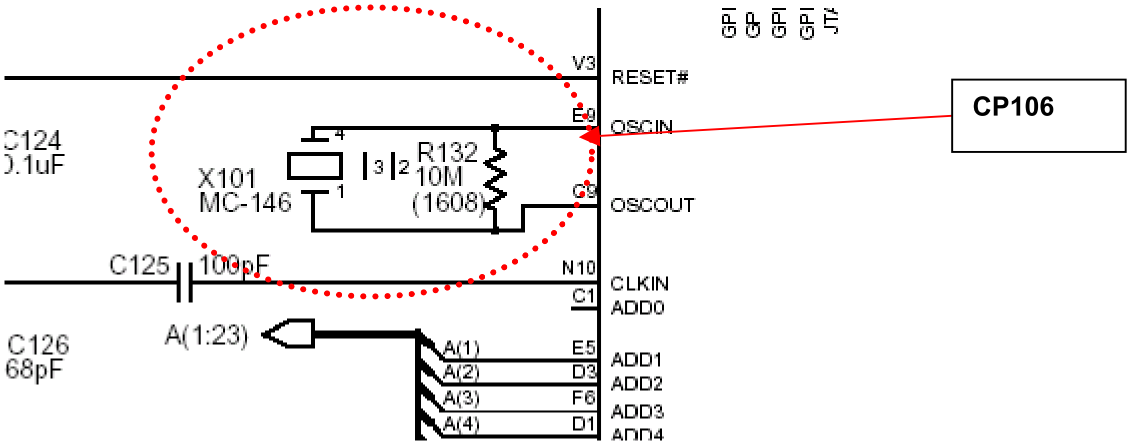


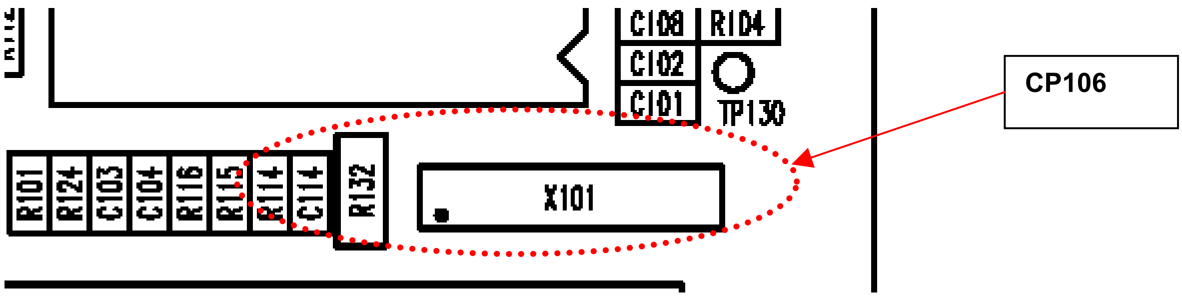


6.1.2 Oscillation CHECK

1. Check to see if U101 No. E9 and C9 pin is oscillated(32.768KHz) : CP106

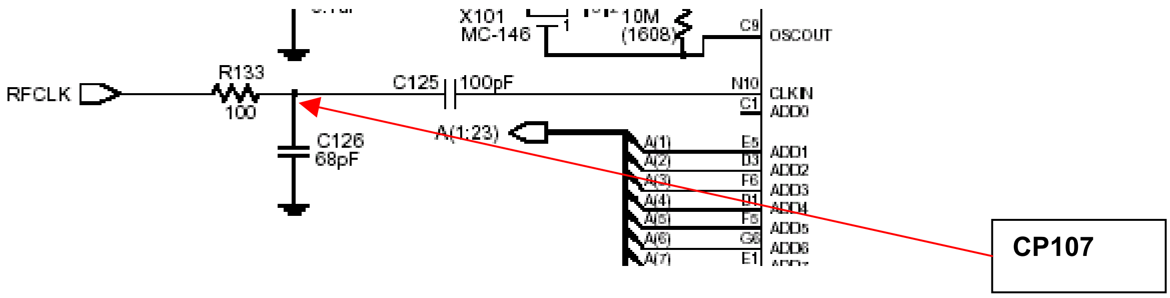
NO → Check R132 and then replace X101

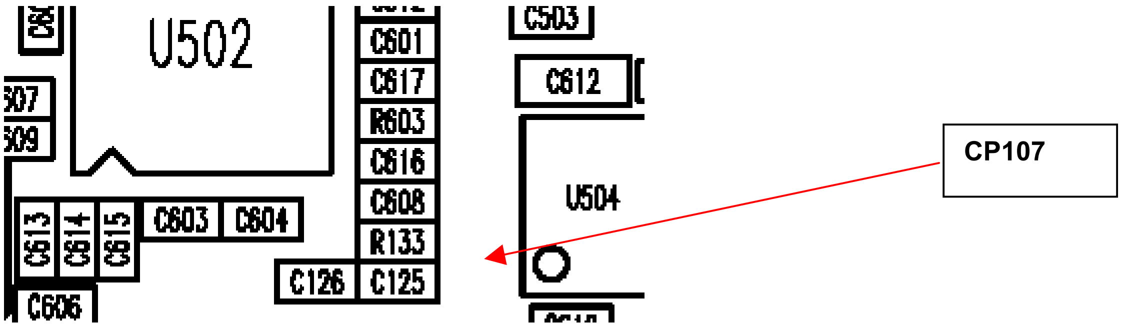




2. Check to see if U101.N10 pin Master Clock(13MHz). : CP107

NO → Check R133, C126 pin and then check the PCB pattern, soldering





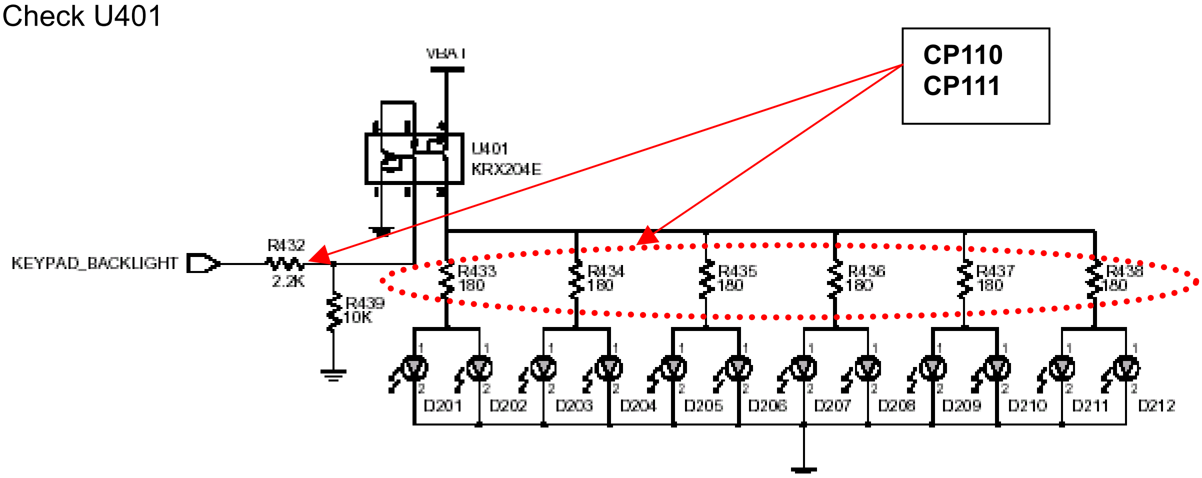
6.1.3 KEYPAD LED Not in Operation

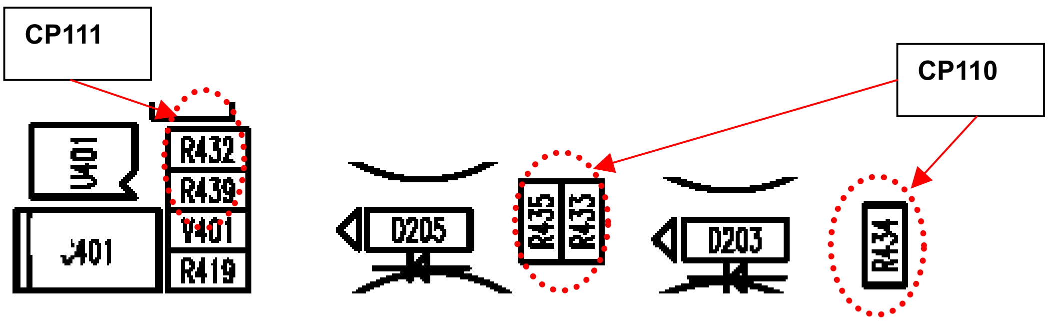
1. Check to see if R433 ~ R438 : CP110

   NO → Replace the resistors.

2. Check R432 signal (control PWM) : CP111

3. Check U401

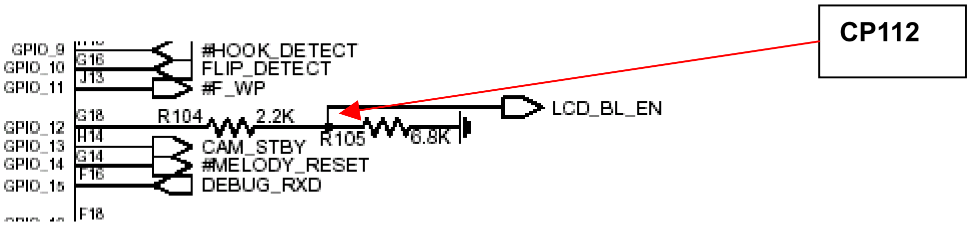


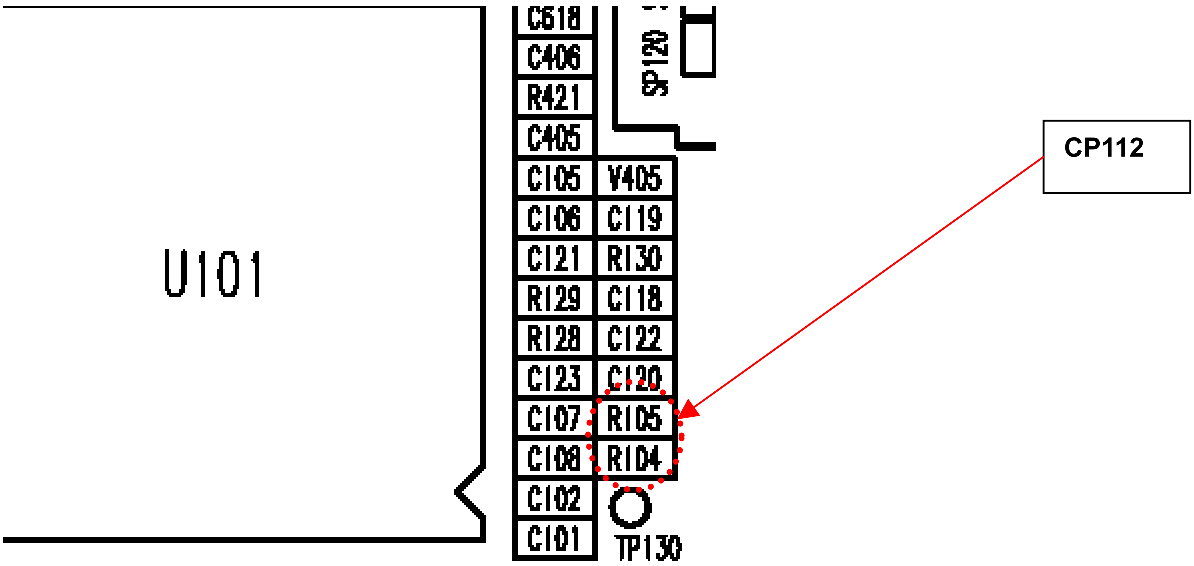


6.1.4 LCD Backlight Not in Operation (White)

1. Check to see if U101.G18 or R104,R105 pins are controlled GPIO (2.8V): CP112

.





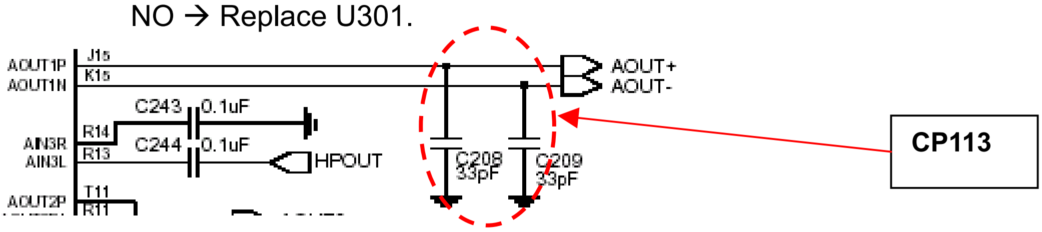
6.2 Audio Part (Earpiece, Hands-free Earphone, Microphone, Hands-free Mic)

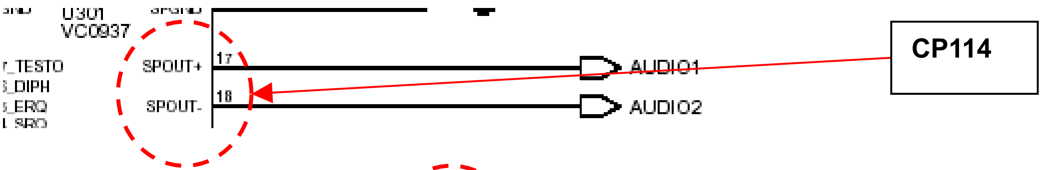
6.2.1 No receiving tone heard (Ear-piece)

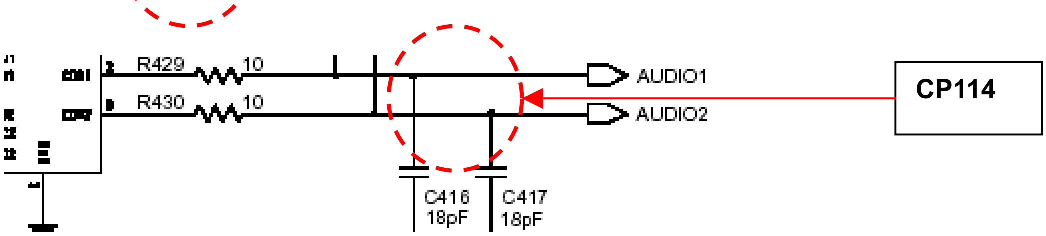
1. BEEP TONE: Check U201.J15 and K15(C208,C209,) pins (Ear Signal) for waveform : CP113 NO → Replace U201.

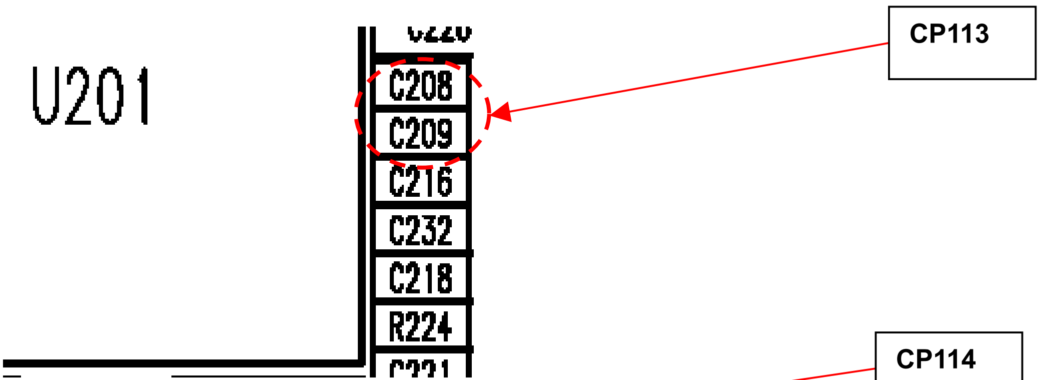
2.VOICE,BELL TONE : Check U301.17, 18 and C416,C417 pins for waveform. : CP114

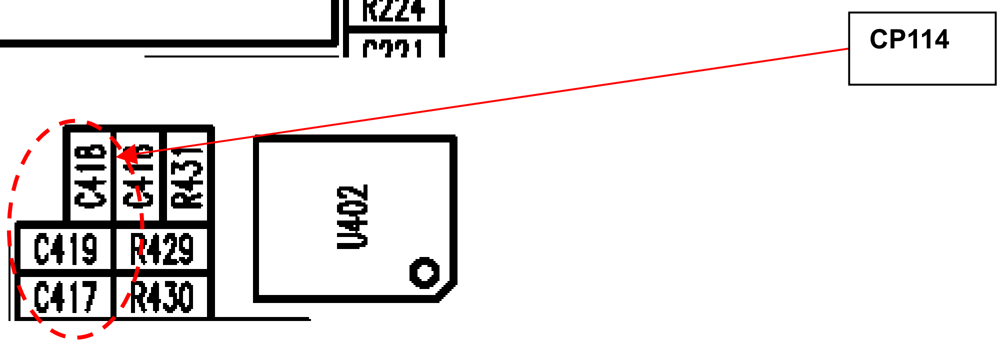
NO → Replace U301.





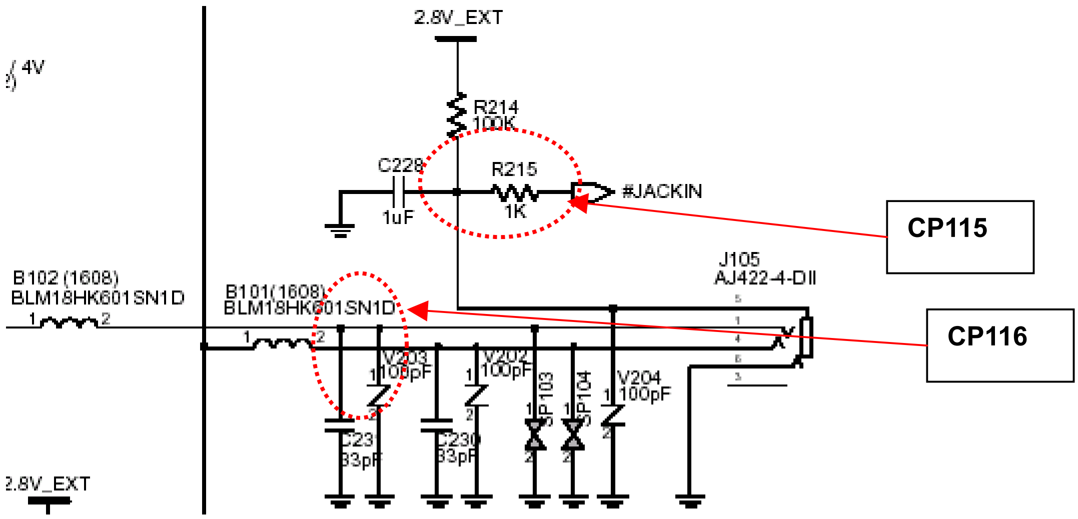


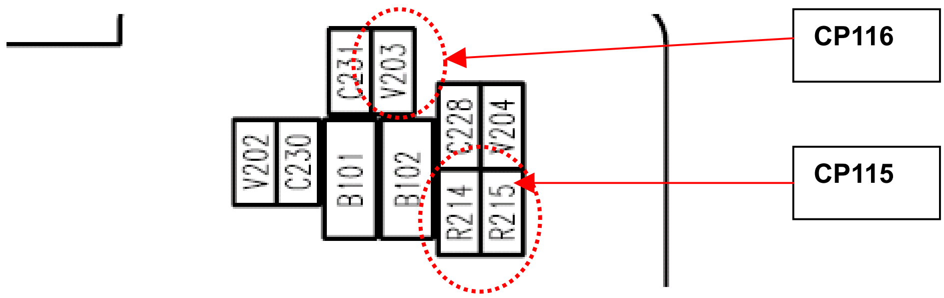




6.2.2 No Receivng tone heard (Hands-free Earphone)

1. Check to see if U101.J16 (R215) is around 0V:
   NO → Check to see J105 : CP115
   Set to HP8922M to connect a call and then set to 1kHz.
2. Check C231, V203 pin for waveform : CP116
3, Check Hands-free Earphone





6.2.3 Side Tone Not transmitted (Ear-piece)

Repeat 6-2-1 No receiving tone heard.(Ear-piece)

1. Check to see if Mic + pin is around 1.5V : CP117

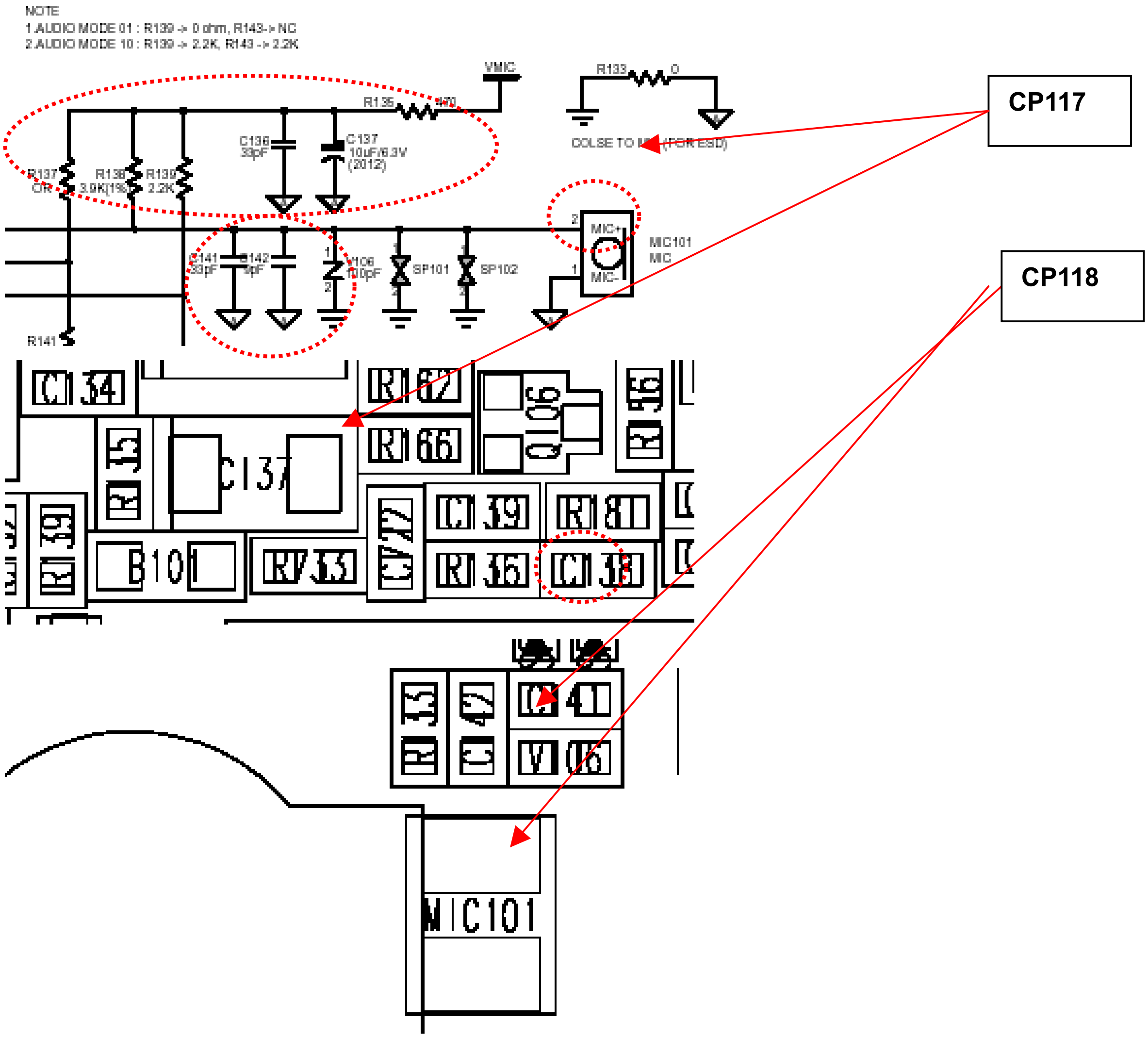
   NO → Check that R135, C137, C136 and R138 is cold solder, broken, short to the other PCB pattern or not

   If you find out any defective part, you replace it.

Set to HP8922M to connect a call and then set to 1kHz with Echo audio mode.

2. Check C142.C141 pins for wave form : CP118

   NO→ Replace MIC



6.2.4 Side Tone Not transmitted (Hands-free Mic.)

Repeat 6-2-2 No receiving tone heard.(Hands-free Earphone).

1. Check to see if R206 pin is 2.5V : CP119

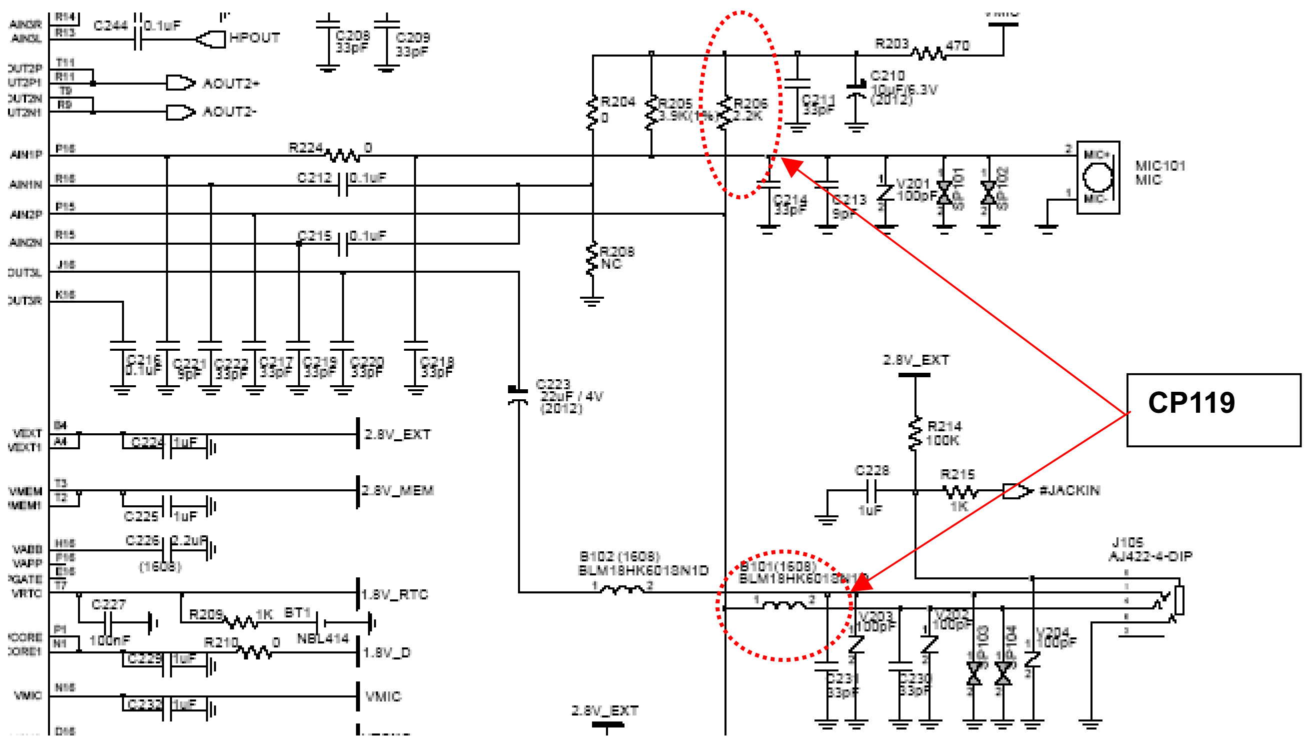
   NO → Check that C222is cold solder,broken,short to the other PCB pattern or not.

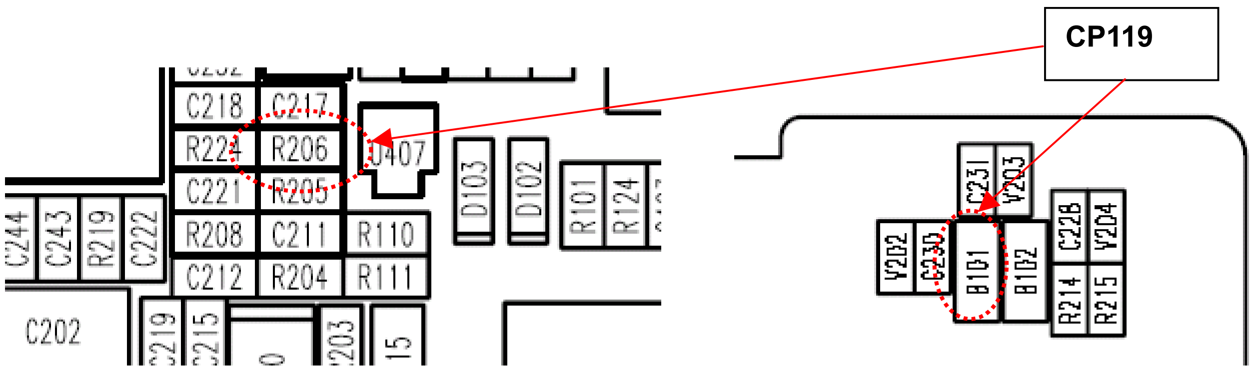
   If you find out any defective part, you replace it.

   Set to HP8922M to connect a call and then set to 1kHz with Echo audio mode.

3. Check B101 pins for wave form : CP119

   NO → Replace Handsfree Mic.





6.2.5 Hook Switch not working

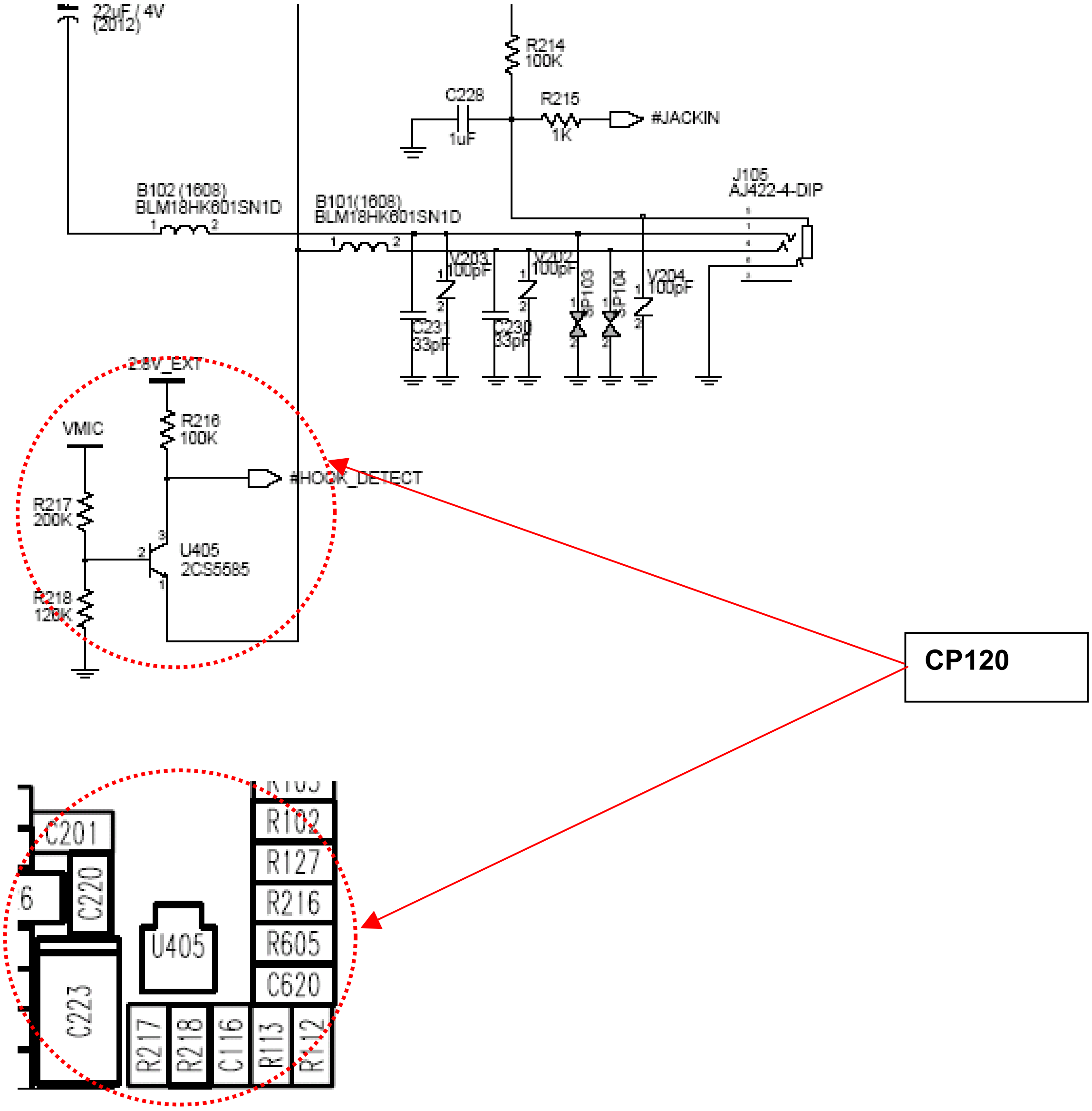
1. Check to see if Q405.1 pin is 2.4V : CP120
2. Check to see if Q405.1 pin is 0V during pressing Hook Switch : CP120

   NO → Check that B101 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it
3. Check to see if U405.3 pin is around 0V, when you press Hook Switch : CP120

   NO→ Check that U405 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

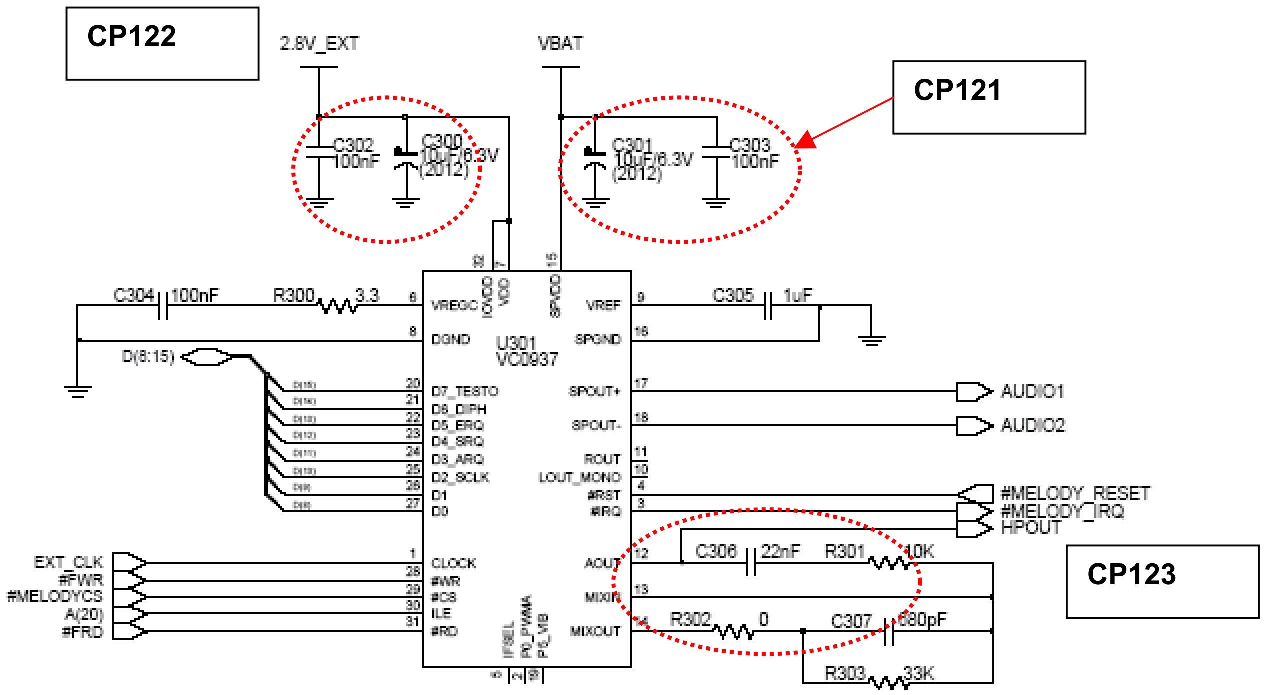


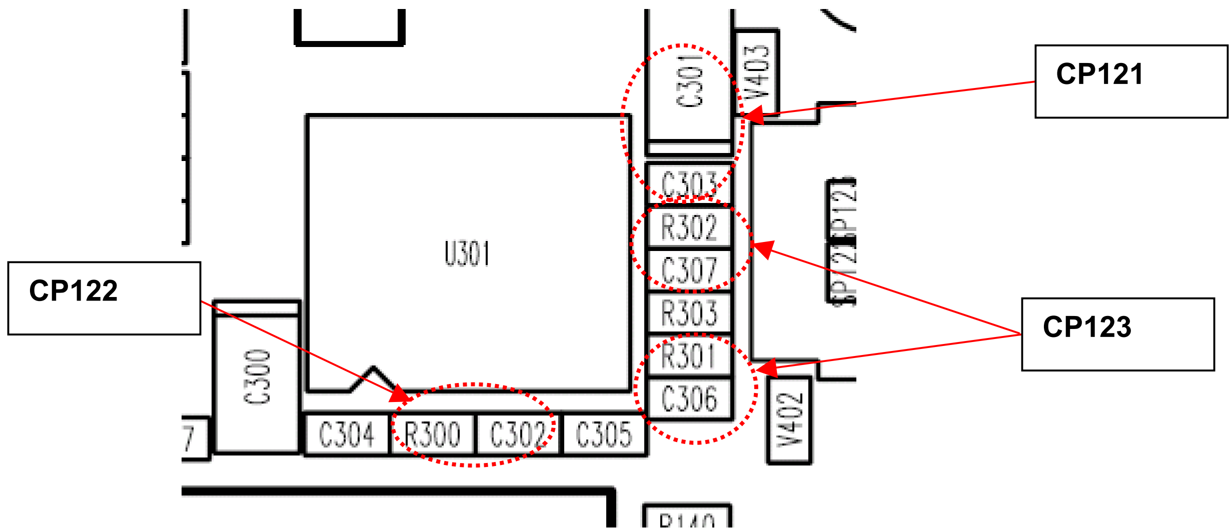
6.2.6 Melody not ringing

1. Check to see if C301, C303 is Vbat : CP121
2. Check to see if C302, C300 is 2.8 V : CP122
3. Check U301.12, 13, 14 pin for waveform: CP123

NO → Check that C306, R301,R302, C307and R303 cold solder, broken, short to the other PCB pattern or not

Check U301 17, 18 pin SPOUT1,SPOUT2 for waveform : NO → replace SPK.





6.2.7 Vibrator not working

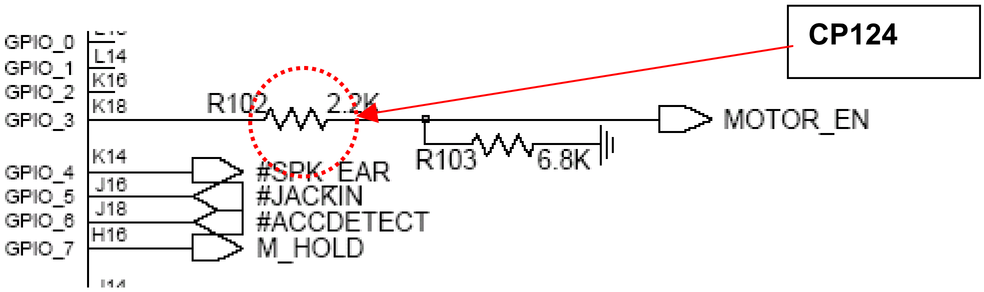
1. Check to see if R102 pin is 2.8V : CP124

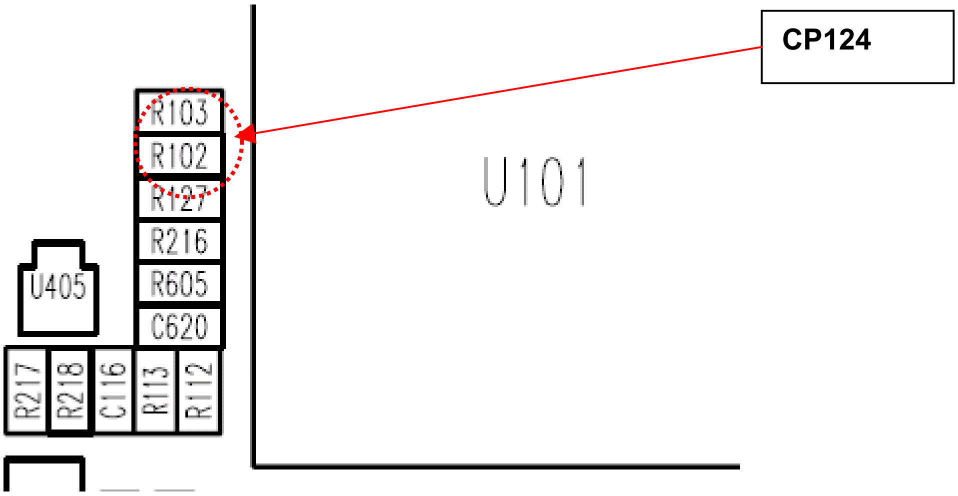
   NO → Check to see R102cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

2. Check to see Vibrator

   If you find out any defect, you replace it





6.3 SIM card part

6.3.1 SIM error

1. Check to see if J104.1 pin is around 2.85V : CP126

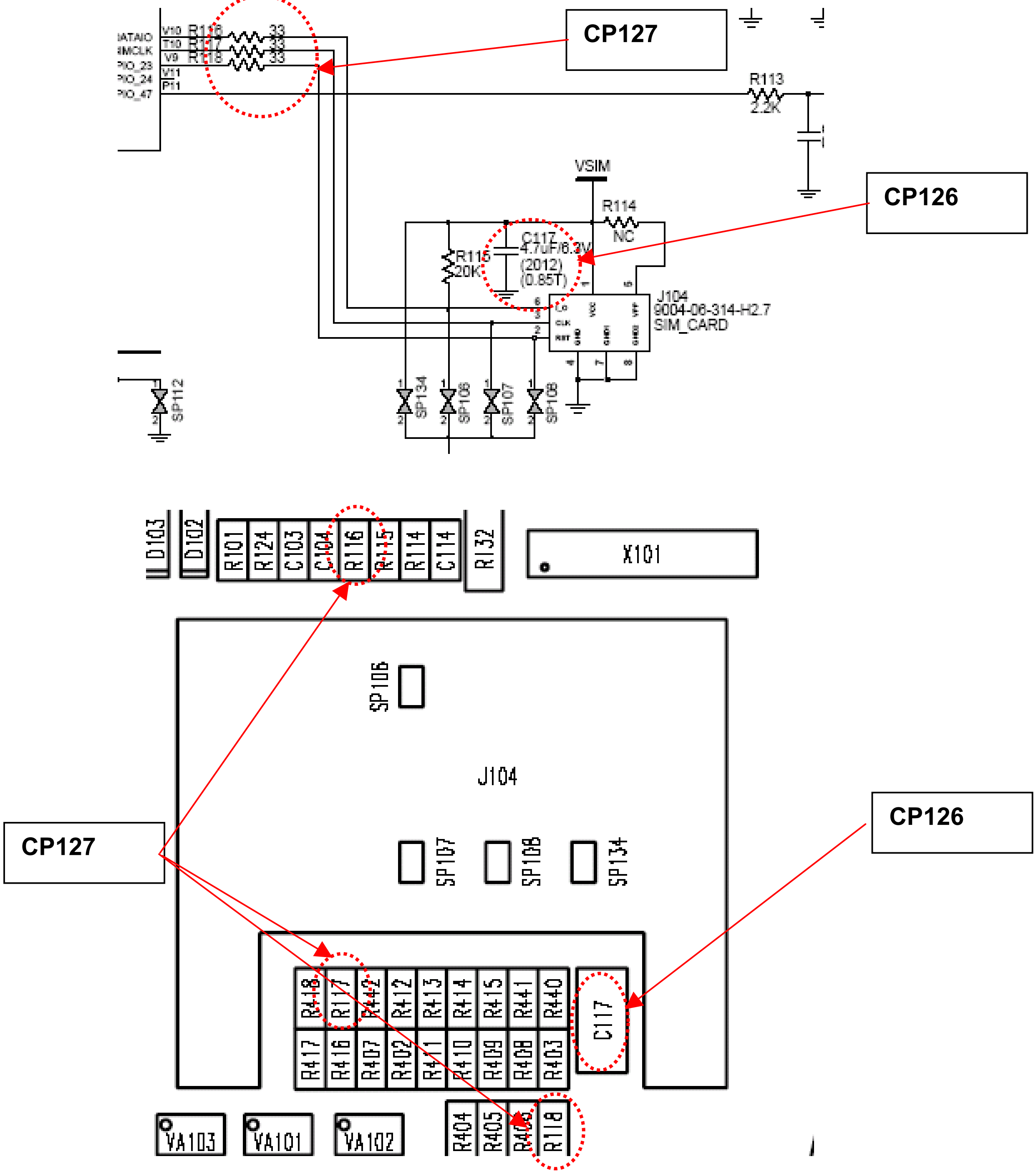
   NO → Check to see C117 pin cold solder, broken, short to the other PCB pattern or not :

   If you find out any defect, you replace it

2. Check to see J103.2, 3, 6(R116,R117,R118) for wave form : CP127

   NO → Check to see J104, R116 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it



6.4 Charger part

6.4.1 Charging error

Insert adaptor into I/O jack.

1. Check to see if F101, D101 pin is 5.2V : CP128

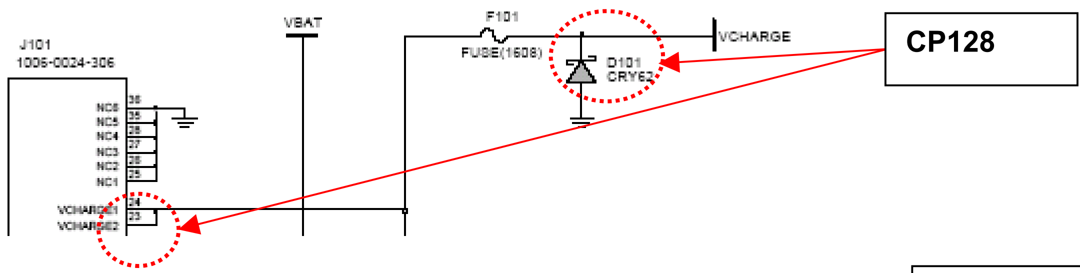
   NO → Check to see J101.23, 24(I/O connector) pin and F101, D118 cold solder, broken, short to the other PCB pattern or not :

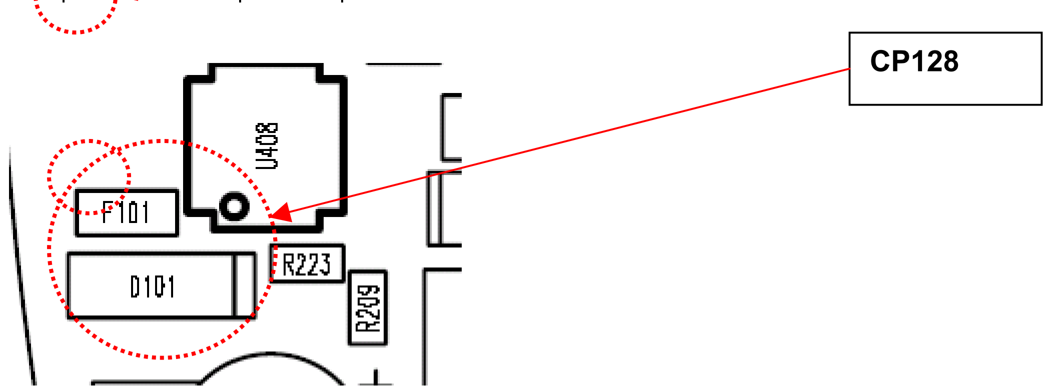
   If you find out any defect, you replace it

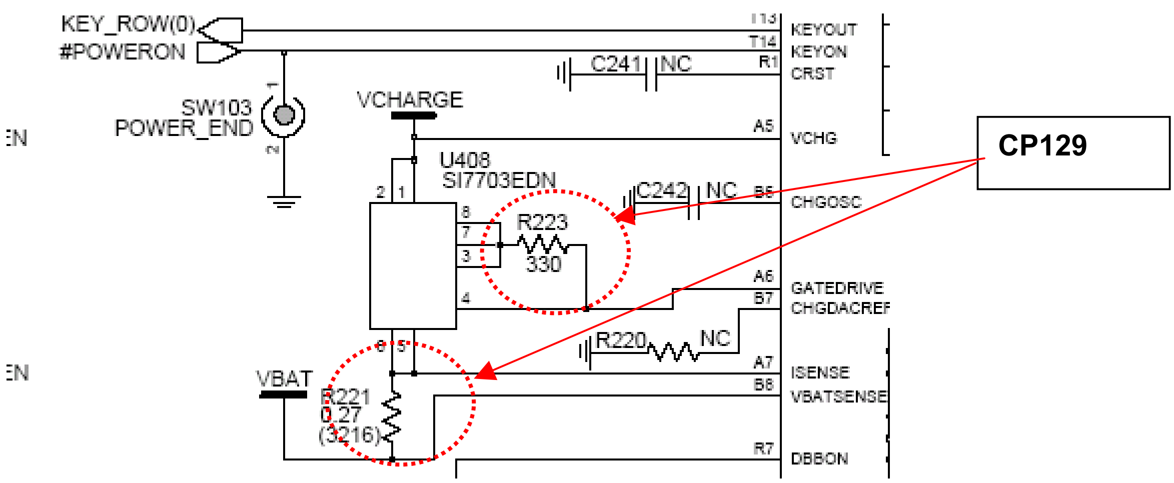
2. Check to see U408 No.1,2 pin is 5.2V : CP129

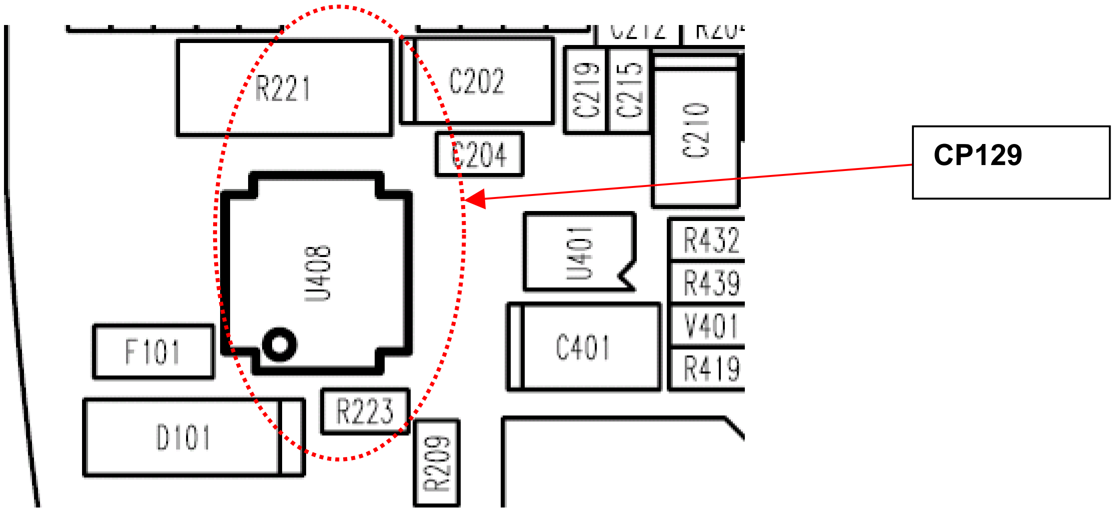
   NO → Check to see U408, R223, and R221 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it








R221
C202
C219
C215
C210
C204
U408
U401
R432
R439
V401
R419
F101
C401
R223
D101
R209
CP129

6.5 RF Part

6.5.1 Test conditions

1. Test condition 1 : VBAT = 3.8V during all tests

2. Test condition 2 : Traffic channel :GSM850 Band
   Tx mode
   Ch190
   Power Level : 13

3. Test condition 3 : Traffic channel : DCS Band
   Tx mode
   Ch698
   Power Level : 10

4. Test condition 3 : Traffic channel : PCS Band
   Tx mode
   Ch662
   Power Level : 10

5. Test condition 4 : Traffic channel :GSM850 Band
   Rx mode
   Ch190
   Input power : -70dBm

6. Test condition 5 : Traffic channel : DCS Band
   Rx mode
   Ch698
   Input power : -70dBm

7. Test condition 5 : Traffic channel : PCS Band
   Rx mode
   Ch662
   Input power : -70dBm

8. RF power values are measured using 50Ω coaxial cable.

6.5.2 Power Supply Check Point

Step	Test point	Typical Value	Condition	Checking Point
2-1	U504 Pin#1	3.8V	2,3,4,5,6,7	Check route connection : VBAT
2-2	U504 Pin#5	2.8V	2,3,4,5,6,7	Check route connection : VCC_RFCHIP
2-3	U505 Pin#3,8,20	3.8V	2,3,4,5,6,7	Check route connection : VBAT

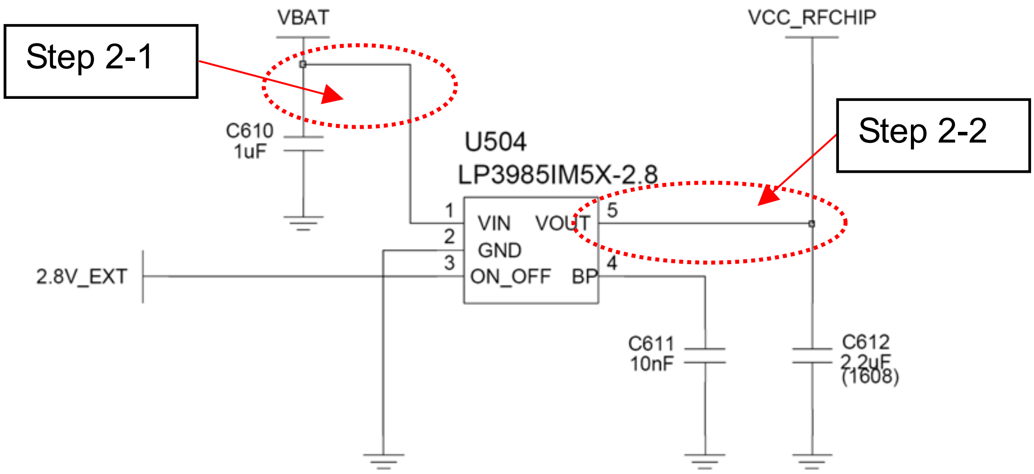


Fig.6-1 U504 Regulator Power Supply Schematic

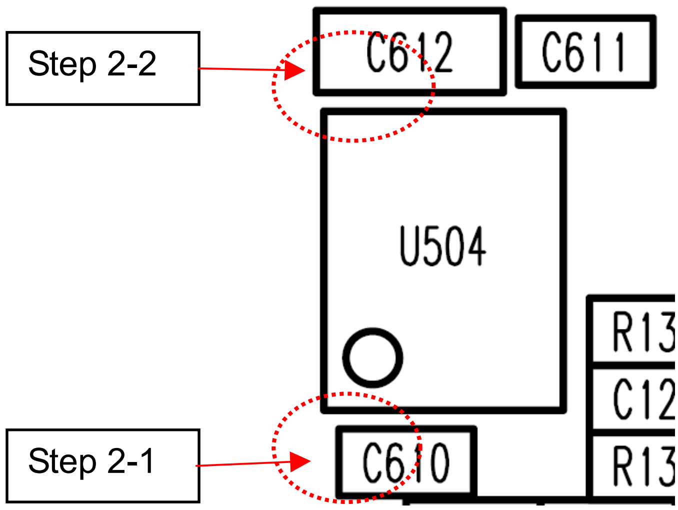


Fig.6-2 U504 Regulator Power Supply PCB Layout

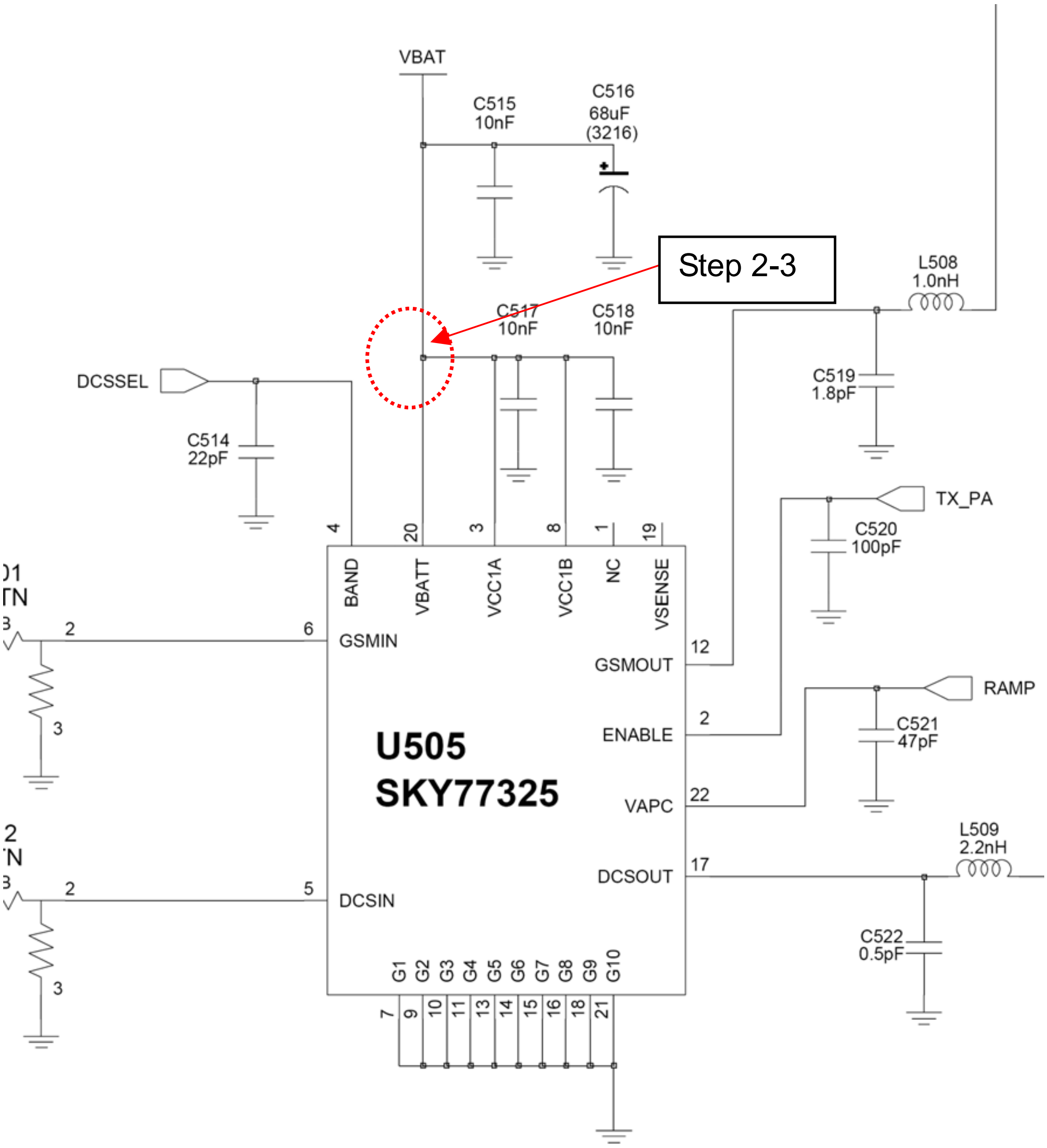


Fig.6-3 U505 PAM's Power Check Point

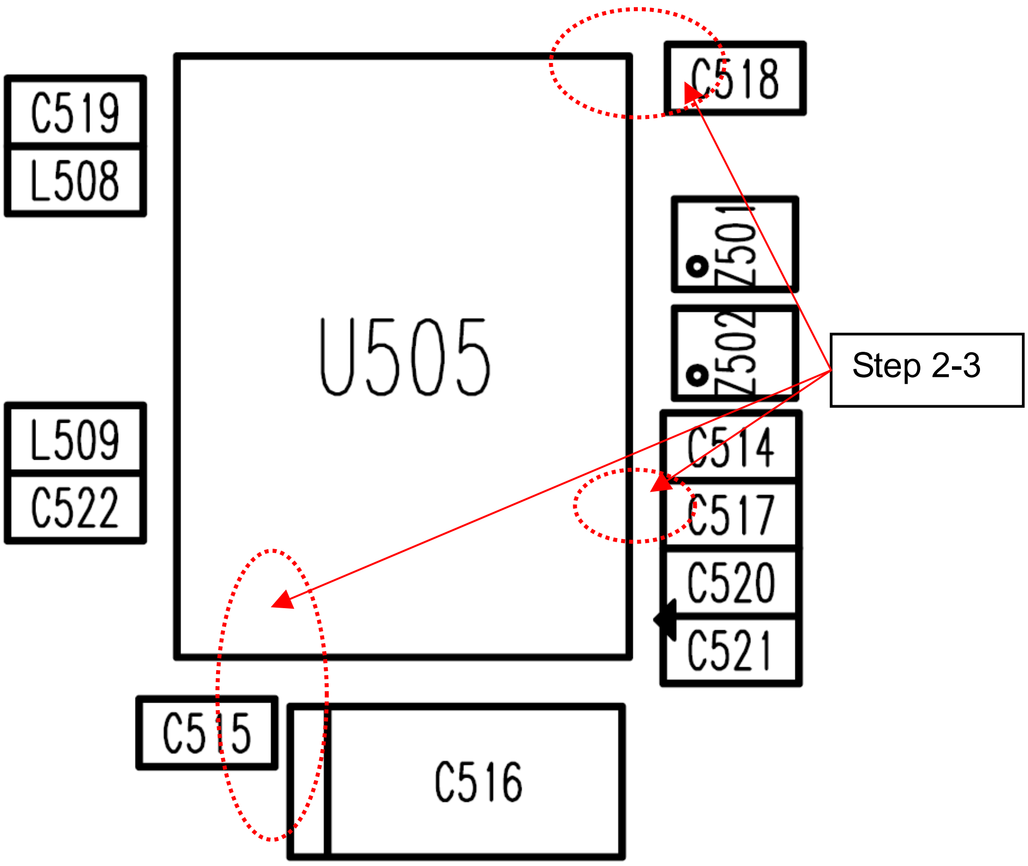


Fig.6-4 U505 PAM's PCB Layout

6.5.3 Power Amplifier Module

Step	Test point	Typical Value	Condition	Checking Point
3-1	U505 Pin#2	Logic High	2, 3, 4	Check route connection : TX_PA
3-2	U505 Pin#4	Logic High	3, 4	Check this pin 2, When Logic High, then DCS/PCS Mode. While Logic Low , GSM850 mode is operating.
		Logic Low	2, 5, 6, 7	

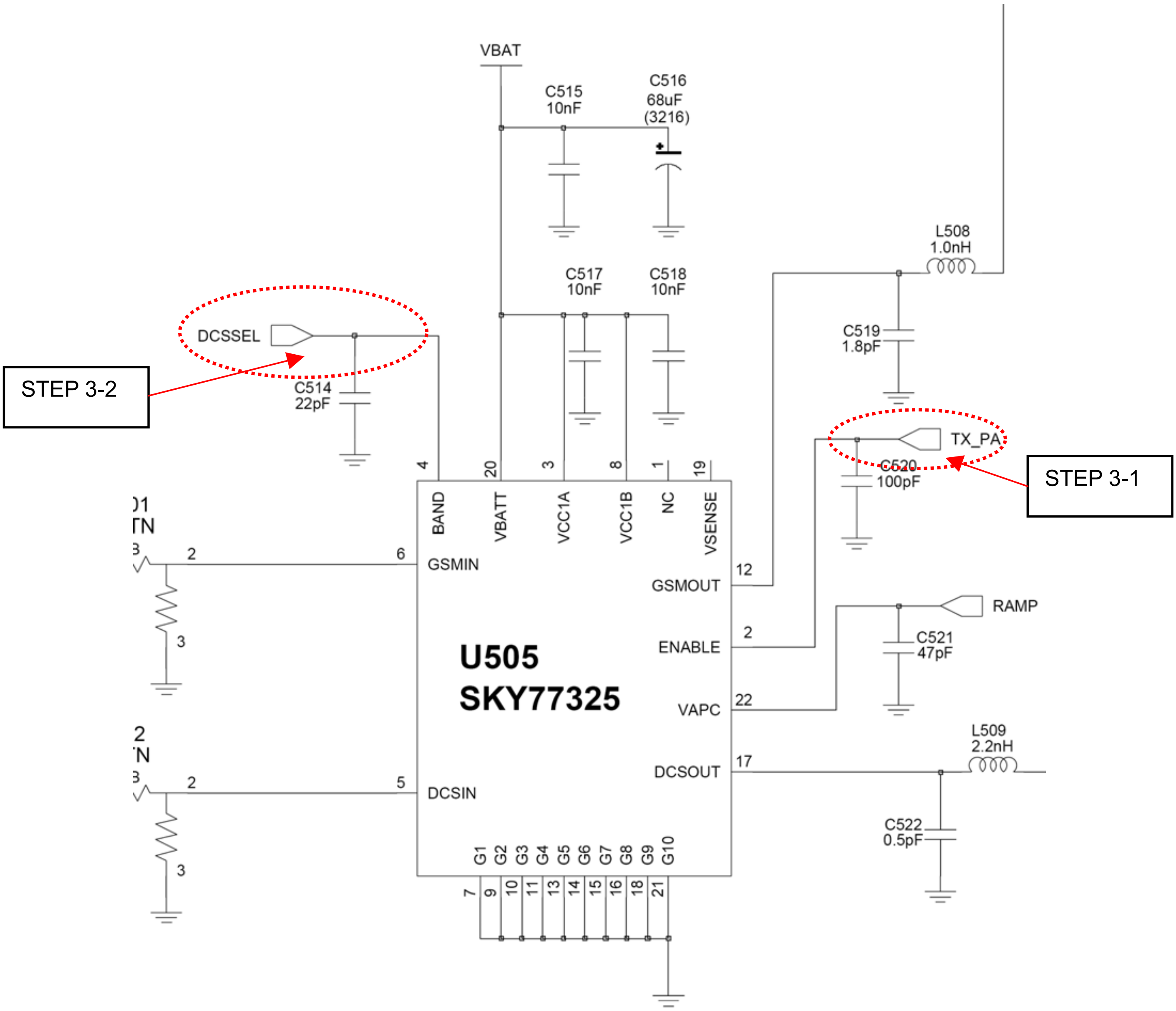


Fig.6-5. U505 PAM TX_PA and DCS SEL Test Point Circuit

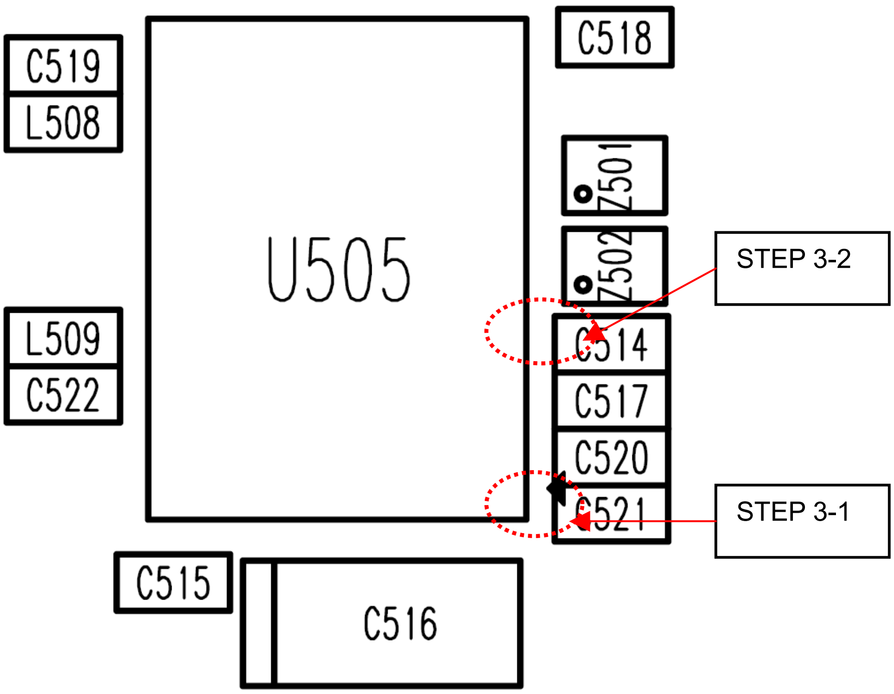


Fig.6-6. U505 PAM TXEN and DCSSEL Test Point on the PCB Layout

6.5.4 VC-TCXO

Step	Test point	Typical Value	Condition	Reaction to Abnormality
4-1	U503 Pin#1	0.5V ~ 2.5V	1,2,3,4,5,6,7	Check route connection : AFC
4-2	U503 Pin#4	2.8V	1,2,3,4,5,6,7	Check route connection : VTCXO

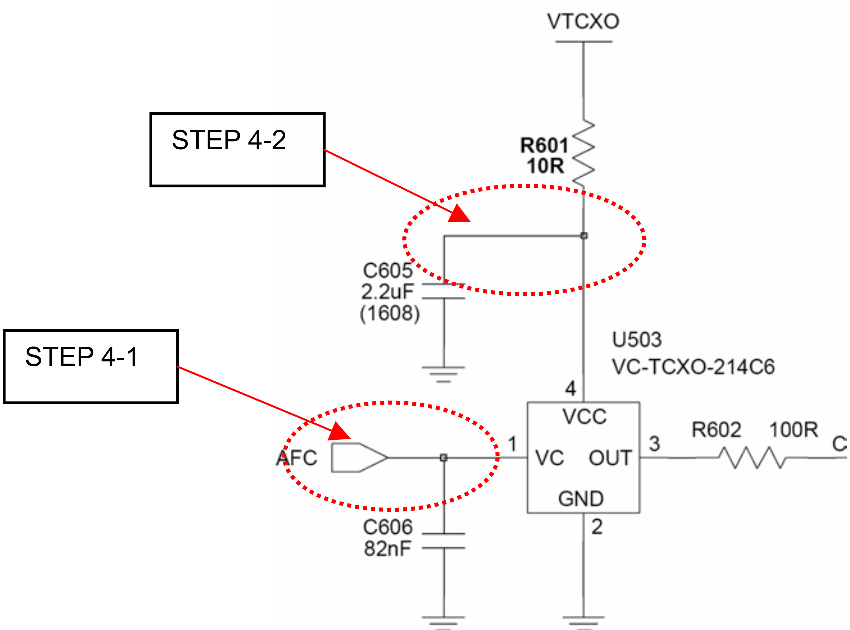


Fig.6-7. U503 VCTCXO Check Point Circuit

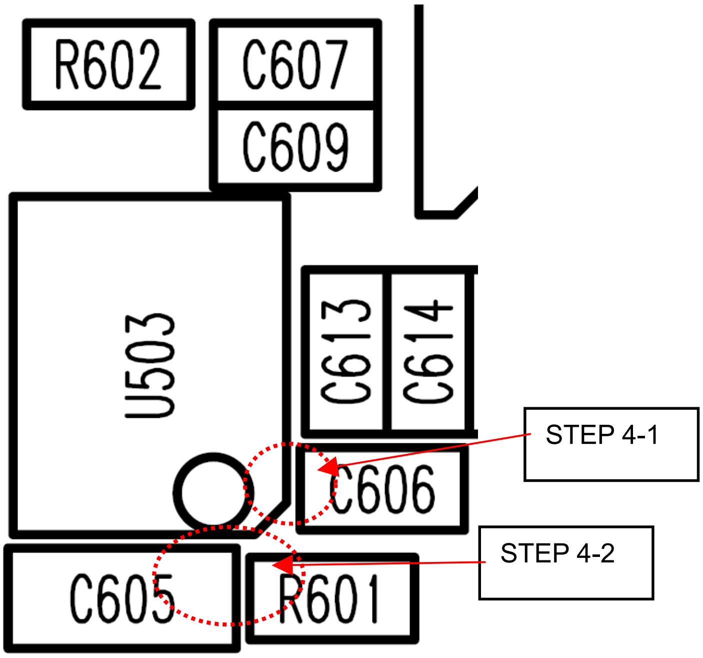


Fig.6-8. U503 VCTCXO Check Point on the PCB Layout

6.5.5 Antenna Switch Module

Step	Test point	Typical Value	Condition	Check point
5-1	U501 Pin#10	2.8V	2	When Pin#10 is Logic High and Pin#4 and Pin#2 is Logic Low the mode is EGSM Tx.
5-2	U501 Pin#4	2.8V	3,4	While Pin#4 is Logic High and Pin#10 and Pin#2 is Logic Low the operating mode is DCS Tx, PCS TX.
5-3	U501 Pin#10, Pin#4, Pin#2	0 V	5,6	While Pin#10, Pin#4 and Pin#2 is Logic Low the operating mode is GSM850 Rx or DCS Rx.
5-4	U501 Pin#2	2.8V	7	While Pin#10 and Pin#4 is Logic Low and Pin#2 is Logic High the operating mode is PCS Rx..

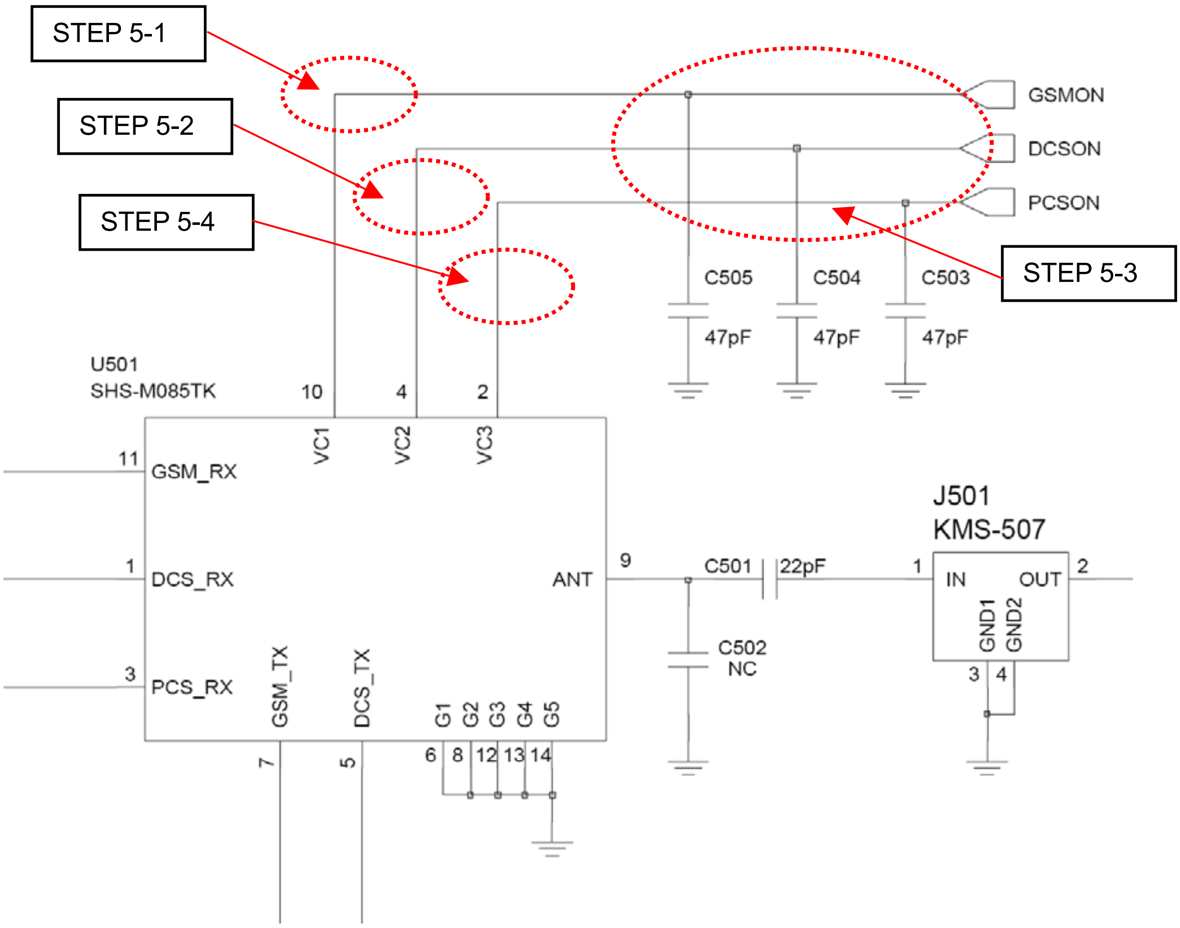


Fig. 6-9 U501 Antenna Switch Module Circuit

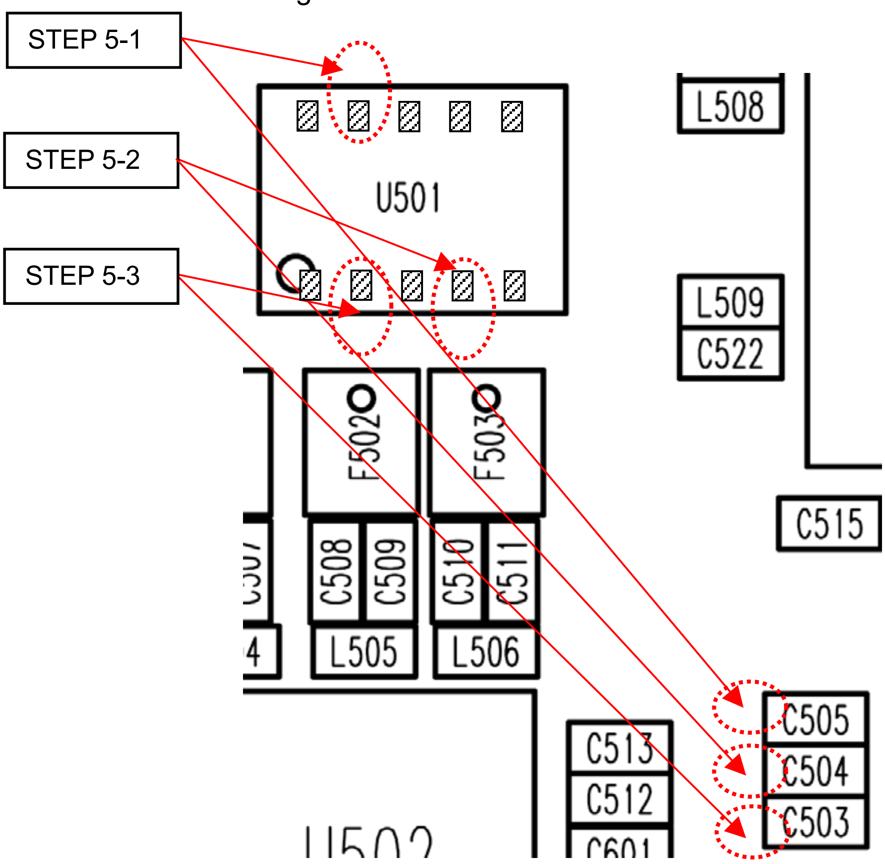


Fig. 6-10 U501 Antenna Switch Module PCB Layout