PANTECH

G800 Service Manual

(GSM Cellular Phone)

Pantech Co., Ltd., Korea

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1st Edition

For Use by Authorized Service/Maintenance Personal Only

Documents to Receive This Addendum:

G800 Maintenance/Repair/Operating Manual

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SECTION 1. Introduction

1.1. An Introduction of GSM Digital Cellular Mobile Communication System

GSM (Global System for Mobile communication) concluded that digital technology working in the Time Division Multiple Access (TDMA) mode would provide the optimum solution for the future system. Specifically , a TDMA system has the following advantage

► Offers a possibility of channel splitting and advanced speech coding ,resulting in improved spectrum efficiency.

► Offers much greater variety of service than the analog

► Allows considerable improvements to be made with regards to the protection of information.

The GSM system is basically designed as a combination of three major subsystem;
The network subsystem, the radio subsystem, and the operation support system.
The functional architecture of a GSM system can be divided into the Mobile Station (MS), the Base Station (BS), and the Network Subsystem (NS). The MS is carried by the subscriber, the BS subsystem controls the radio link with the MS and the NS performs the switching of calls between the mobile and other fixed or mobile network users as well as mobility management. The MS and the BS subsystem communicate across the Um interface also known as radio link
The specifications relating to MS are as follows:

- TS 100 607-1 : Digital cellular telecommunication system(Phase2+)Mobile Station (MS) con Formance specification Part1:Conformance specification

1.2. Frequency Allocation and Its Use

Transmit frequency band : 880 MHz ~ 915 MHz(For EGSM), 1710 MHz ~ 1785 MHz(For DCS), 1850 MHz ~ 1910 MHz(For PCS)

Receive frequency band : 925 MHz ~ 960 MHz(For EGSM), 1805 MHz ~ 1880 MHz(For DCS), 1930 MHz ~ 1990 MHz(For PCS)

Channel spacing : 200 KHz

ARFCN(Absolute Radio Frequency Channel Number) : 1~124 and 975~1023 (For EGSM), 512~885 (For DCS), 512~810 (For PCS)

Transmit receive frequency spacing : 45MHz(For EGSM), 95MHz(For DCS), 80MHz(For PCS)

Frequency band and Channel Arrangement

For standard GSM Fl(n)=890+0.2*n 1 ≤n≤ 124 Fu(n)=Fl(n)+45
890 MHz ~915 MHz : Mobile Transmit,Base receive
935 MHz ~960 MHz : Base Transmit, Mobile receive
For Extended GSM Fl(n)=890+0.2*n 1 ≤n≤ 124 Fu(n)=Fl(n)+45 Fl(n)=890+0.2*(n-1024) 975 ≤n≤ 1023
880 MHz ~915 MHz : Mobile Transmit,Base receive
925 MHz ~960 MHz : Base Transmit, Mobile receive
For DCS Fl(n)=1710.2+0.2*(n-512) 512≤n≤885 Fu(n)=Fl(n)+95
1710 MHz ~ 1785 MHz : Mobile Transmit,Base receive
1805 MHz ~ 1880 MHz : Base Transmit, Mobile receive
For PCS Fl(n)=1850.2+0.2*(n-512) 512 ≤n≤ 810 Fu(n)=Fl(n)+80
1850 MHz ~1910 MHz : Mobile Transmit,Base receive
1930 MHz ~1990 MHz : Base Transmit, Mobile receive
** Fl(n)= frequency value of the carrier , Fu(n)= corresponding frequency value in upper band

1.3. Item Name and Usage

G800, GSM digital cell phone, is supercompact, superlight mobile communication terminal for personal use. It has a 900MHz, 1800MHz, and 1900MHz frequency band and adopts GSM, DCS, and PCS mode having excellent spectrum efficiency, economy, and portability.

This product is GSM Cellular type portable phone, adopting 1-cell Li-ion battery and power saving circuit to maximize its operation time. Also, it is equipped with a fixed snap-in antenna and its color LCD with font built in enables both Chinese and English text service. And power control(basic feature of GSM), security feature, voice symbol feature, and variable data rate feature are used appropriately to ensure its best performance. This product consists of a handset, battery pack, and Travel charger.

1.4. Characteristics

1) All the active devices of G800 are made of semiconductors to ensure excellent performance and semi-permanent use.

2) Surface mounting device (SMD) is used to ensure high reliability, compactness and lightness.

3) G800 adopts the Silabs's AERO I RF transceiver, which is CMOS RF front-end for multi-band GSM digital cellular handsets. The AERO I's highly-integrated architecture eliminates the IF SAW filter, low noise amplifiers (LNAs) for three bands, transmit and RF voltage-controlled oscillator (VCO) modules, and more than 60 other discrete components found in conventional GSM handsets to deliver smaller, more cost effective GSM solutions that are easier to design and manufacture.

4) G800 is designed to perform excellently even in the worst environment

SECTION 2. Electrical Specifications

2.1. General E-GSM / DCS / PCS Band

Mobile Transmit Frequency	880 MHz ~ 915 MHz / 1710 MHz ~1785 MHz / 1850MHz ~ 1910MHz
Mobile Receive Frequency	925 MHz ~ 960 MHz / 1805 MHz ~ 1880 MHz / 1930MHz ~1990MHz
The Number of Time Slot	8
The Number of Channels	174 / 374 / 299
Channel Spacing	200 kHz
Power Supply	Rechargeable Li-Ion Battery 3.7V/640mAH,950mAH
Operating Temperature	-10℃ ~ +55℃
Dimension	81(H) ×41(W) ×19.6(D) mm (SLIM)
Weight	80.08 g

2.2. Transmitter E-GSM / DCS / PCS Band

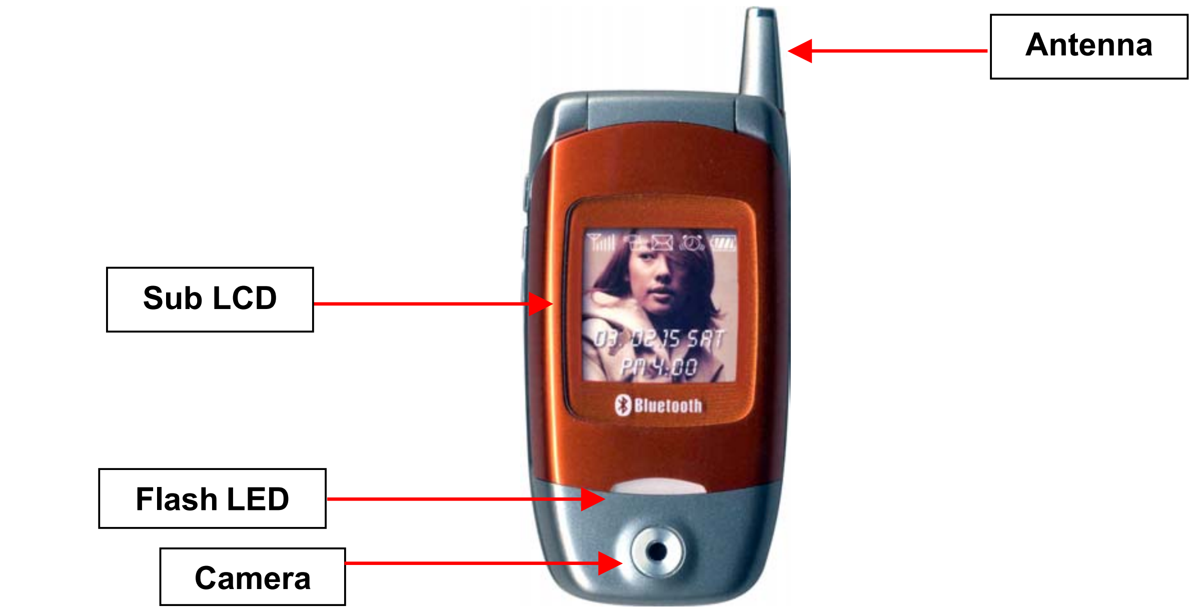
Maximum Output Power	33±2 / 30±2 / 30±2 dBm
Frequency Error	±90Hz / ±180Hz / ±180Hz
Phase Error	RMS < 5° , PEAK < 20°
Minimum Output Power	5±5 / 0±5 dBm / 0±5 dBm
Power Control	5~19(2 dB Step)) / 0~15(2 dB Step) / 0~15(2 dB Step)
Output RF Spectrum	TS 100 910V6.2.0
Switching Transient	TS 100 910V6.2.0
Intermodulation attenuation	
Conducted Spurious Emissions	**EGSM and DCS** Allocated a channel; -36dBm 9kHz ~ 1GHz -30dBm 1GHz ~ 12.75GHz Idle mode; -57dBm 9KHz ~ 1GHz -47dBm 1GHz ~ 12.75GHz with the following excoptions -59dBm 880MHz ~ 915MHz -53dBm 1.71GHz ~ 1.785GHz -76dBm 1900 ~ 1920MHz, 1920 ~ 1980MHz, 2010 ~ 2025MHz, 2210 ~ 2170MHz
	PCS Allocated Channel; -36dBm 9KHz~ 1GHz -30dBm 1GHz~ 12.75GHz Idle mode; -57dbm 9kHz ~ 1000MHz -53dBm 1850MHz ~ 1910MHz -47dBm 1GHz ~ 12.75GHz

2.3. Receiver

Reference Sensitivity	For GSM900 small MS :-102dBm	
	For DCS1800 / PCS1900 class3 MS : -102dBm	
For Adjacent interference	C/Ic	9 dB
For Adjacent(200KHz) interference	C/Ia1	-9 dB
For Adjacent(400KHz) interference	C/Ia2	-41 dB
For Adjacent(600KHz) interference	C/Ia3	-49 dB

SECTION 3 Operation

3.1. Name of each part



3.2. Display(Dual LCD)

Parameter	Projected Actual(MAIN LCD)
Display	Color TFT LCD with white LED back lighting 262144 colors European Character : (font size : 16×16) 6 lines x 16 characters Chinese Character : (font size : 16×16) 6 lines × 7 characters
Model	COM18T1188DEB(CASIO)
Module Dimen.	36.5(W) x 55.1(H) x 5.1(D) mm
Effective Area	28.42(W) x 35.52(H) mm (1.8 inch)
Number of Dots	128(W) x RGB(W)x 160(H) dot
Dot pitch	74(W) x 222(H) um

Parameter	Projected Actual(SUB LCD)
Display	Full Graphic FSTN LCD with white LED back lighting Pixels : 96 x 48 European Character : (font size : 7×15) 1 lines x 12 characters Chinese Character : (font size : 16×16) 1 lines × 6 characters
Model	COM18T1188DEB(CASIO)
Module Dimen.	36.5(W) x 55.1(H) x 5.1(D) mm
Effective Area	23.04(W) x 23.04(H) mm (1.3 inch)
Number of Dots	128(W) x RGB(W) x 128(H) dot
Dot pitch	60(W) x 180(H) um

3.3. Keypad

	Market Goal	Projected Actual	Comments
English Keypad	0-9, *,# Send (Color) End/Pwr (Color) Up, Down, WAP Soft1, Soft2, CLR * Key: Vib. Mode # Key: Auto Lock 0/+Key: nternational 2 Volume Keys	0-9, *,# Send (Color) End/Pwr (Color) Up, Down, WAP Soft1, Soft2, CLR * Key: Vib. Mode # Key: Auto Lock 0/+ Key: International 2 Volume Keys	Meets Goal. (Industrial design sample required) Meets Goal Keys for VR and Lock International Volume up/down

3.4. Camera Module

Product Name	PO1030KC-MS21
Optical Format	1/4.5 inch
Effective pixel array	640 x 480
Unit Pixel size	5.2um x 5.2um
Module size	7mm x 6mm x 5.5mm +-0.1mm
Operating voltage	2.6V
Apeture	F#2.8+-5%

SECTION 4. Theory of Operation

4.1. Logic Section

4.1.1 DC Distribution and Regulation Part

Applying battery voltage and pressing "END" key on the key pad short-circuits "Ground" and "_ PowerON".ADP3522(U103)control that power manage regarding power on/off in handset
Pressing POWERKEY on the key pad is active on the handset.
This will turn on all the LDOs ,when POWERKEY is held low. The power of RF Tx power amplifier is supplied directly by the battery.

4.1.2 Logic part

4.1.2.1 Summary

The logic part consists of AD6526 ARM7 microprocessor-combined GSM-ASIC, COMBO(flash ROM & SRAM), AD6521 VBC Chip. AD6526 is GSM-ASIC chipset implemented for GSM terminal's system control and baseband digital signal processing.

Major parts used in the logic part are as follows:

1) AD6526 : U101, [ARM7 Processor Core + GSM Signal Processing] ASIC
2) AD6521 : U102, Voiceband Baseband Codec
3) COMBO MEMORY(Flash ROM : U104, 128Mbit Flash Memory + 32Mbit SRAM)

Baseband Digital Signal Processing

AD6526 is a GSM core device containing ARM7 CPU core. AD6526 is 160 pin PBGA package, consisting of terminal chips. The function and characteristics of clock are as follows:

Complete single chip GSM Processor

Channel codec sub-system

- Channel coder and decoder
- Interleaver and Deinterleaver
- Encryption and Decryption

Control Processor Subsystem including

- Parallel and serial Display interface
- Keypad Interface
- SIM Interface
- Control of RADIO subsystem
- Real Time Clock with Alarm

☞ Configuration by Function of AD6526

1 Microprocessor Core

AD6526 has a built-in ARM7 microprocessor core, including microprocessor interrupt controller, timer/counter, and DMA controller. And besides, 32bit data path is included, and up to 8Mbyte addressing is enabled and can be extended up to 16Mbyte. Although external clock should be provided to operate the microprocessor, this core uses 13MHz VCTCXO to provide clock.

2 Input Clock

Main Clock(13 MHz):

This is the clock needed for the microprocessor built in AD6526 to operate.

VC-TCXO(13 MHz) , 32.768KHz Clock:

This is the system reference clock to control SLEEP mode.

This is the clock derived from 13MHz VC-TCXO clock, provided by RF part. It is the timing reference clock for GSM signal processing.

3 DSP Subsystem

This is a GSM signal processing part in GSM mode, consisting of speech transcoding and Channel equalization as follows:

Speech transcoding

In full rate, the DSP receives the speech data stream from VBC and encodes data from 104kbps to13kbps. Using algorithm is Regular Pulse Excitation with Long Term Prediction (RPE-LTP).

Equalization

The Equalizer recovers and demodulates the received signal

The Equalizer establishes local timing and frequency references for mobile terminal as well as RSSI calculation.

The equlization algorithm is a version of Maximum Likelihood Sequency Estimation(MLSI) using Viterbi Algorithm.

☞ GSM Core and RF Interface

Transmitter:

AD6521 VBC receive data at 270kbps and use an on chip lock-up table to perform GMSK modulation. A pair of 10bit matched differential DACs convert the modulated data and pass I and Q analog data to the transmit section of the radio system.

Receiver:

The receiver I and Q signals are sampled by a pair of APCS at 270kbps.

The I and Q samples are transferred to the EGSMP through a dedicated receive path serial port.

4 RF Interface

This interfaces the RF part to control power amplifier, Tx LO buffer amplifier, VC-TCXO, and AGC-end on transmit/receive paths in the RF part.

Transmitter Interface:

This transmits TX_AGC signal to Tx AGC amplifier to adjust transmit power level and sends Ramp_DAC signal to the RF part to control power amplifier.

Receiver Interface:

This transmits RX_AGC signal to Rx AGC amp. to adjust receive path gain.

5 General Purpose ADC Support

The AD6521 includes a general purpose 10bit auxiliary ADC with four multiplexed input channel

These are used for measurment of battery voltage ID , temperature and accessory ID.

6 USC(Universal System Connector) Interface

A Typical GSM handset requires serial connections to provide data during normal phone operation manufacturing,testing and debugging.

7 General Purpose Interface

The AD6526 provides 32 interface pin for control of peripheral devices.

All GPIO pins start up as inputs. Additional purpose inputs and outputs are available under SW control.

8 Speech Transcoding

In full rate mode, the DSP receive the speech data stream from the VBC and encodes data from 104kbps to 13kbps.Using algorithm is Regular Pulse Exitation with Long Term Prediction as specified GSM Recommandation

9 Power Down Control Section

1) Idle Mode Control:

If IDLE/ signal turns 'Low', transmitter section becomes disabled.

2) Sleep Mode Control:

If IDLE/ and SLEEP/ signals turn 'Low', all the sections except for VC-TCXO circuit become disabled.

3) Receiver & Transmitter Mode Control:

If IDLE/ and SLEEP/ signals turn 'High', all the sections become enabled to perform transmit/receive operation.

4.1.3 Memory Part

Memory consists of COMBO(flash ROM & SRAM).

1 Flash ROM

Flash ROM has a capacity of 128Mbit(16MByte). The main programs of the terminal(call processing, user interface, and diagnostic task) and supplemental programs(NAM program and test program) are stored in the flash ROM. Even if the program version may be changed in the future, customers can download the program.

2 Static RAM

SRAM has a capacity of 32Mbit(4MByte) and stores system parameters, data buffer, and stack of each task in it.

3 Key Tone Generation

All alert signals are generated by the DSP and output to the EVBC.

These alert can be used for the earpiece.

4.1.4 Notification Part

The notification of incoming call is given by melody, vibrator.

Melody:

This is a device sounding alert/melody tones.

The melody datas are stored in flash memory(U104) And generated by Melody IC(U105).

Vibrator:

This is a device enabling vibration. The vibrator data is stored in flash memory(U104)
And generated by U101.C5(GPO_23)pin.

4.1.5 Key Pad Part

To enable key operation to input information, the key matrix is configured using strobe signal of KEYPADROW(0-4) and 5 input ports of KEYPADCOL(0-4). Also, to use the key even at light, the backlight circuit is provided for LED 13.

4.1.6 LCD Module(Display Part)

LCD module consists of LCD , controller, LED-Backlight, and LCD reflector.using dual LCD

Main LCD: 1S/W Icon x 6 lines[(128x3)x160] can be displayed on the LCD panel. 6 icons could be provided by S/W. Controller with English font built in has been used.

Sub LCD: 1S/W Icon x 1 lines(48x96) can be displayed on the LCD panel. 6 icons are provided. Controller with English font built in has been used.

LED-backlight Using illuminates the LCD panel, and LCD reflector enhances LCD display effect.

4.1.7 CAMERA Module

Camera Module is activated by keypad sw27.

Taking a picture, Flash LED is provided to bright dark surroundings, and generated by U101.B12(GPIO2)

4.2. Radio Transceiver Section

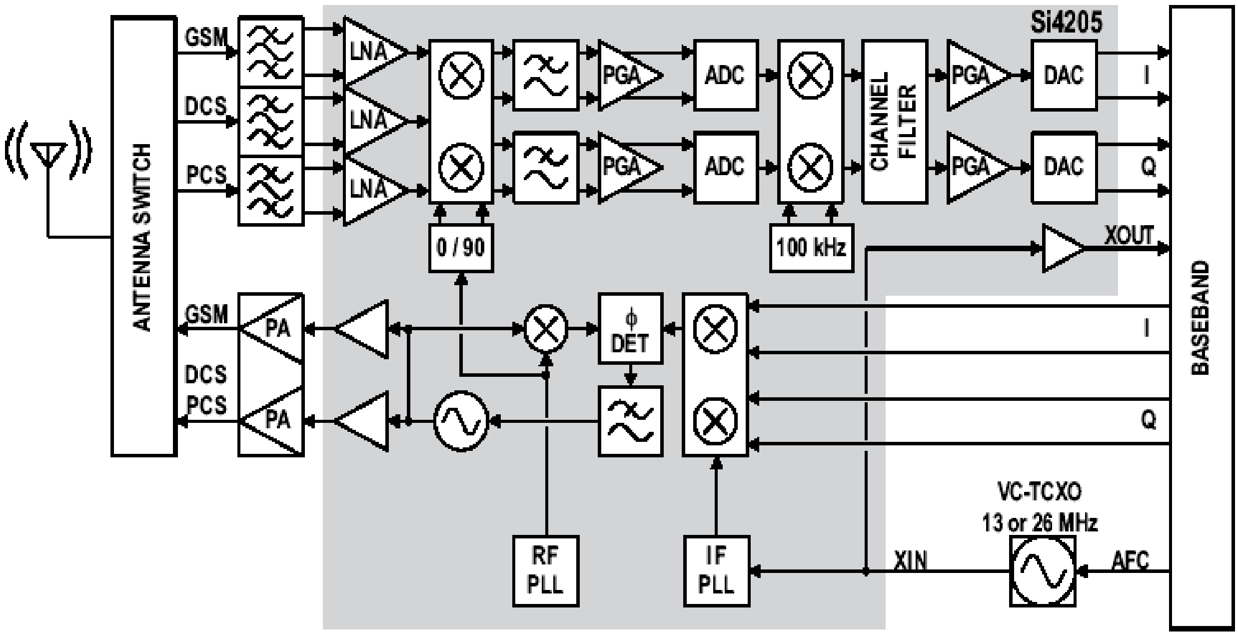


Fig.4-1. RF Transceiver block diagram

The G800's RF Transceiver(U710), which is AERO I, consists of the GSM transmitter,the GSM Receiver, and the RF synthesizer. The highly integrated solution eliminates the IF SAW filter, external low noise amplifiers (LNAs) for three bands, transmit and RF voltage controlled oscillator (VCO) modules, and more than 60 other discrete components found in conventional designs.

The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduced complexity.

The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifer (U701) and uses an offset phase locked loop (PLL) with a fully integrated transmit VCO.

The RF synthesizer includes integrated RF and IF VCO's, Varactors, and Loop filters. The unique integer-N PLL architecture used in the RF synthesizer produces a transient response that is superior in speed to fractional architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

The following Figure shows G800's top view of PCB artworks.

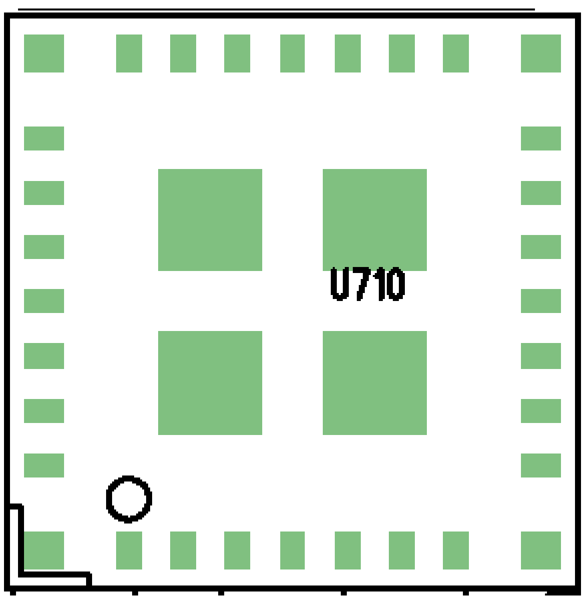


Fig.4-2. Top view of RF Transceiver PCB Layout

4.2.1 DC Distribution and Regulation Part

The battery voltage, in return, is applied to the logic part and RF part via LDO(Low Drop-Out) regulator. As several LDO regulators are used, power can be supplied for each necessary part efficiently. Audio/Logic parts use +2.8V. Si4205 RF Transceiver (U710) and RF3133 Power Amplifier (U701) also use +2.8V DC voltage.

4.2.2 Transciever pin description

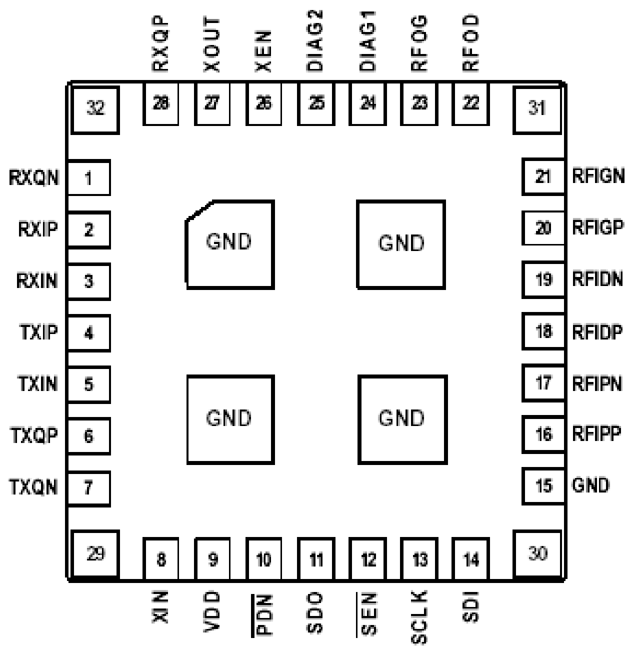


Fig.4-3. Top View of Si4205-BM

Pin Number(s)	Name	Description
1, 28	RXQN, RXQP	Receive Q output (differential).
2, 3	RXIP, RXIN	Receive I output (differential).
4, 5	TXIP, TXIN	Transmit I input (differential).
6, 7	TXQP, TXQN	Transmit Q input (differential).
8	XIN	Reference frequency input from crystal oscillator.
9, 32	VDD	Supply voltage.
10	$\overline{PDN}$	Powerdown input (active low).
11	SDO	Serial data output.
12	$\overline{SEN}$	Serial enable input (active low).
13	SCLK	Serial clock input.
14	SDI	Serial data input.
15, 29–31	GND	Ground. Connect to ground plane on PCB.
16, 17	RFIPP, RFIPN	PCS LNA input (differential). Use for PCS 1900 band.
18, 19	RFIDP, RFIDN	DCS LNA input (differential). Use for DCS 1800 band.
20, 21	RFIGP, RFIGN	GSM LNA input (differential). Used for GSM 850 or E-GSM 900 bands.
22	RFOD	DCS and PCS transmit output to power amplifier. Used for DCS 1800 and PCS 1900 bands.
23	RFOG	GSM transmit output to power amplifier. Used for GSM 850 and E-GSM 900 bands.
24, 25	DIAG1, DIAG2	Diagnostic output. Can be used as digital outputs to control antenna switch functions.
26	XEN	XOUT pin enable.
27	XOUT	Clock output to baseband.

Table 4-1. Pin Description of Si4200DB-BM

4.2.3 Receiver Section

4.2.3.1 An Overview of Receive section

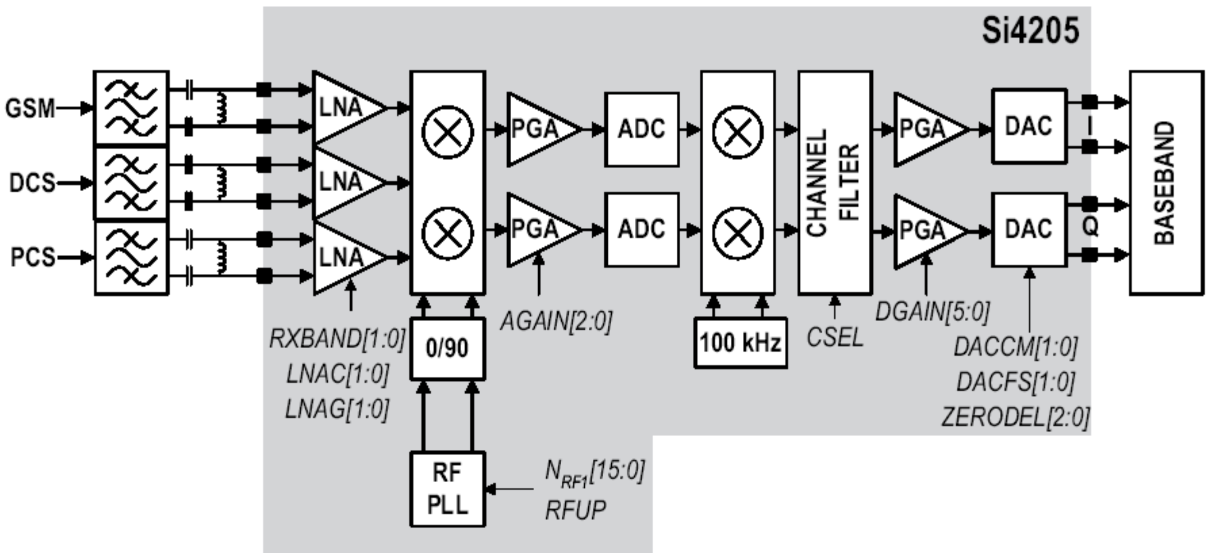


Fig.4-6. Receiver block diagram

G800's Aero I transceiver uses a low-IF receiver architecture which allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF

SAW filter required in conventional superheterodyne architectures. Compared to a direct-conversion architecture, the low-IF architecture has a much greater degree of immunity to dc offsets, which can arise from RF local oscillator (RFLO) self-mixing, 2nd-order distortion of blockers, and device 1/f noise. This relaxes the common-mode balance requirements on the input SAW filters, and simplifies PC board design and manufacturing.

Three differential-input LNAs are integrated on the Aero I transceiver. The GSM input supports the GSM 850 (869–894 MHz) or EGSM 900 (925–960 MHz) bands. The DCS input supports the DCS 1800 (1805–1880 MHz) band. The PCS input supports the PCS 1900 (1930–1990 MHz) band. G800 use all the input ports that are GSM, DCS and PCS inputs.

The LNA inputs are matched to the 150 Ω balancedoutput SAW filters through external LC matching networks. The LNA gain is controlled with the LNAG and LNAC bits.

A quadrature image-reject mixer downconverts the RF signal to a 100 kHz intermediate frequency (IF) with the RFLO from the frequency synthesizer. The RFLO frequency is between 1737.8 to 1989.9 MHz, and is internally divided by 2 for GSM 850 and E-GSM 900 modes. The mixer output is amplified with an analog programmable gain amplifier (PGA), which is controlled with the AGAIN bits in register 05h. The quadrature IF signal is digitized with high resolution A/D converters (APCS).

The ADC output is downconverted to baseband with a digital 100 kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. The response of the IIR filter is programmable to a high selectivity setting or a low selectivity setting. The low selectivity filter has a flatter group delay response which may be desirable where the final channelization filter is in the baseband chip. After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN bits.

The LNAG, LNAC, AGAIN and DGAIN bits must be set to provide a constant amplitude signal to the baseband receive inputs.

DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, and RXQN pins to interface to standard analog-input baseband ICs. No special processing is required in the baseband for offset compensation or extended dynamic range. The receive and transmit baseband I/Q pins can be multiplexed together into a 4-wire interface. The common mode level at the receive I and Q outputs is programmable, and the full scale level is also programmable.

4.2.3.2 Receiver Part

A. Diplexer: Z701

Diplexer consists of Tx filter, having an antenna port, and dual configuration with the transmitting path isolated from the receiving path. A signal receives from the antenna of frequency band which is 942.5 ± 17.5MHz for EGSM bands, 1842.4 ± 37.4 MHz for DCS bands, and 1960.2 ± 30 MHz for PCS bands and transmits it to the saw filter for each band. The Tx filter passes through the output signals of frequency band that is 897.5MHz ±17.5MHz for EGSM bands, 1747.4±37.4 MHz for DCS bnads, and 1880.2 ±30 MHz for PCS bands from the power amplifier and transmits it to the antenna. The maximum insertion loss is about 0.8 dB for the receiving bands at 25° C and about 1.35 dB for the transmitting bands at 25° C.

B. SAW filter (BPF / Band select filter): Z510, Z511, Z512

The **Z510** filter is for the EGSM band signals which range 942.5±17.5MHz with low insertion loss. And the **Z512** filter passes the PCS bands that cover 1960.2±3MHz.

These filters degrade other band signals with high passing loss of 30~60 dB. The EGSM, DCS, and PCS's maximum insertion loss is 3.2 dB.

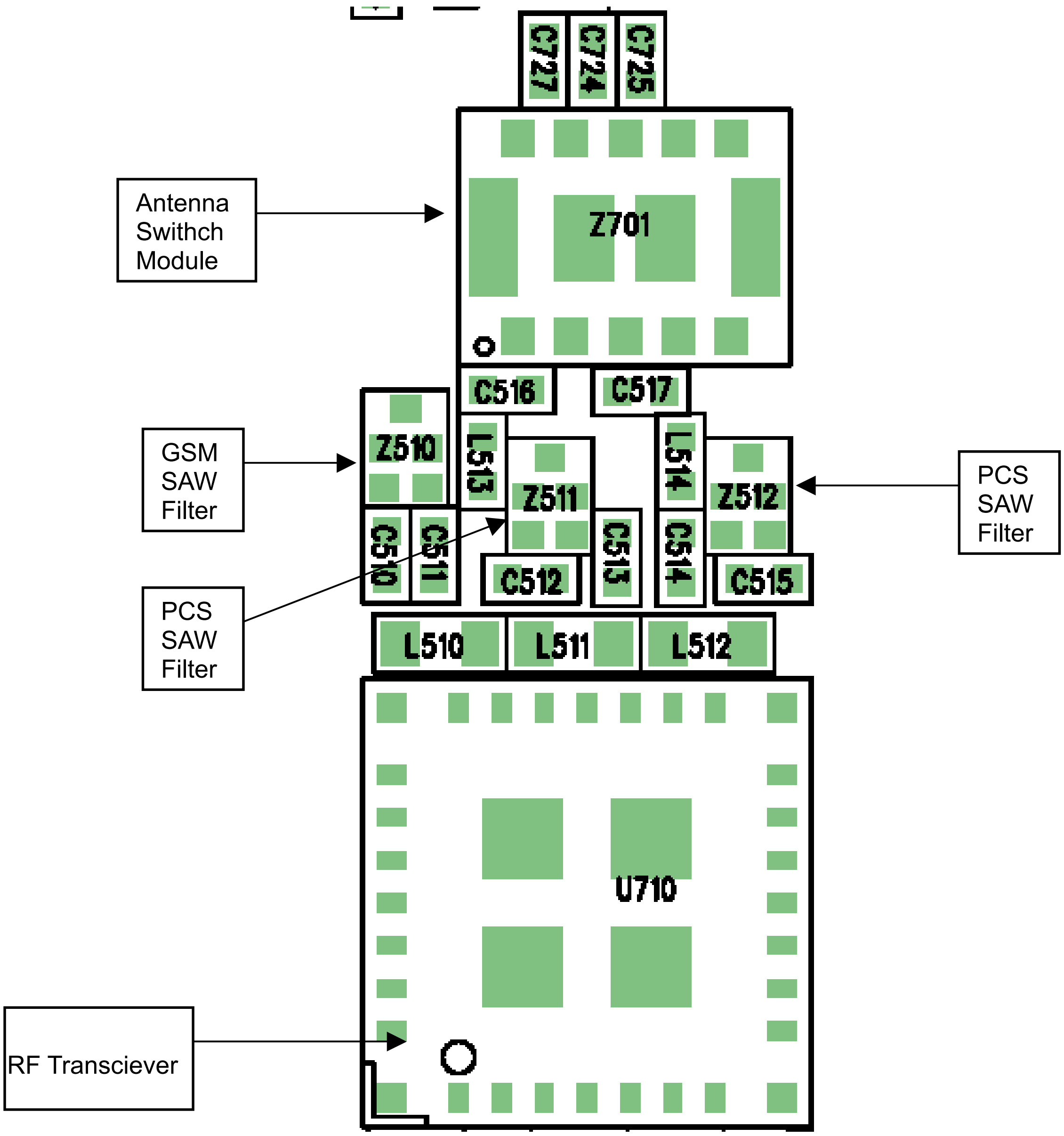


Fig.4-7. Receiver part PCB Layout

4.2.4 Transmit Section

4.2.4.1 An Overview of Transmit Section

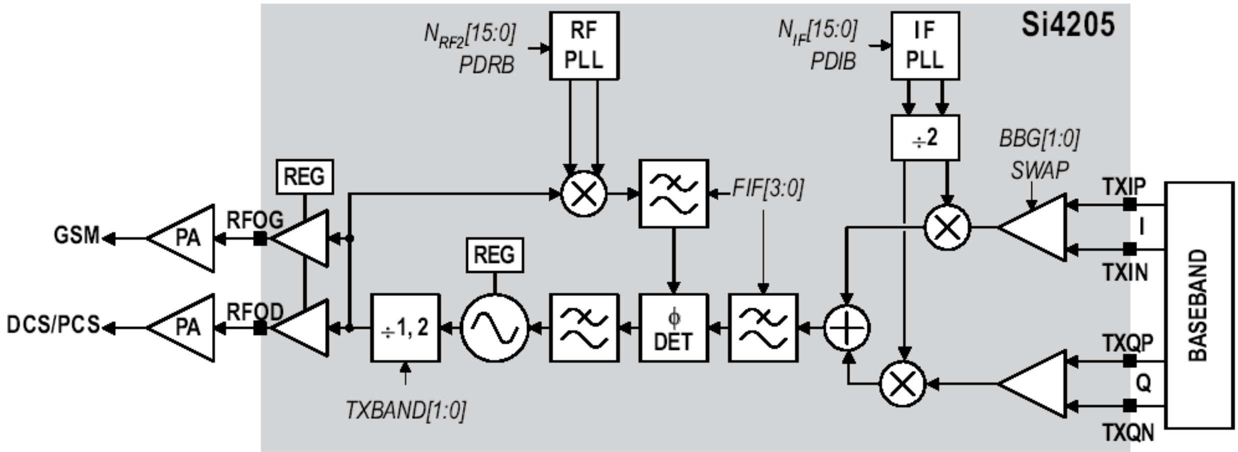


Fig.4-8. Transmitter block diagram

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two output buffers that can drive external power amplifiers (U701), one for the GSM 850 (824 to 849 MHz) and E-GSM 900 (880 to 915 MHz) bands and one for the DCS 1800 (1710 to 1785 MHz) and PCS 1900 (1850 to 1910 MHz) bands. The OPLL requires no external duplexer to attenuate transmitter noise or spurious signals in the receive band, saving both cost and power. Additionally, the output of the transmit VCO(TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA.

A quadrature mixer upconverts the differential in-phase (TXIP, TXIN) and quadrature (TXQP, TXQN) signals with the IFLO to generate a SSB IF signal that is filtered and used as the reference input to the OPLL. The IFLO frequency is generated between 766 and 896 MHz and internally divided by 2 to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz. For the E-GSM 900 band, two different IFLO frequencies are required for spur management. Therefore, the IF PLL must be programmed per channel in the E-GSM 900 band.

The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the PCS 1900 and PCS 1900 bands, and its output is divided by 2 for the GSM 850 and E-GSM 900 bands. The RFLO frequency is generated between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the GSM 850 and E-GSM 900 bands, and low-side injection is used for the DCS 1800 and PCS 1900 bands. The I and Q signals are automatically swapped when switching bands. Additionally, the SWAP bit in register 03h can be used to manually exchange the I and Q signals.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. The cutoff frequency of the filters is programmable.

4.2.4.2 Transmitter Part

A. 6 dB attenuator : Z705, Z706

These passive components are adopted for PAM to operate in a stable output power.

B. ASM(Antenna Switch Module / built in LPF): Z701

These filters pass through the signals of which frequency band of 880MHz~915MHz, 1710MHz~1785MHz, and 1850MHz~1910MHz which is the transmit frequency of GSM, PCS system terminal, and it suppresses other images and spurious frequencies when the terminal transmits GMSK modulated frequencies.

C. Power AMP Module(PAM): Z710

This device amplifies signals ahead of transmiting them through the antenna to provide a sufficient RF power. It has amplification factor of 28dB and efficiency of about 55% typically in GSM band and amplification of 27dB and efficiency of about 52% typically DCS / PCS band.

D. RF Switch connector: J701

RF Swithc connector used to test Mainboard's RF characteristics.

E. Antenna: Antenna Contact Plate J702

This device enables signals to be transmitted and received from BTS by Um interface.

External Antenna can be contacted with Mainboard through Antenna Contact Plate.

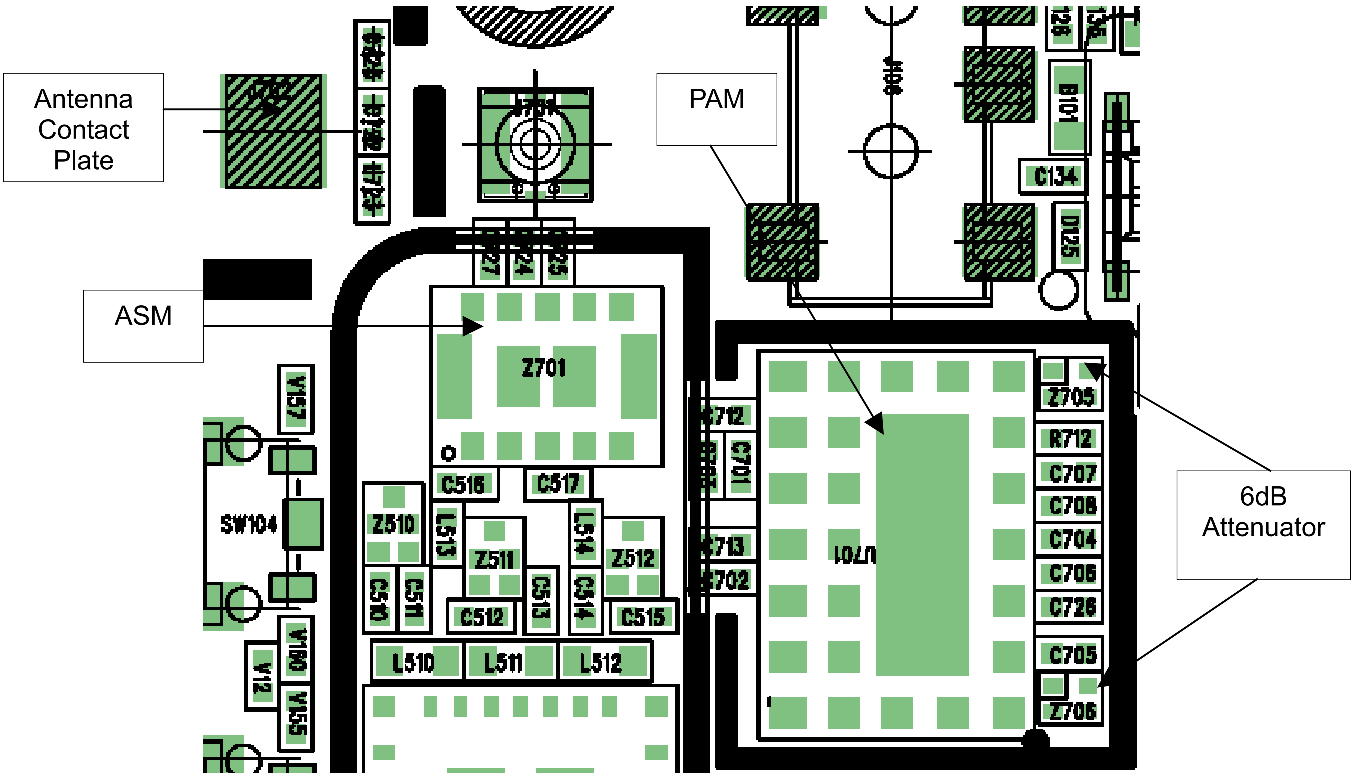


Fig.4-9. Transmit part PCB Layout

4.2.5 Offset PLL

4.2.5.1 An Overview of Offset PLL

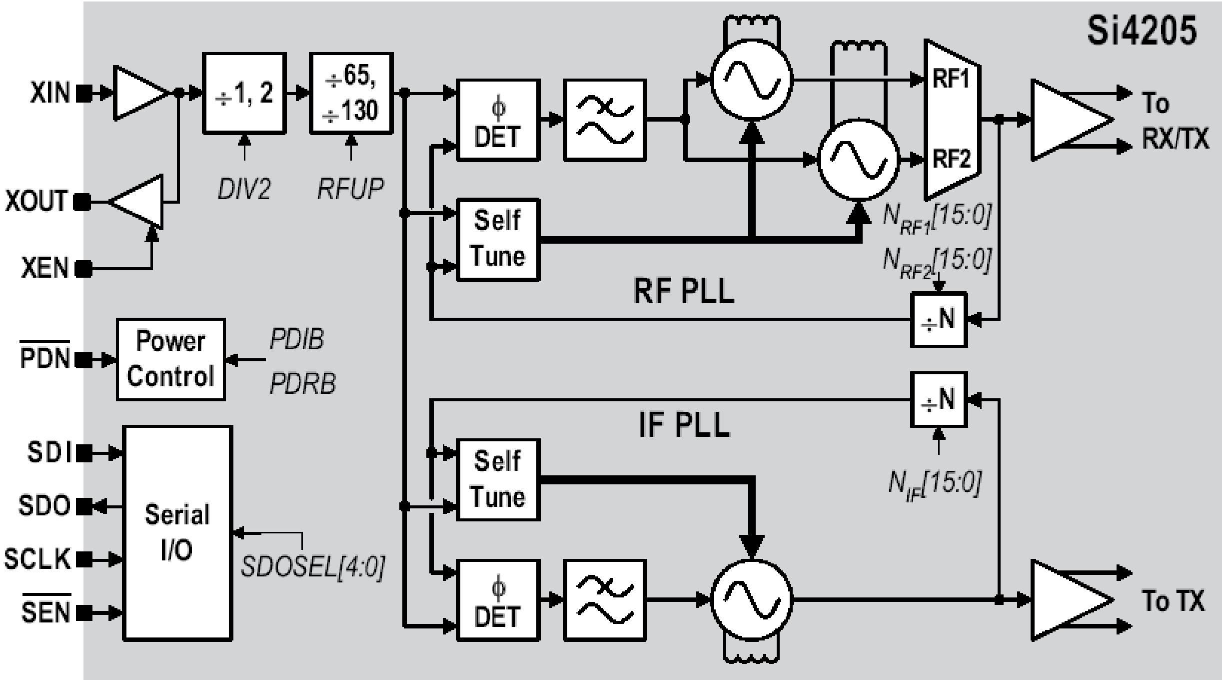


Fig.4-10. Si4205 Frequency Synthesizer Block Diagram

The Aero I transceiver integrates two complete PLLs including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and the RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode. All VCO tuning inductors are also integrated.

The IF and RF output frequencies are set by programming the N-Divider registers, NRF1, NRF2 and NIF. Programming the N-Divider register for either RF1 or RF2 automatically selects the proper VCO. The output frequency of each PLL is as follows:

$$f_{OUT} = N \times f_{\phi}$$

The DIV2 bit in register 31h controls a programmable divider at the XIN pin to allow either a 13 or 26 MHz reference frequency. For receive mode, the RF1 PLL phase detector update rate (f_{ϕ}) should be programmed f_{ϕ} = 100 kHz for DCS 1800 and PCS 1900 bands, and f_{ϕ} = 200 kHz for GSM 850 and E-GSM 900 bands. For transmit mode, the RF2 and IF PLL phase detector update rates are always f_{ϕ} =200 kHz.

4.2.5.2 VC-TCXO(Voltage Controlled Temperature Compensated Crystal Oscillator): V801

This is the mobile station's reference frequency source. Its frequency is 13MHz, this signal is applied to Si4205(U710)_pin8, AD6526(U101) and YMU765(U105).

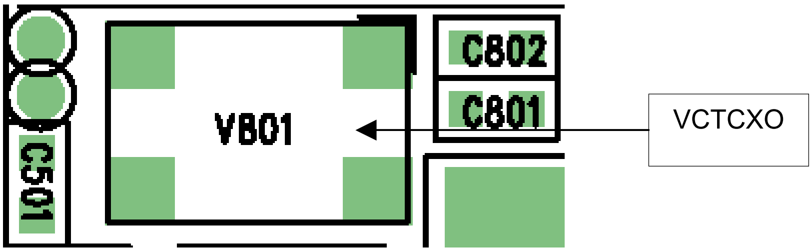


Fig.4-11. Top view of VCTCXO part on the PCB artwork

SECTION 5. Alignment Procedure

5.1. Recommended Test Equipment

Model No.	Description	Maker	Remark
8960	GSM Mobile Station Test Set	Agilent Technologies	
8593E	Spectrum Analyzer	Hewlett Packard	
TDS 340A	Oscilloscope	Tektronix	
FLUKE 87	Digital Multimeter	Fluke	
E3630A	DC Power Supply	Hewlett Packard	
Others	Accessory		Interface Connectors RF Connectors

5.2. Connection of Test Equipment

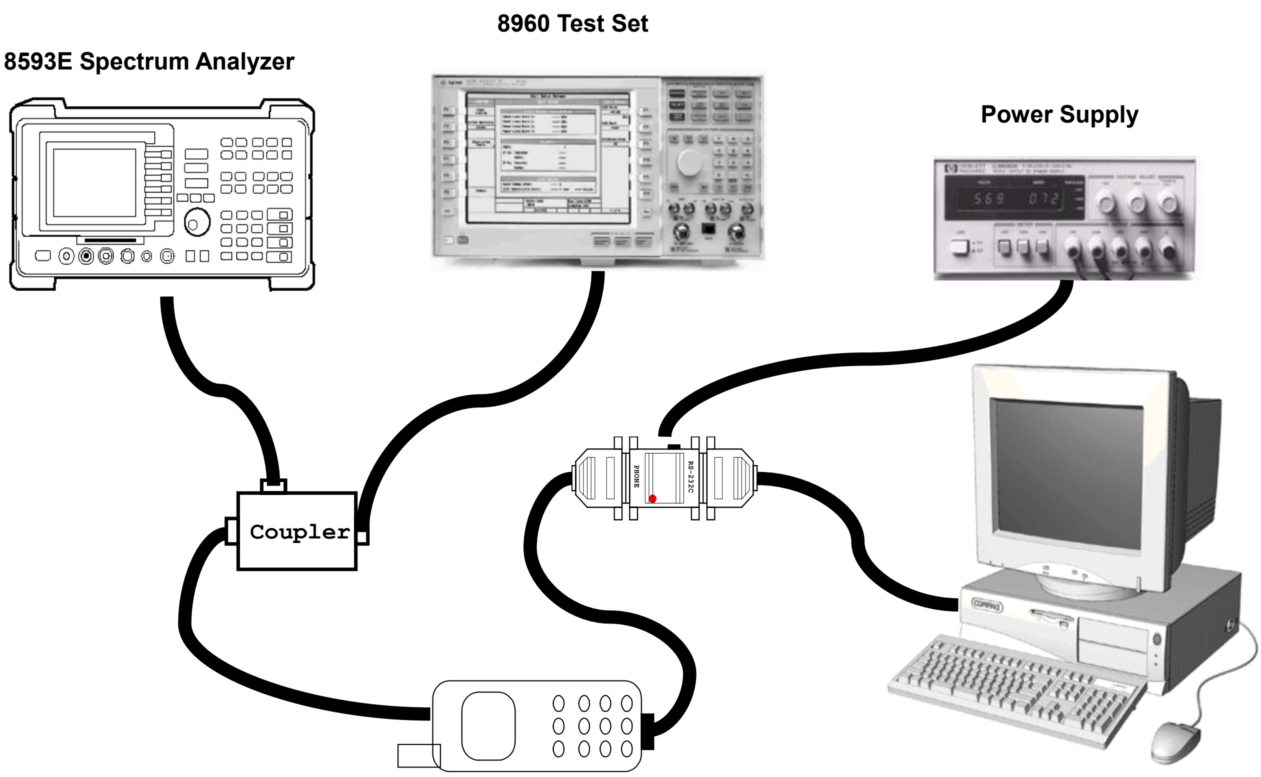


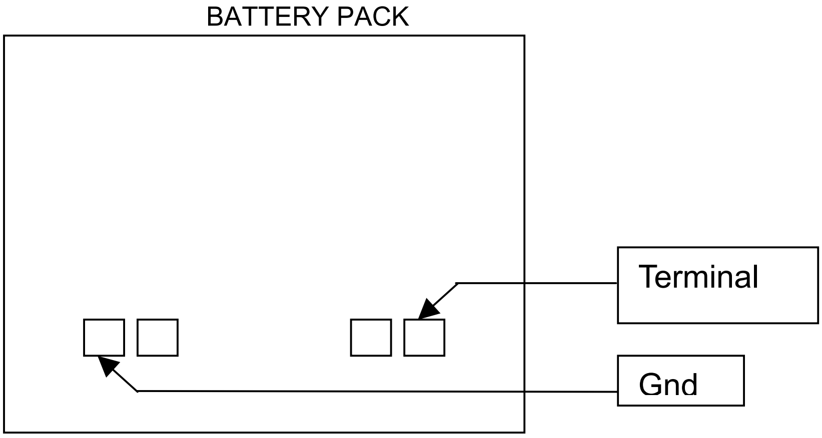
Fig.5-1. Test Set Configuration

SECTION 6. Equipment Repair Procedure

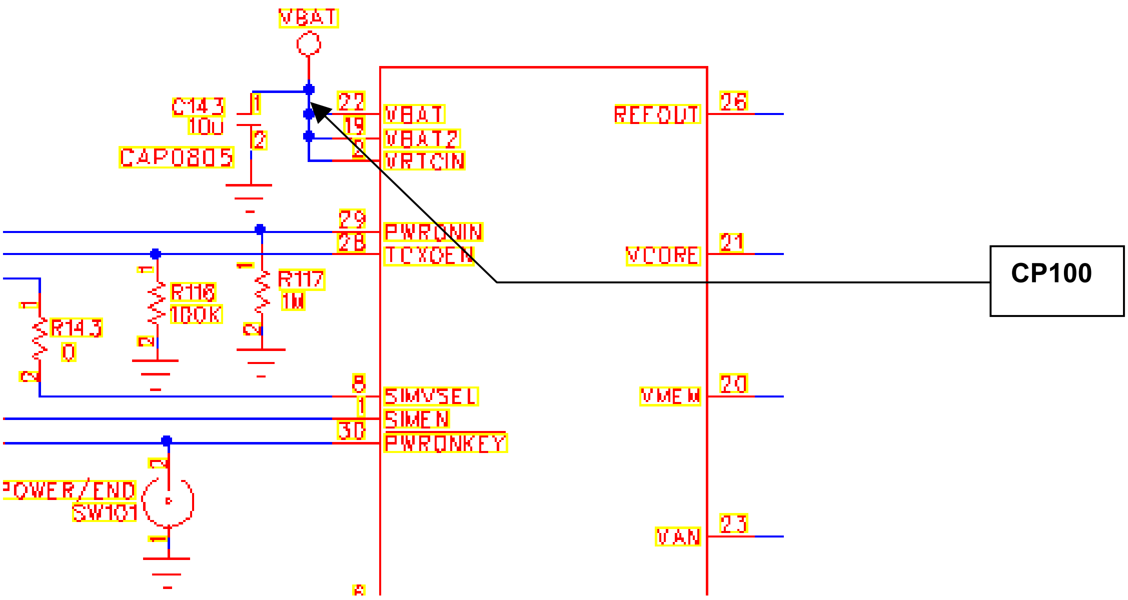
6.1. No Power On with battery Applied.

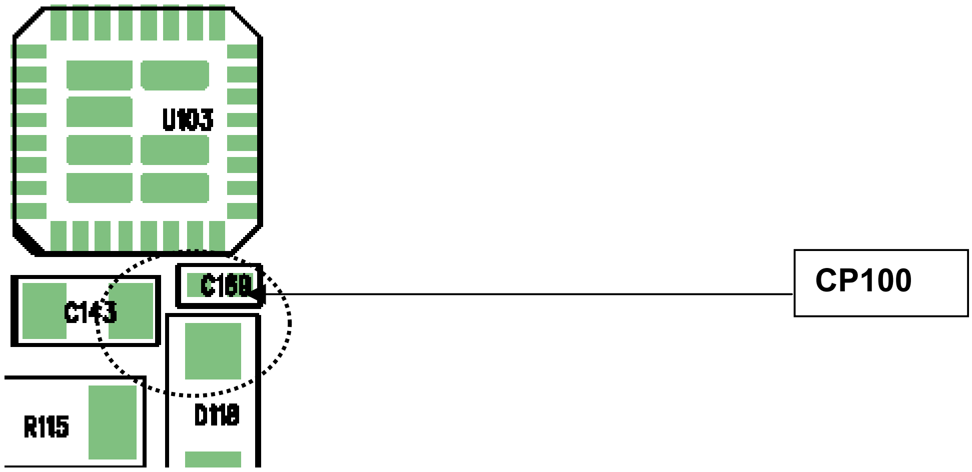
6.1.1 Power CHECK

1.Check battery power : 3.5V~4.2V.

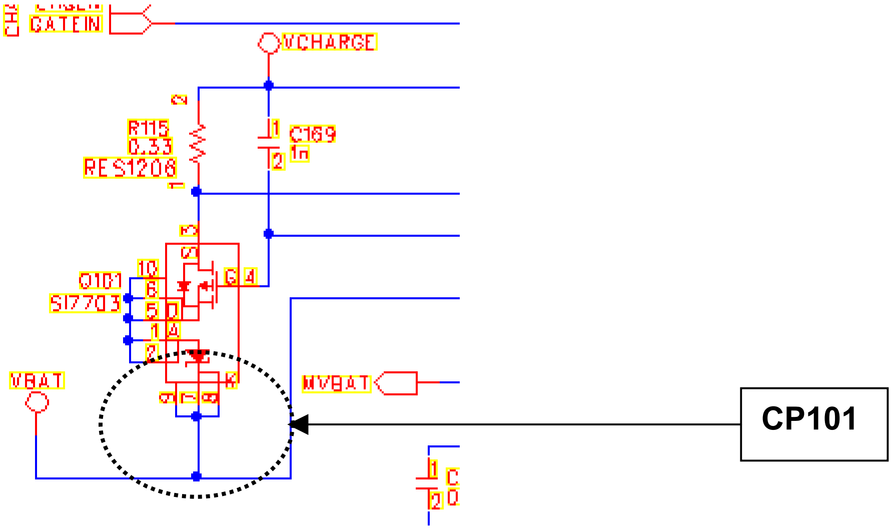


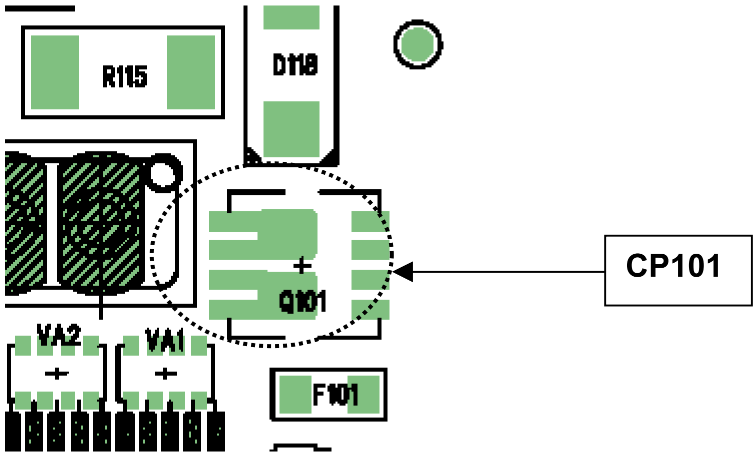
2.Check to see if U103.22,19,2 pin voltage is same with battery power : CP100



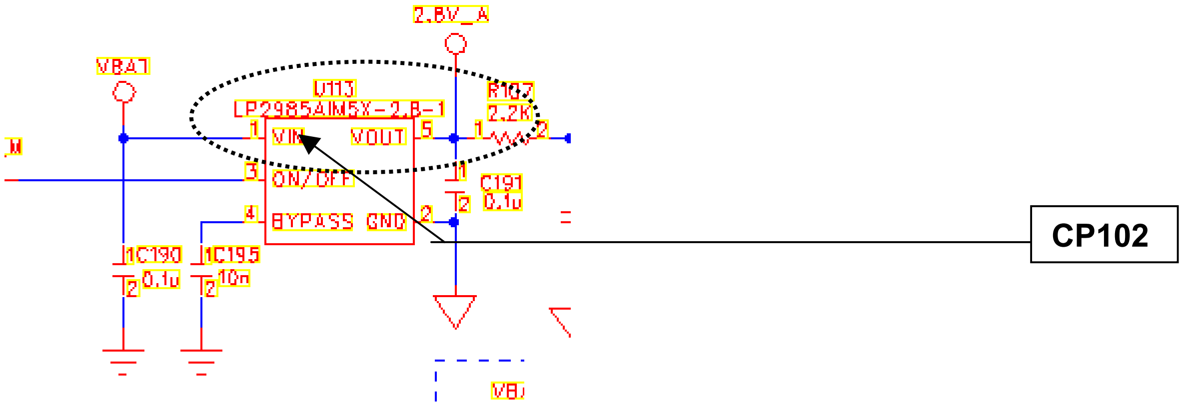


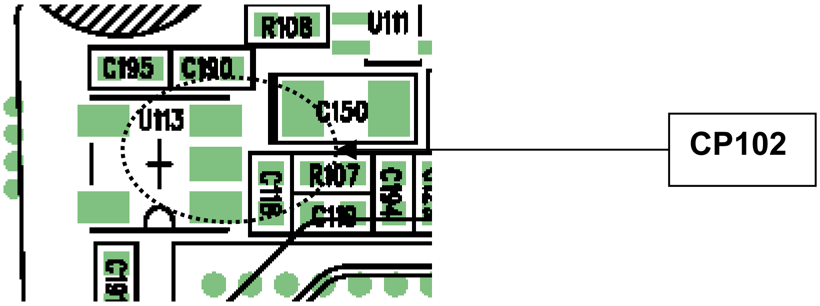
3. Check to see if Q101.7,8 and 9 pin is same with battery power : CP101



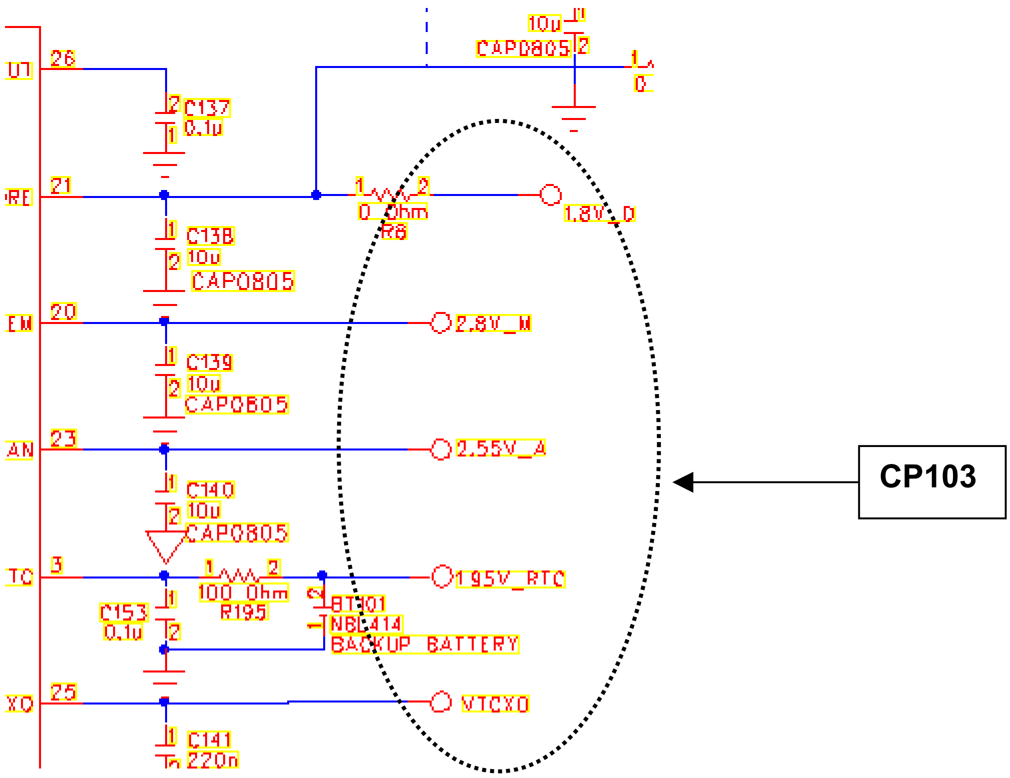


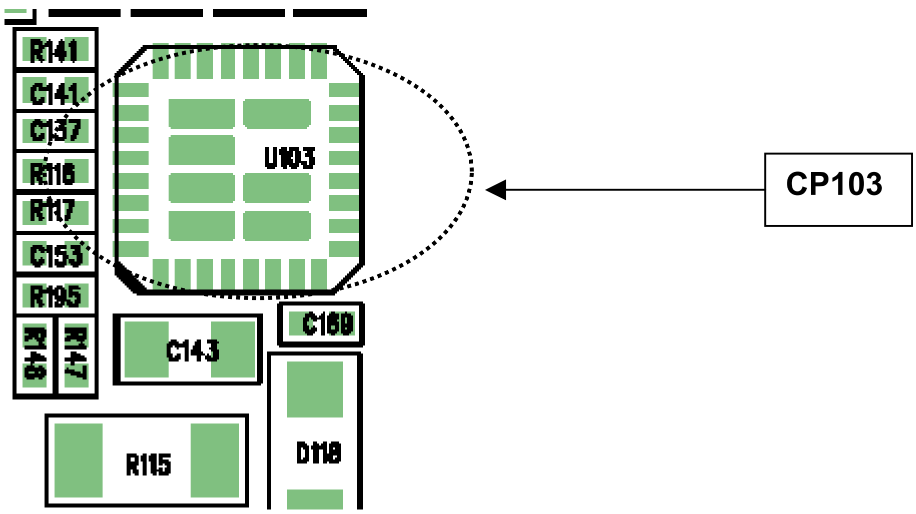
4. Check to see if U113 .1 pin is same with battery power : CP102





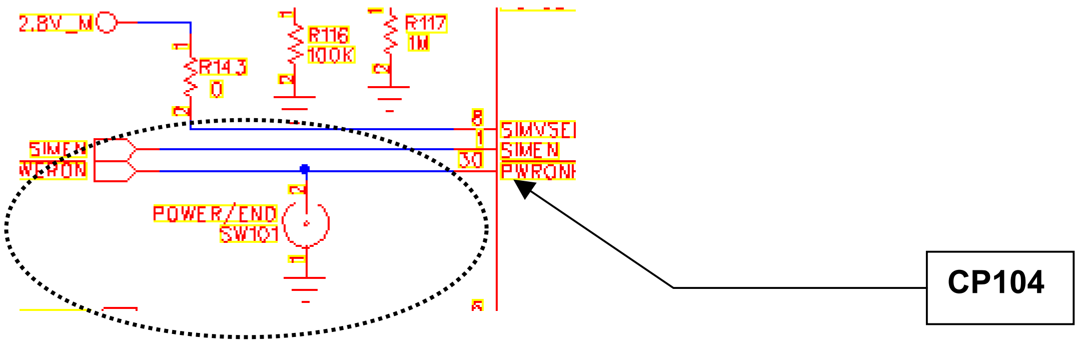
5. Check to see if U103. 21,20.23 and 3 pin is 1.8V, 2.8V, 2.55V_A,1.95V_RTC : CP103



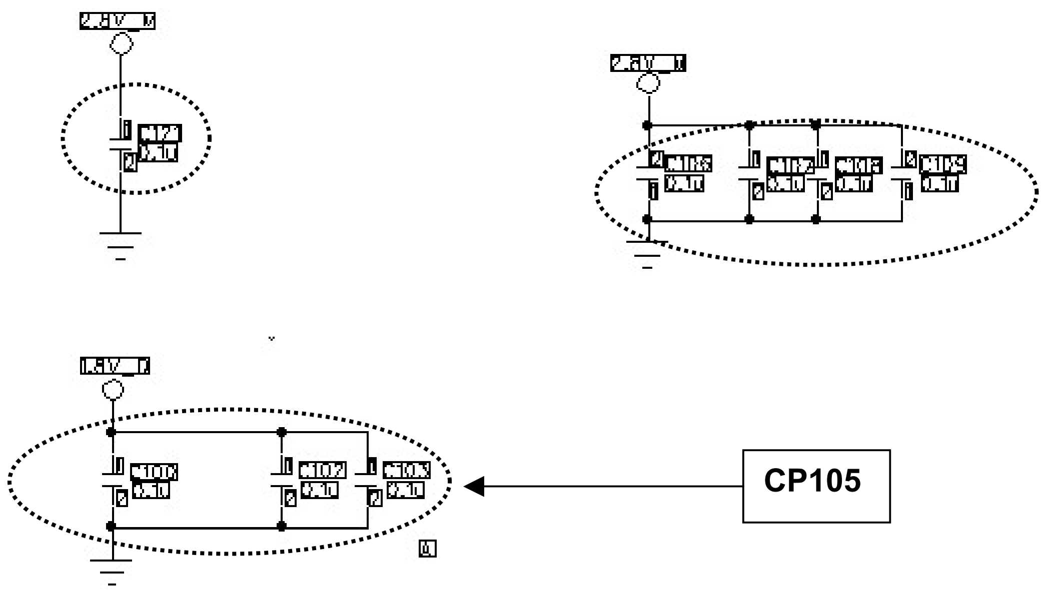


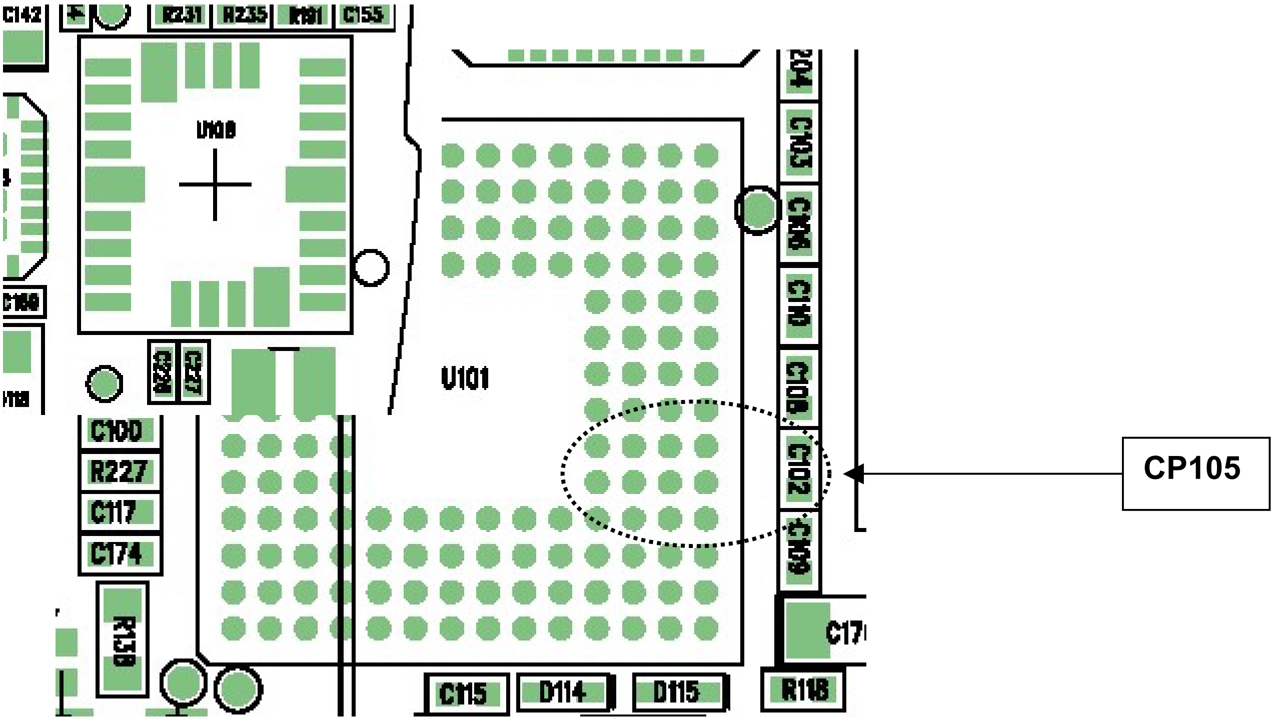
6. Check to see if U103.30 pin becomes to 0V : CP104

Pressing “END” key to turn on equipment.

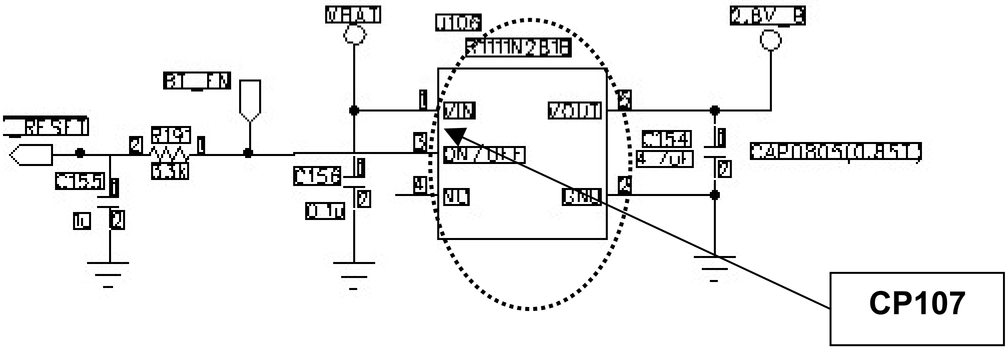


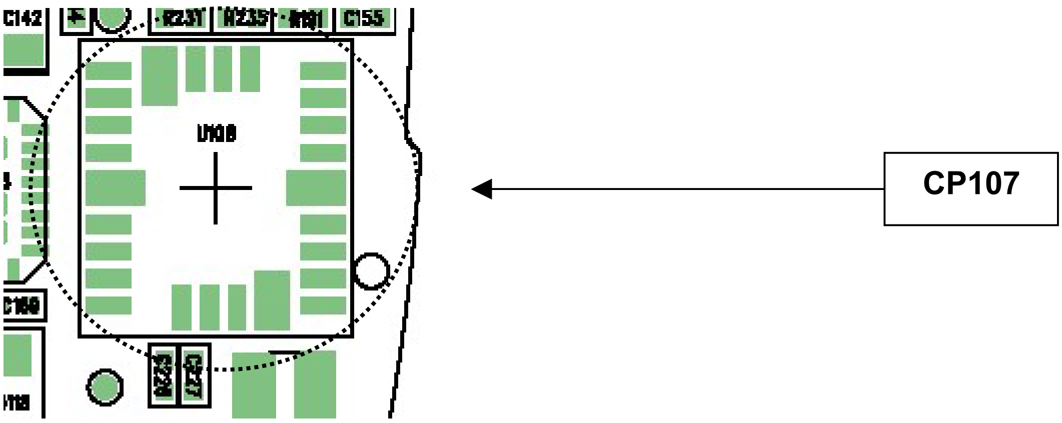
7. Check to see if C106~109,C121,C100,C102,C103 is 2.8V_M, 1.8V_D : CP105





8. Check to see if U106.5 pin and J103.28 pin is 2.8V_EXT : CP107

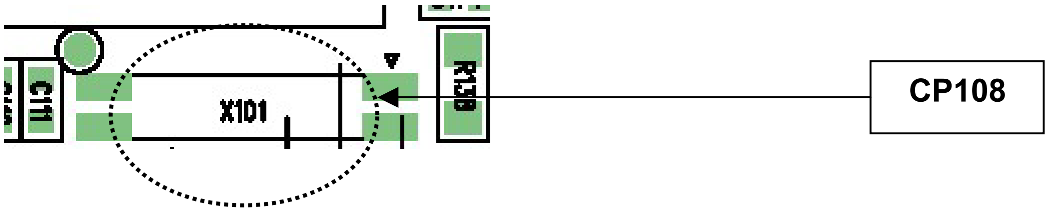




6.1.2 Oscillation CHECK

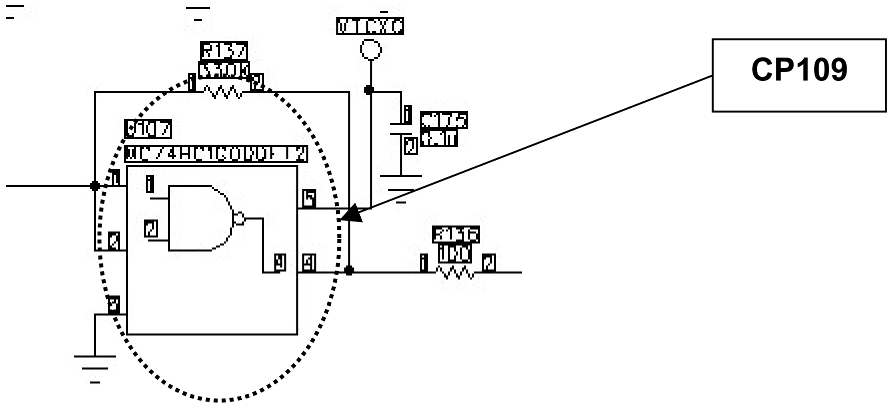
Check to see if U101 No. A3 and B3 pin is oscillated(32.768KHz) : CP108

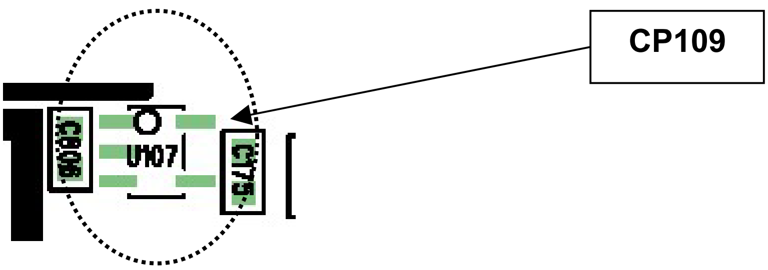
NO → Check R138 and then replace X101



Check to see if U107.4 pin Master Clock(13MHz). : CP109

NO → Check U107 No. 1.2 pin and then check the PCB pattern, soldering





6.1.3 KEYPAD LED Not in Operation(blue)

1.Check to see if R129. 1 pin is around 2.8V(duty:80%, 256Hz) : CP110

NO → Check R129 and Q102 and then replace those

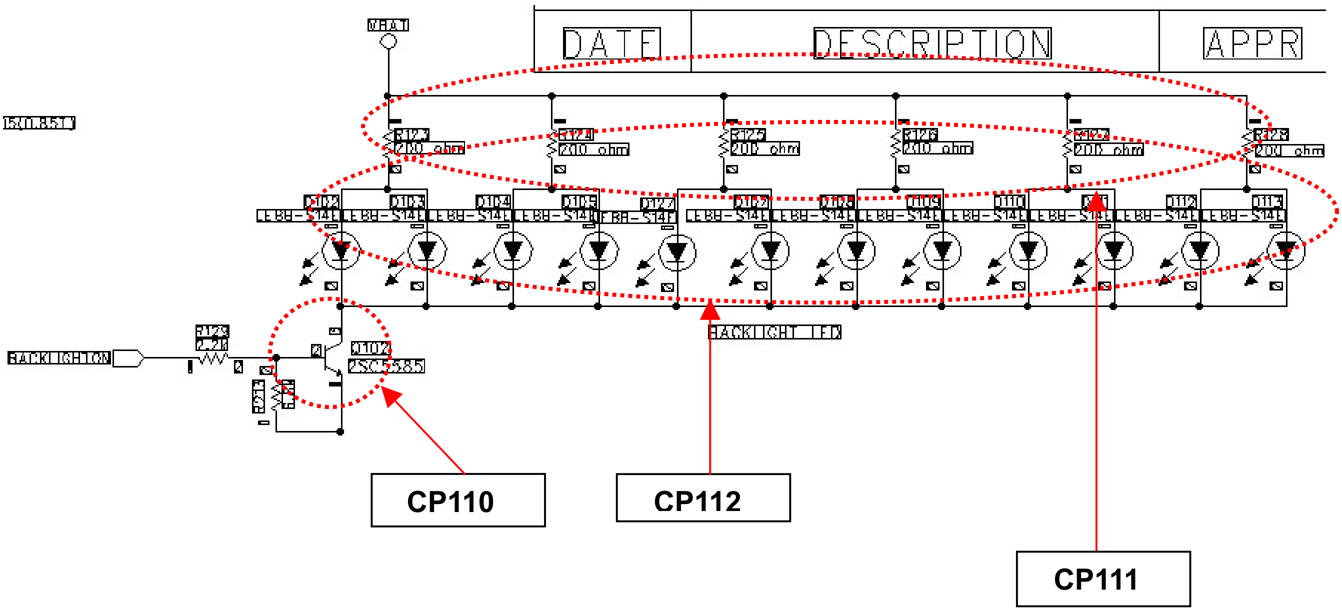
2.Check to see if R123.124.125.126.127.128 is same with battery voltage : CP111

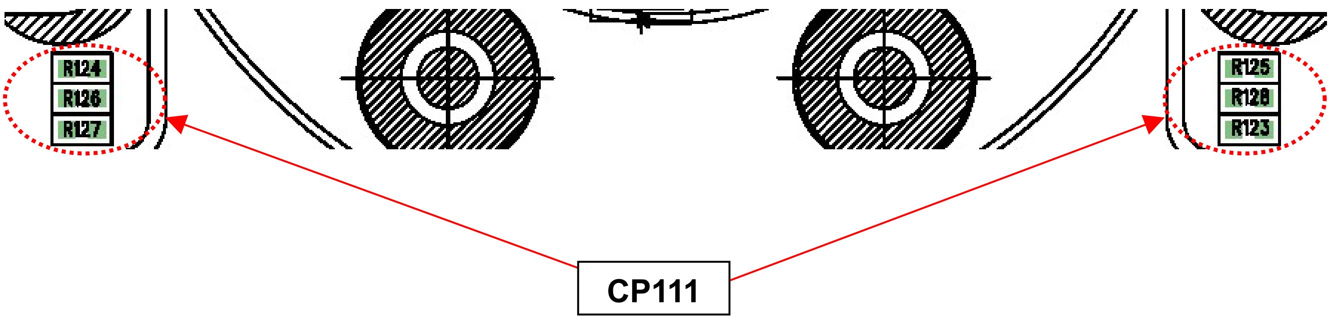
NO → Check the PCB pattern between battery and the resistors.

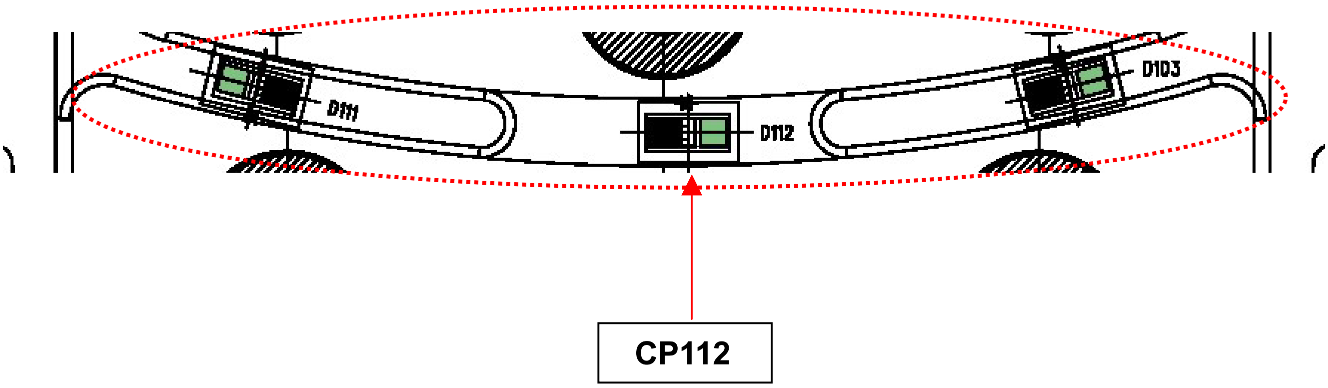
NO → Replace the resistors.

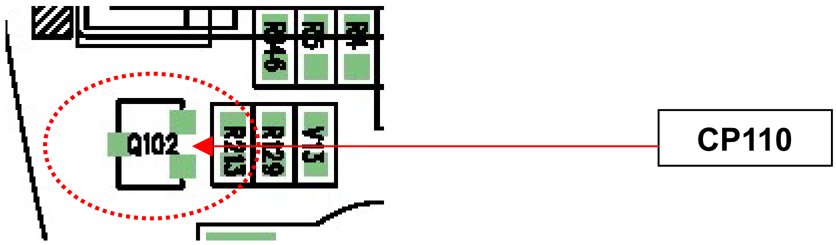
3.Check to see if D102.103.104.105.106.107.108.109.110.111.112.113 is well operated by multimeter : CP112

NO → Replace the LEDS.





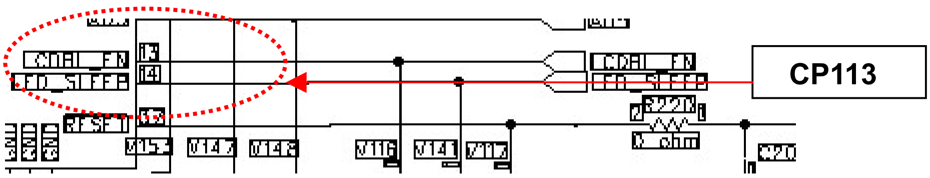


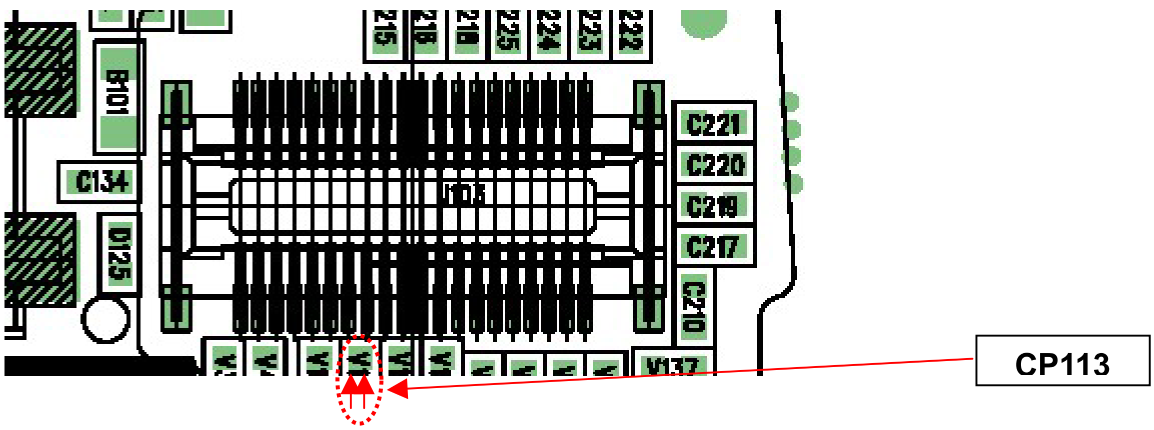


6.1.4 LCD Backlight Not in Operation(White)

1. Check to see if J103.13 pin is around 2.8V(duty:80%, 256Hz) : CP113

NO → Check J103 and resoldering





6.2. Audio Part (Earpiece, Hands-free Earphone, Microphone, Hands-free Mic)

6.2.1 No receiving tone heard(Ear-piece)

1.Check to see if U102 Nos. F10.A9 and J8(C118.C119) is 2.55V_A : CP114

2.Check to see if U102 No. A7(C124) is around 1.2V : CP115

Set to HP8922M to connect a call and then set to 1Khz.

3.Check U102 No. K8 and K7(C147,C148)pins(Ear Signal) for wave form : CP116

NO→ Replace U102.

4.Check Earpiece No. Audio1 and Audio2(C198.1,C199.1) pin for wave form : CP117

NO → Replace Earpiece.

6.2.2 No Receivng tone heard (Hands-free Earphone)

1.Check to see if U102 Nos. F10.A9 and J8(C118. C119) is 2.55V_A: CP114

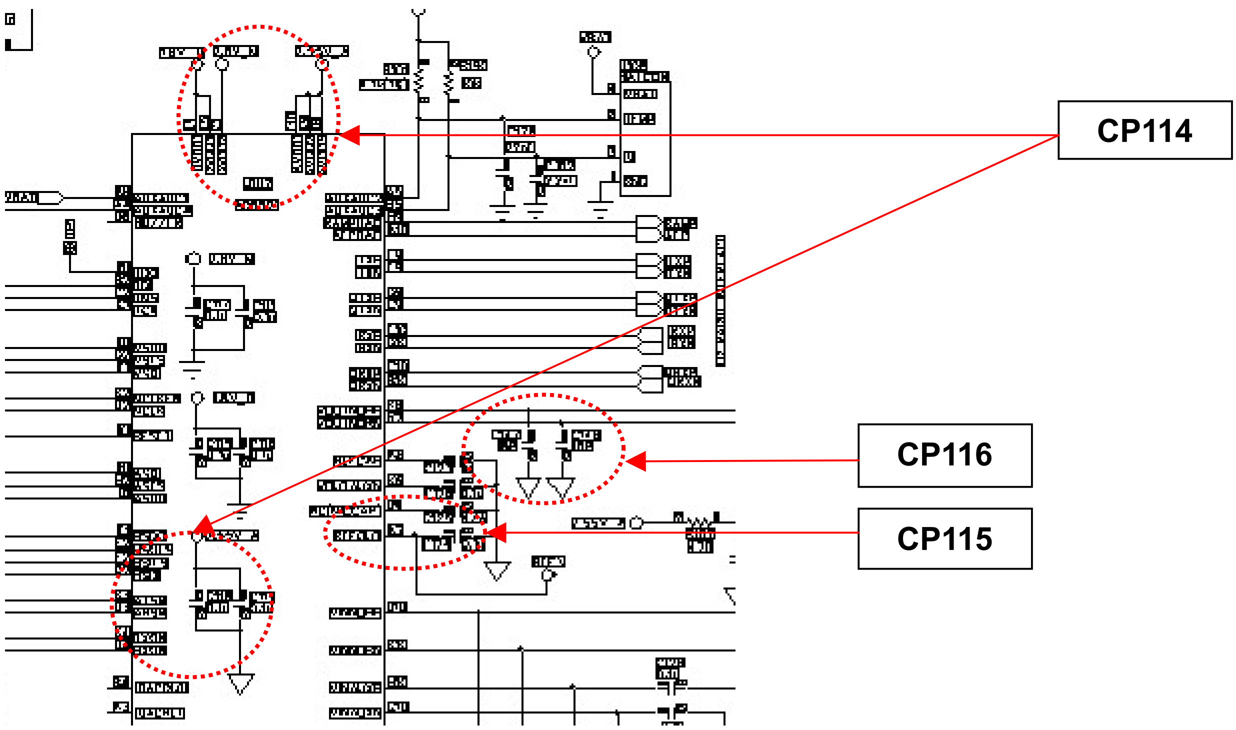
2.Check to see if 102 No. A7(C124) is around 1.2V : CP115

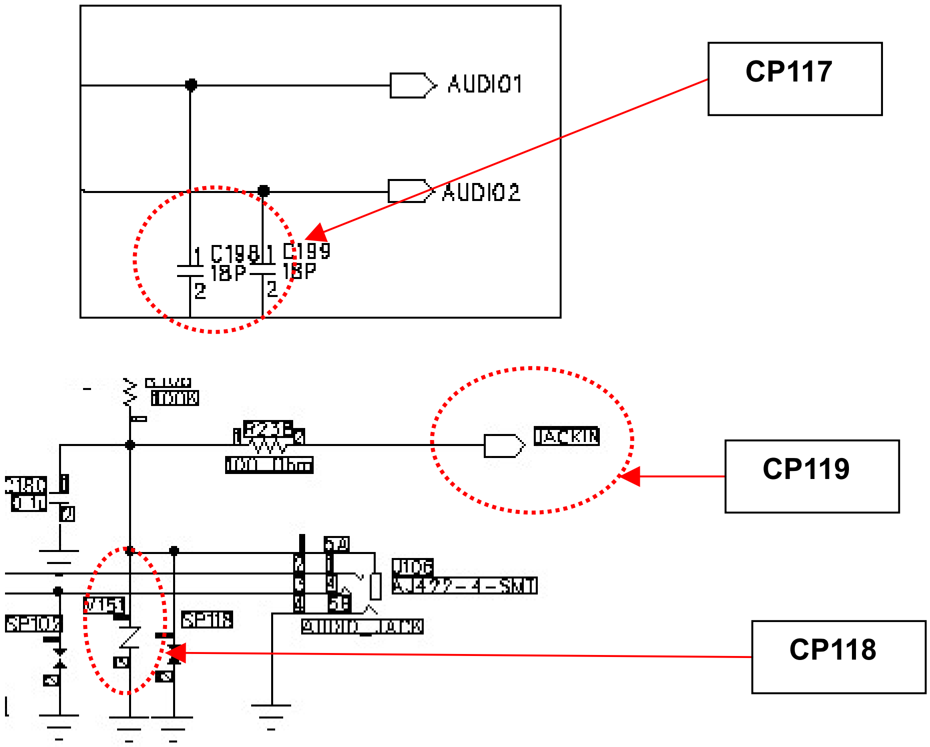
3.Check to see if U101 No. B11(V151) is around 0V: CP118

NO → Check to see J106 : CP119

Set to HP8922M to connect a call and then set to 1Khz.

4.Check Hands-free Earphone





6.2.3 Side Tone Not transmitted (Ear-piece)

Repeat 6-2-1 No receiving tone heard.(Ear-piece)

1.Check to see if Mic + pin is around 1.8V : CP120

NO → Check that R104,C181 is cold solder,broken,short to the other PCB pattern or not

If you find out any defective part, you replace it.

Set to HP8922M to connect a call and then set to 1Khz with Echo audio mode.

2.Check U102 No. J10(C132) pins for wave form : CP121

NO→ Replace MIC

6.2.4 Side Tone Not transmitted (Hands-free Mic.)

Repeat 6-2-2 No receiving tone heard.(Hands-free Earphone).

1. Check to see if U102 No. H10(C130) pin is 2.5V : CP122

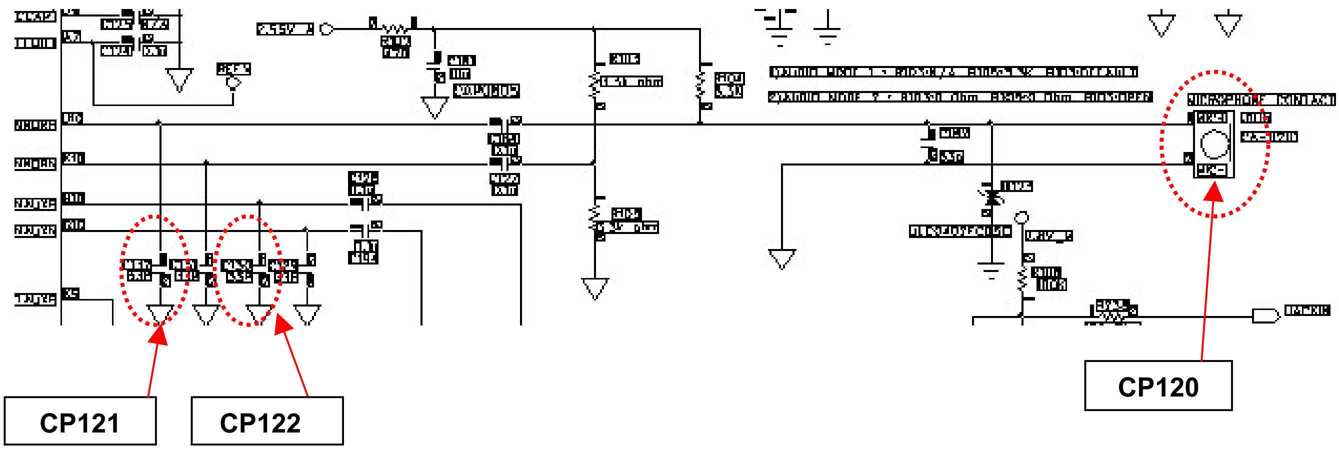
NO → Check that R107, R108, C128 and C151 is cold solder,broken,short to the other PCB pattern or not.

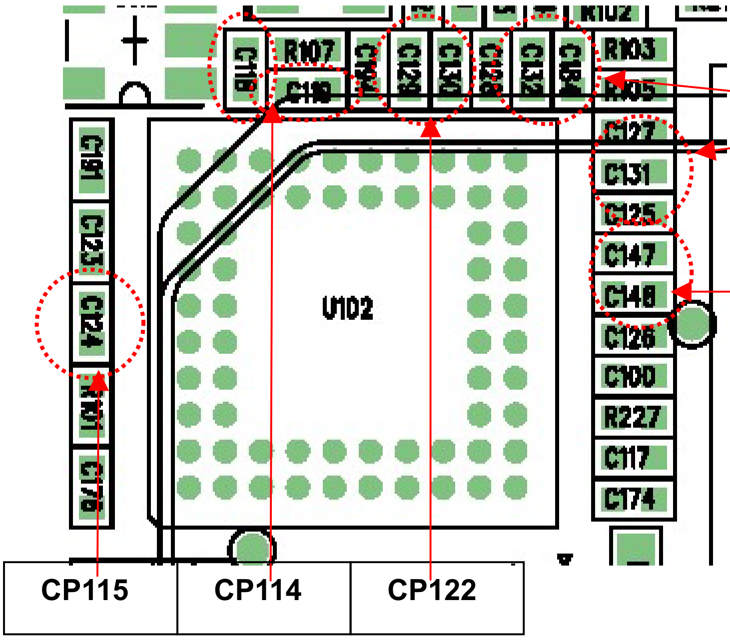
If you find out any defective part, you replace it

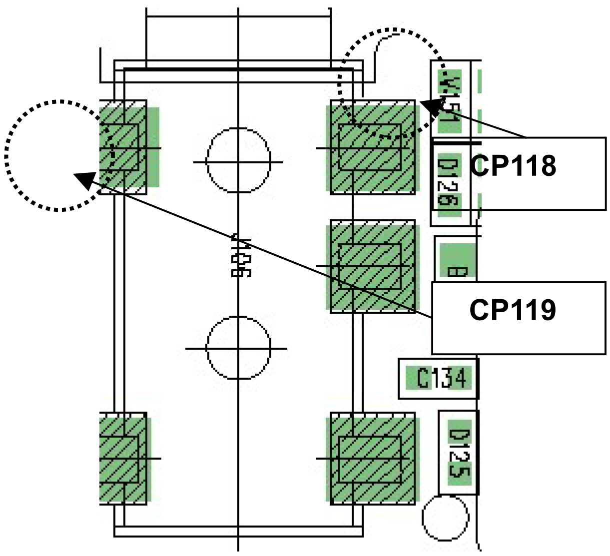
Set to HP8922M to connect a call and then set to 1Khz with Echo audio mode.

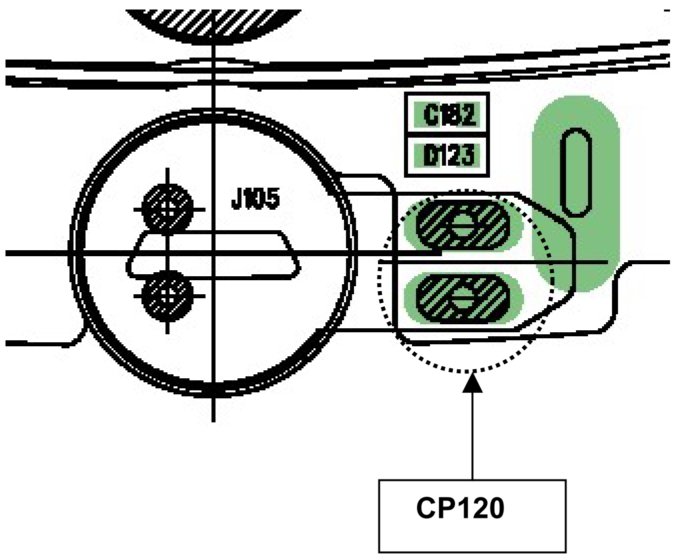
3. Check U102 No. H10(C130) pins for wave form : CP122

NO → Replace Handsfree Mic.


CP121
CP122
CP120

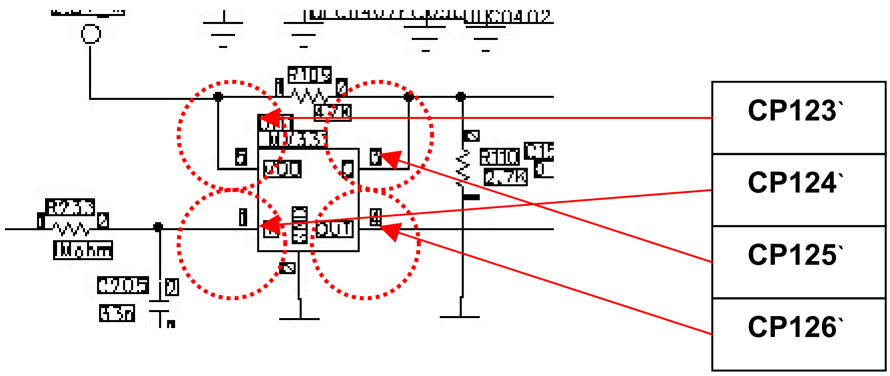

R107
C118
R103
C127
C131
C125
C147
C148
C126
C100
R227
C117
C174
C191
C123
C124
C178
U102
CP121
CP116
CP115
CP114
CP122

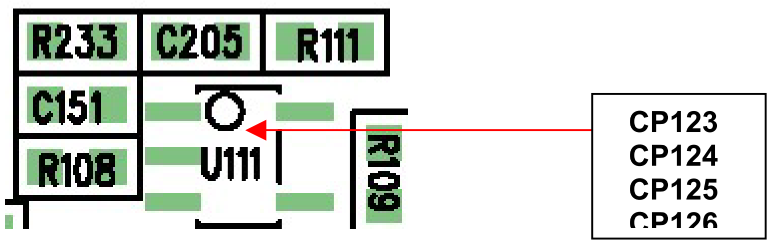

CP118
CP119
C134
D125


C182
D123
J105
CP120

6.2.5 Hook Switch not working

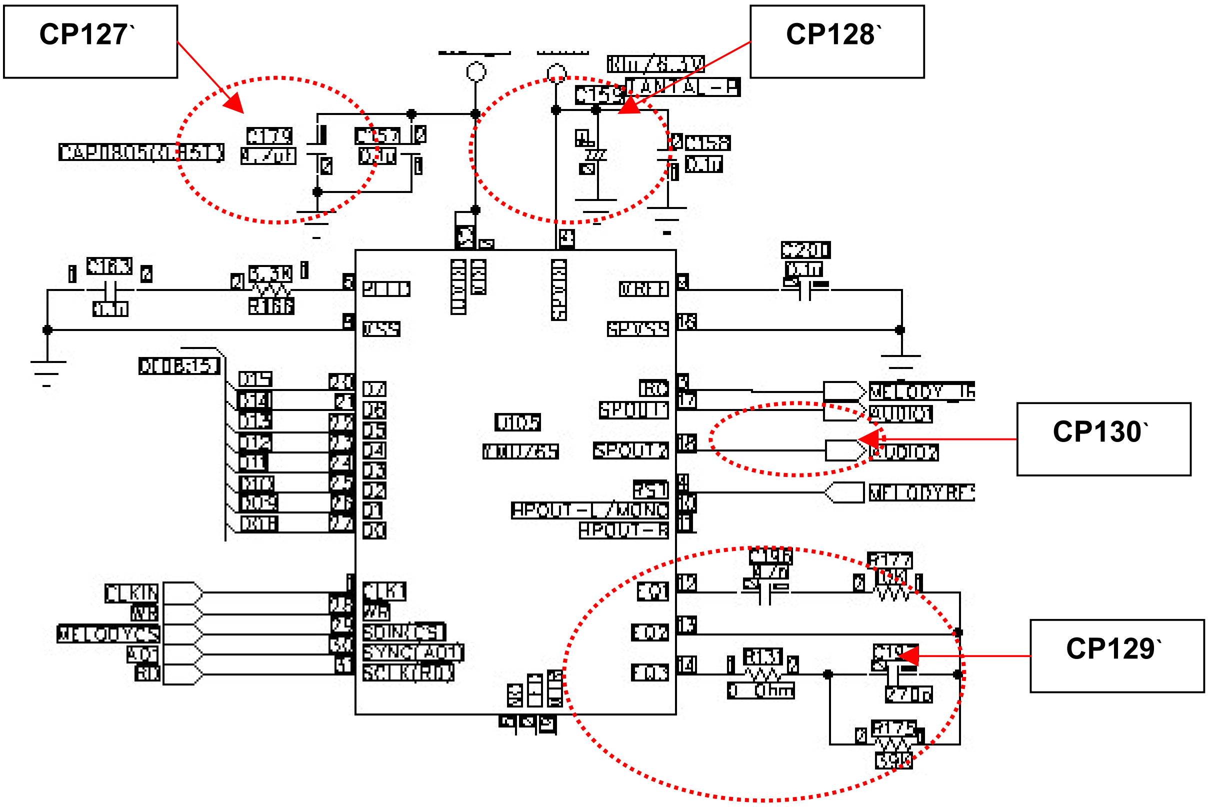
1.Check to see if U111 No.5 is 2.8V : CP123
2.Check to see if U111 No.1 is 0V during pressing Hook Switch : CP124
3.Check to see if U111 No.3 is around 0.15V : CP125
NO → Check that R109 and R110 cold solder,broken,short to the other
PCB pattern or not
If you find out any defect, you replace it
4.Check to see if U111 No.4 is around 0V When you press Hook Switch : CP126
NO→ Check that U111 or R109 cold solder,broken,short to the other
PCB pattern or not
If you find out any defect, you replace it

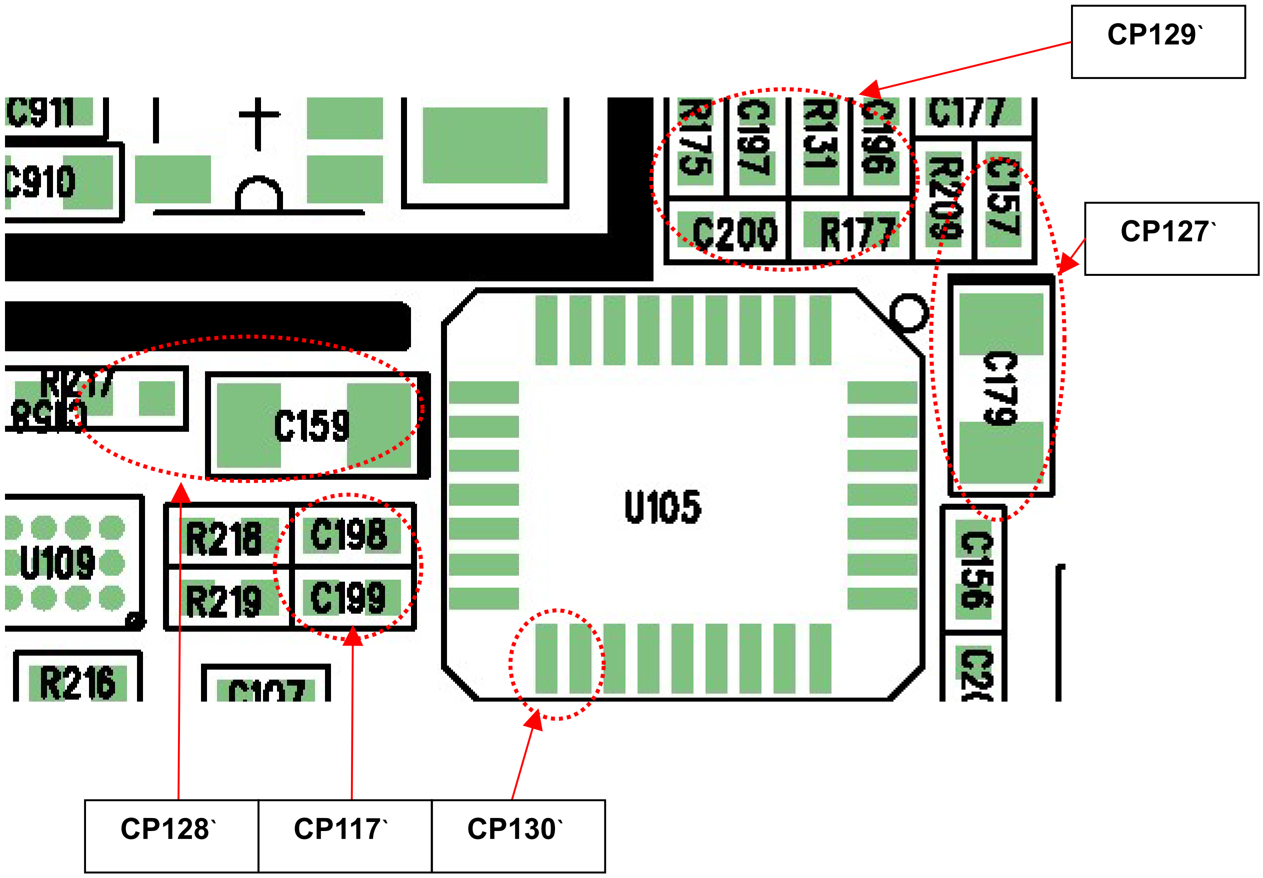




6.3. 6.2.6 Melody not ringing

1.Check to see if U105.7 , 32 is 2.8V_EXT : CP127
2.Check to see if U105.15 is Vbat : CP128
3.Check U105.Nos 12, 13 and 14 pin for wave form : CP129
NO → Check that R175, R177, R131, C196, C197 cold solder,broken,short to the other
PCB pattern or not
If you find out any defect, you replace it
4.Check SPK No. SPOUT1 and SPOUT2 for wave form : CP130
NO → Replacd SPK


CP127`
CP128`
CP130`
CP129`


CP129`
CP127`
C911
C910
R175
C197
R131
C196
C177
R209
C157
C200
R177
C179
C159
U105
U109
R218
C198
R219
C199
R216
C156
CP128`
CP117`
CP130`

6.4. 6.2.7 Vibrator not working

Check to see if U101 No. C5(Q105.2) pin is 2.8V(duty:70%, 70Hz) : CP131

NO → Check to see Q105 cold solder,broken,short to the other PCB pattern or not

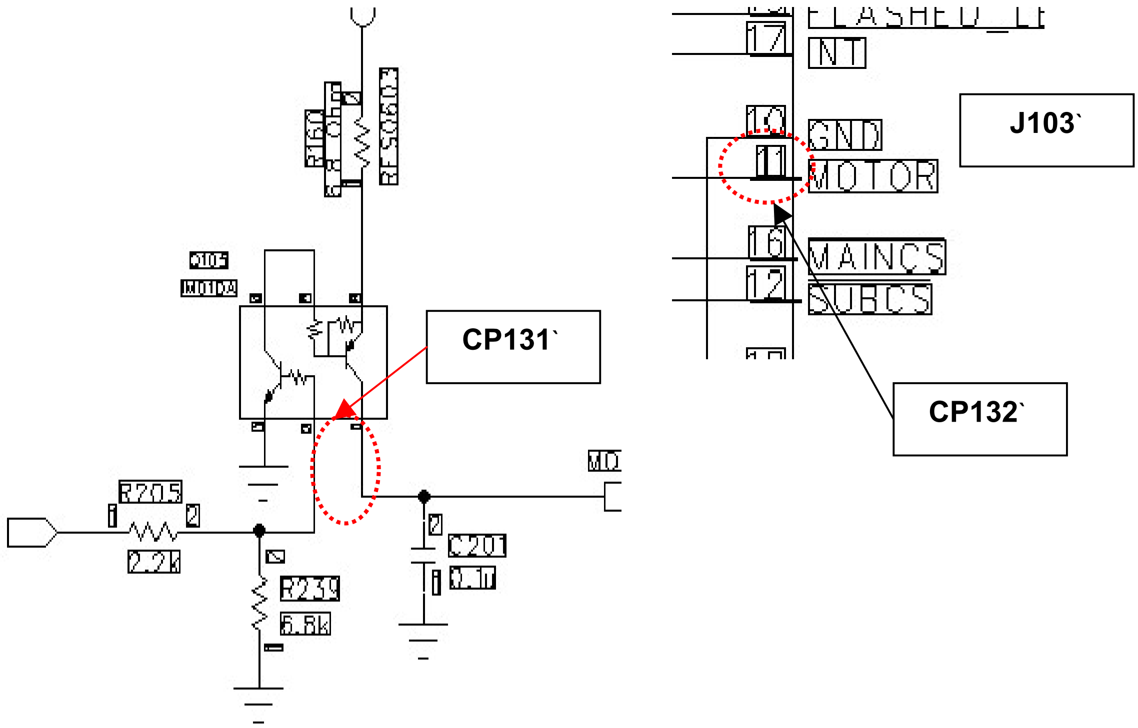
If you find out any defect, you replace it

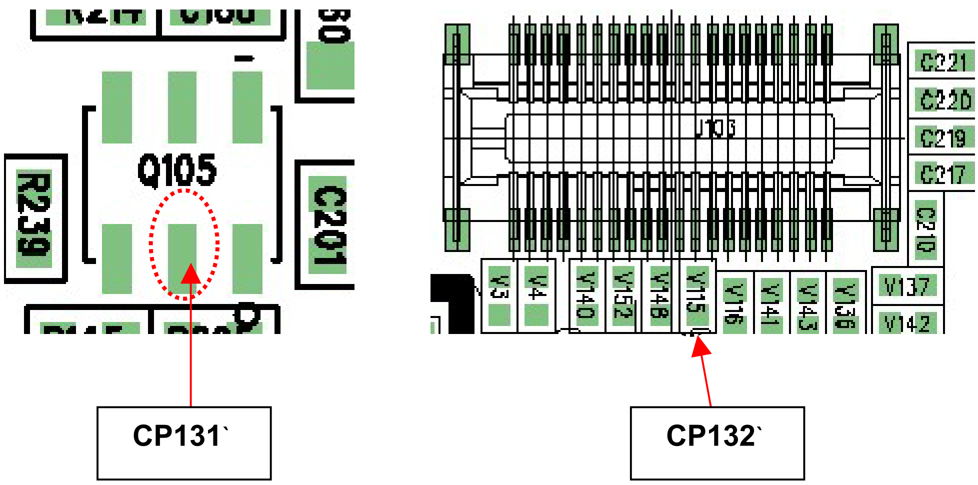
Check to see J103.11 is same with battery power : CP131,CP132

NO → Check to see R160 cold solder,broken,short to the other PCB pattern or not

If you find out any defect, you replace it

3.Check to see Vibrator If you find out any defect, you replace it





6.3 SIM card part

6.3.1 SIM error

1. Check to see if J103-JST No. 1 pin is 2.85V : CP133

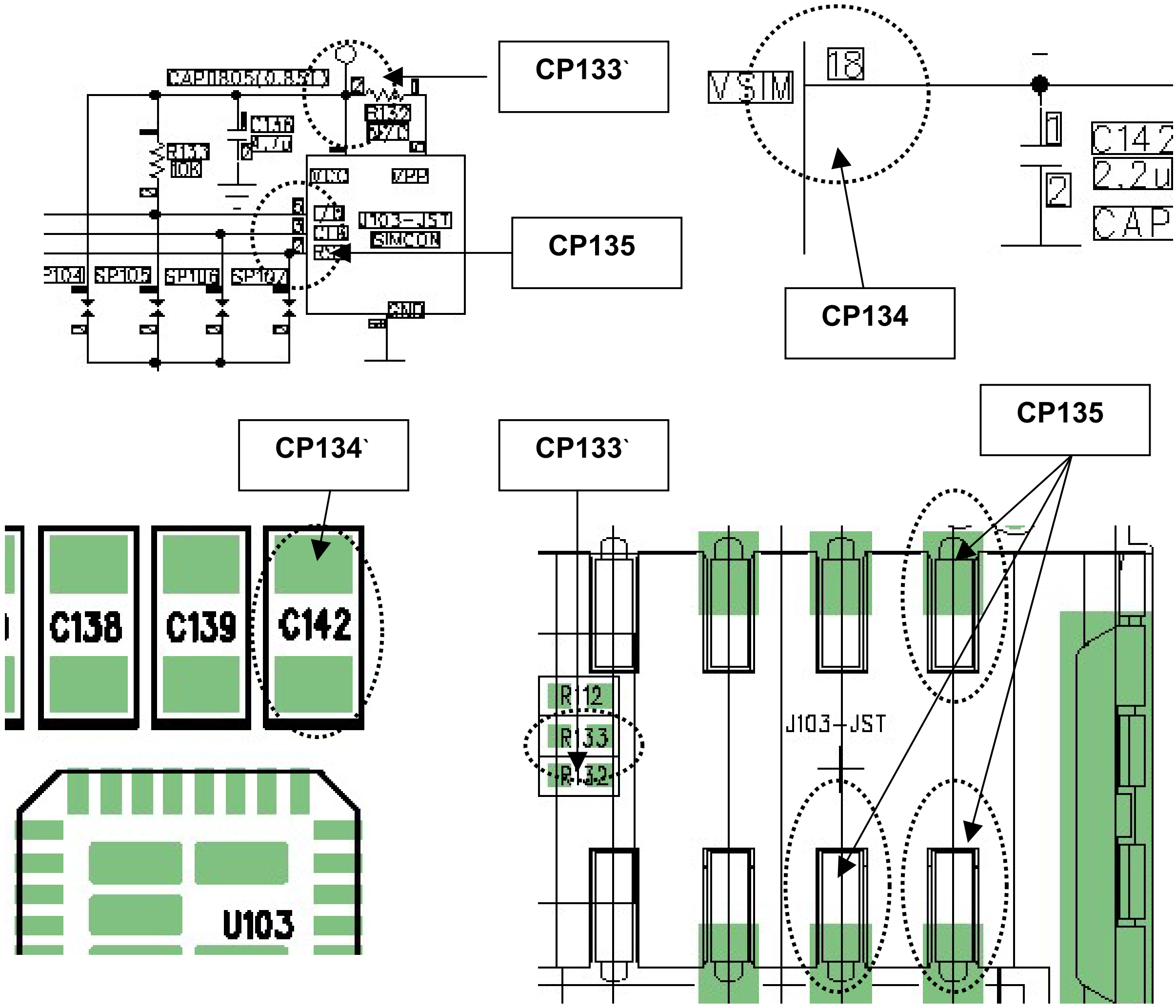
NO → Check to see U103.18 pin cold solder,broken,short to the other PCB pattern or not : CP134

If you find out any defect, you replace it

2.Check to see J103-JST.2.3.6 for wave form : CP135

NO → Check to see J103-JST,R133 and C136 cold solder,broken,short to the other PCB pattern or not

If you find out any defect, you replace it



6.4 Charger part

6.4.1 Charging error

Insert adaptor into I/O jack.

1. Check to see if U103. 7 pin is 5.2V : CP136

NO → Check to see J101.23 .24 pin and D116 cold solder,broken,short to the other PCB pattern or not : CP137

If you find out any defect, you replace it

2.Check to see U103.14 pin is low(0V) : CP138

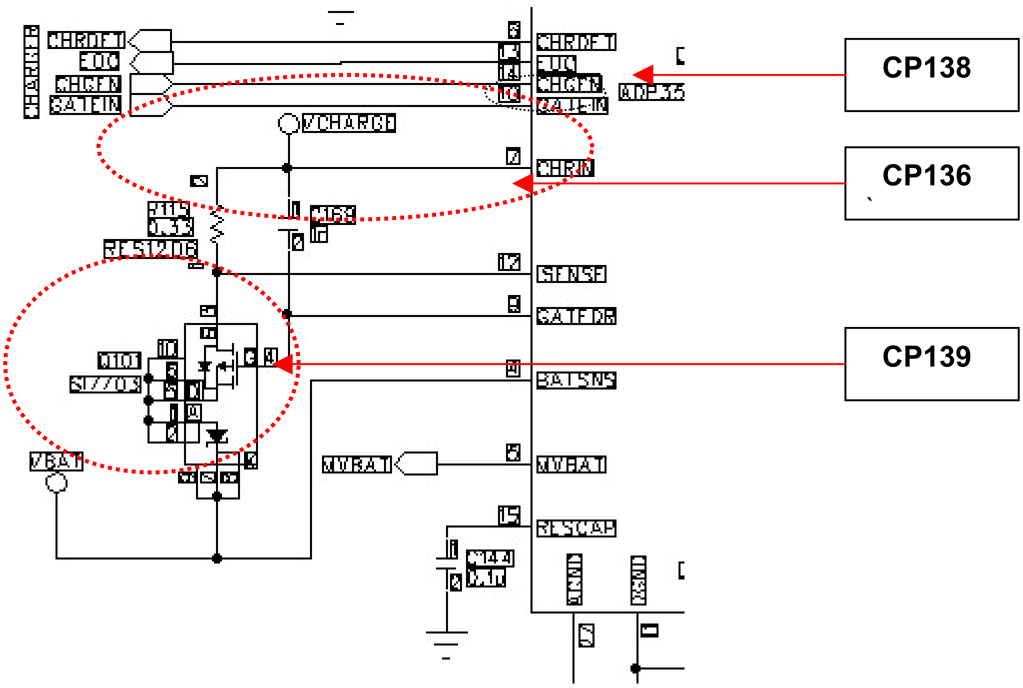
NO → Check to see U103 cold solder,broken,short to the other PCB pattern or not

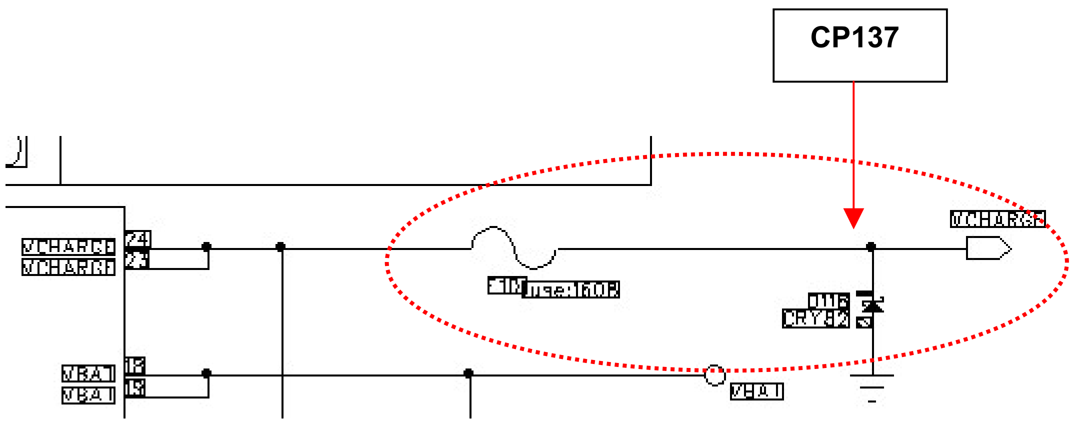
If you find out any defect, you replace it

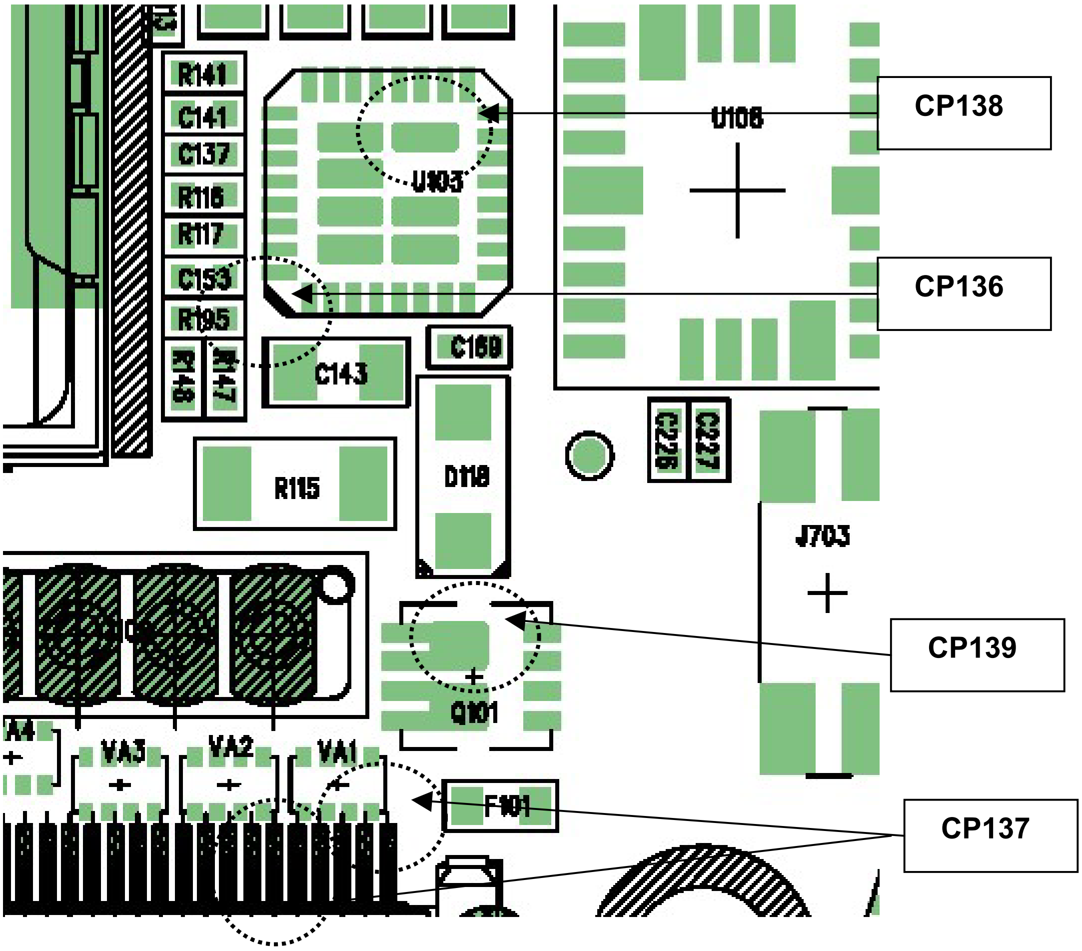
3.Check to see Q101 No.4 pin is 4.2V : CP139

NO → Check to see Q101.R115.C169 cold solder,broken,short to the other PCB pattern or not

If you find out any defect, you replace it






R141
C141
C137
R116
R117
C153
R195
R148
R147
C143
C169
U103
U106
CP138
CP136
R115
D118
C226
C227
J703
CP139
Q101
VA3
VA2
VA1
F101
CP137

6.5. Bluetooth part

6.5.1 Bluetooth error

After BT_En(U101.A9,U106.3) Pin is enable,

1. Check to see if U108. 1,14,15,19,20 pin is 2.8V : CP140

NO → Check to see U106.5 cold solder,broken,short to the other PCB pattern or not : CP141

If you find out any defect, you replace it

2.Check to see U115.5,U116.5,U117.5,U118.5 pin is 2.8V : CP142

NO → Check to see U115,U116,U117,U118 cold solder,broken,short to the other PCB pattern or not

If you find out any defect, you replace it

3.Check to see R231,R235 pin's data link connected : CP143

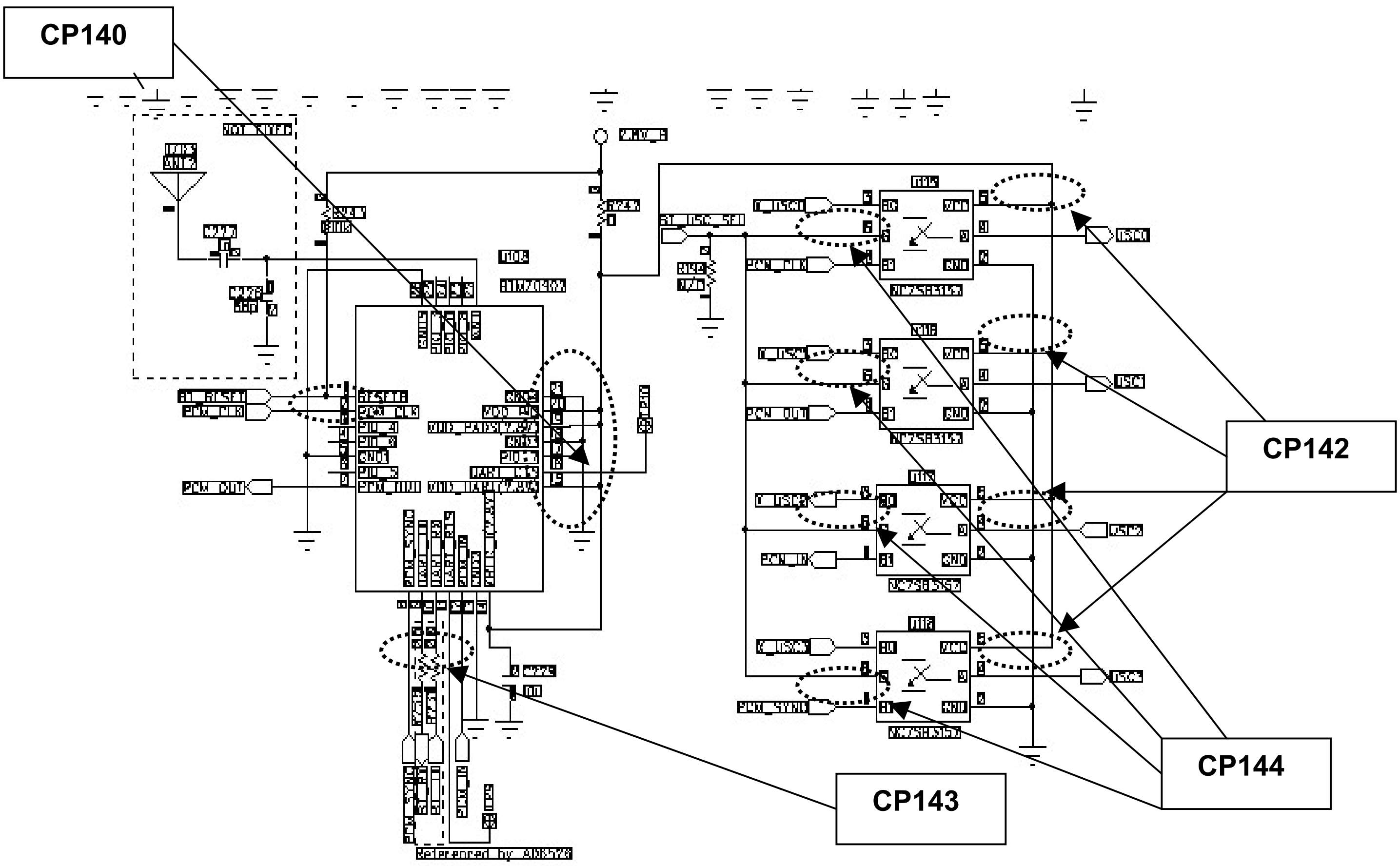
NO → Check to see R231.R235 cold solder,broken,short to the other PCB pattern or not

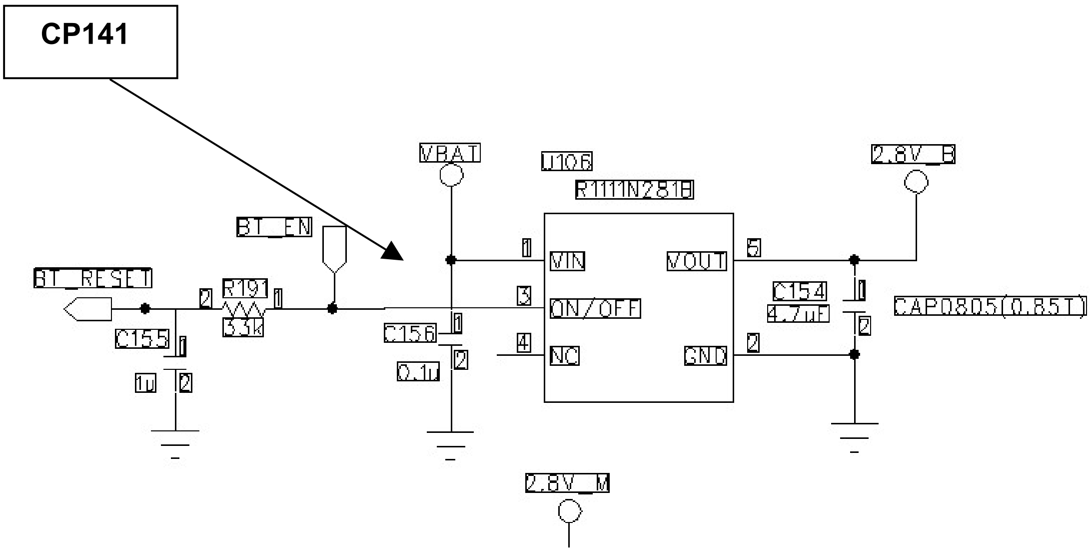
If you find out any defect, you replace it

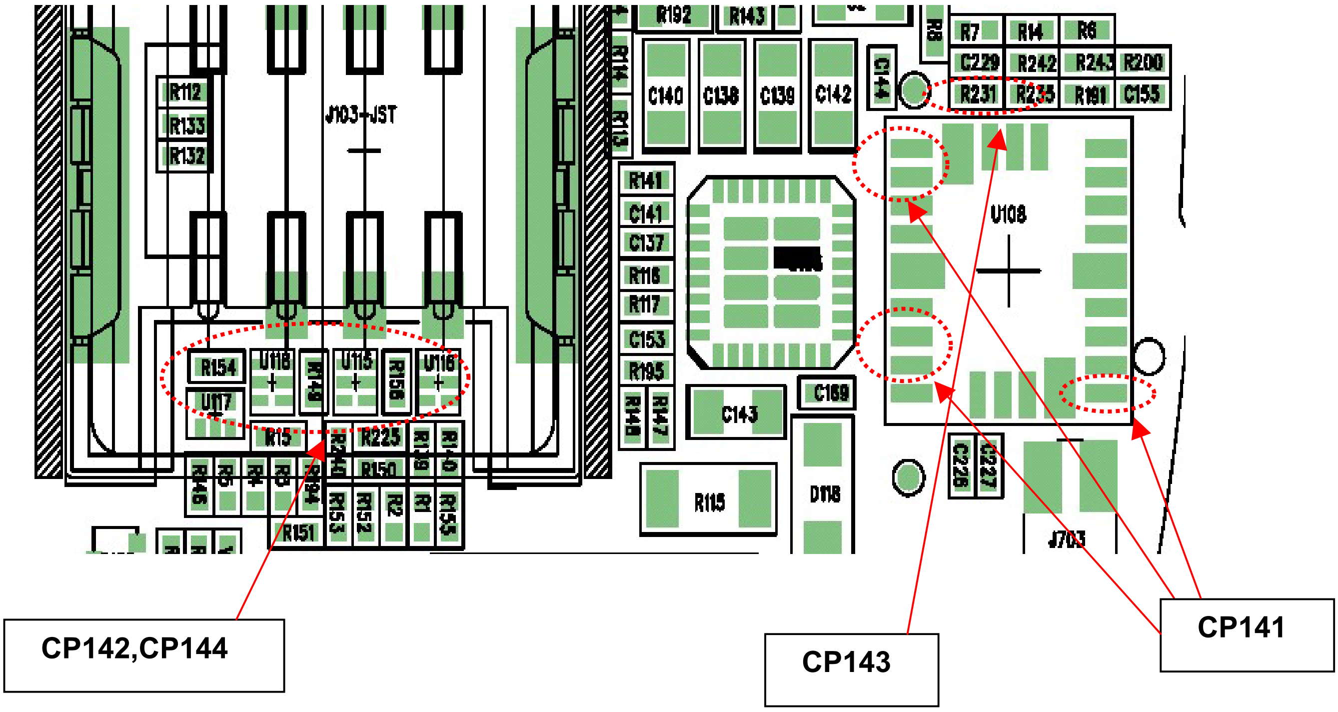
4.To see Audio Gateway is enabled,Check U115,U116,U117,U118.6 is low(0V):CP144

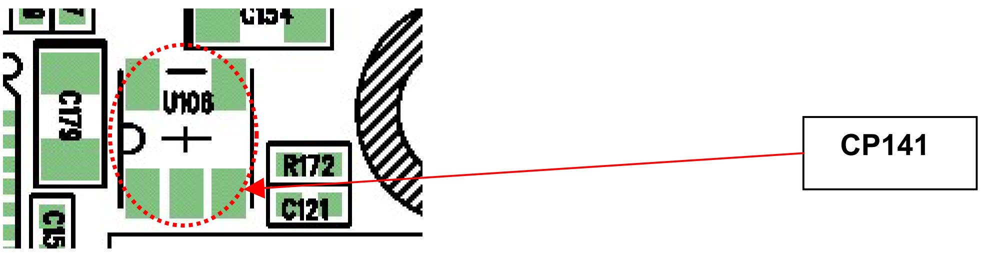
NO → Check to see U115,U116,U117,U118 cold solder,broken,short to the other PCB pattern or not

If you find out any defect, you replace it




CP141
VBAT
U106
R1111N281B
2.8V_B
BT_EN
BT_RESET
R191
33k
C155
1u
C156
0.1u
VIN
ON/OFF
NC
VOUT
GND
C154
4.7uF
CAP0805(0.85T)
2.8V_M


J103-JST
U108
CP142,CP144
CP143
CP141


U106
R172
C121
C179
CP141

6.6. RF Part

6.6.1 Test conditions

1. Test condition 1 : VBAT = 3.8V during all tests

2. Test condition 2 : Traffic channel :EGSM Band
   Tx mode
   Ch62
   Power Level : 13

3. Test condition 3 : Traffic channel :DCS Band
   Tx mode
   Ch698
   Power Level : 10

4. Test condition 4 : Traffic channel : PCS Band
   Tx mode
   Ch662
   Power Level : 10

5. Test condition 5 : Traffic channel :GSM Band
   Rx mode
   Ch62
   Input power : -70dBm

6. Test condition 6 : Traffic channel : DCS Band
   Rx mode
   Ch698
   Input power : -70dBm

7. Test condition 7 : Traffic channel : PCS Band
   Rx mode
   Ch662
   Input power : -70dBm

8. RF power values are measured using 50Ω coaxial cable.

6.6.2 Power Supply Check Point

Step	Test point	Typical Value	Condition	Checking Point
2-1	U907 Pin#1	3.8V	2, 3, 4, 5, 6, 7	Check route connection : VBAT
2-2	U907 Pin#5	2.8V	2, 3, 4, 5, 6, 7	Check route connection : VCC_RFCHIP
2-3	U701 Pin#4	3.8V	2, 3, 4, 5, 6, 7	Check route connection : VBAT
2-4	U701 Pin#5	2.8V	2, 3, 4, 5, 6, 7	Check route connection : VCC_RFCHIP

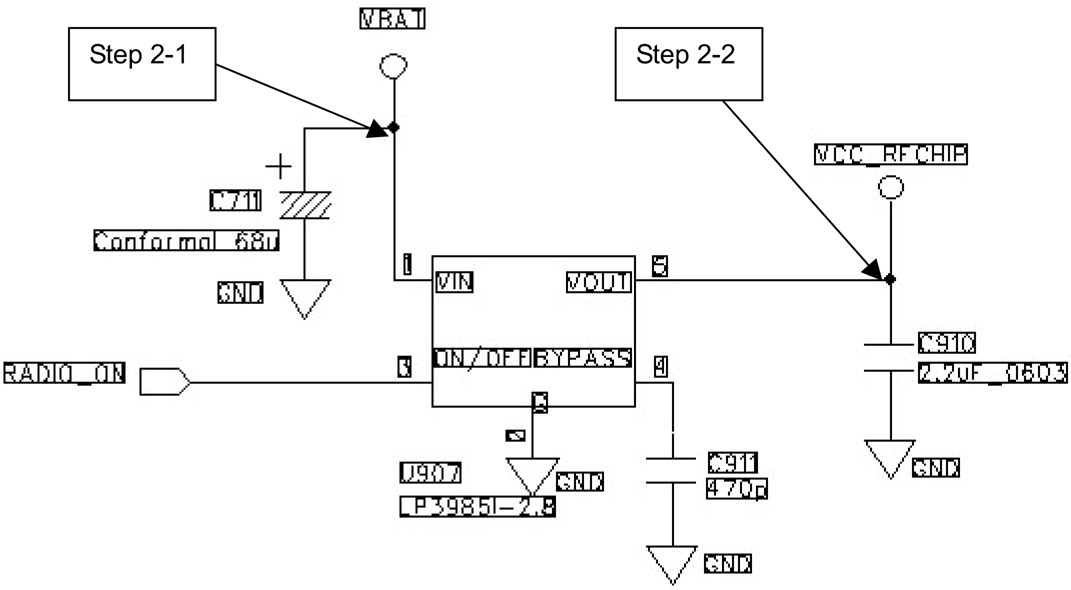


Fig.6-1 U907 Regulator Power Supply Schematic

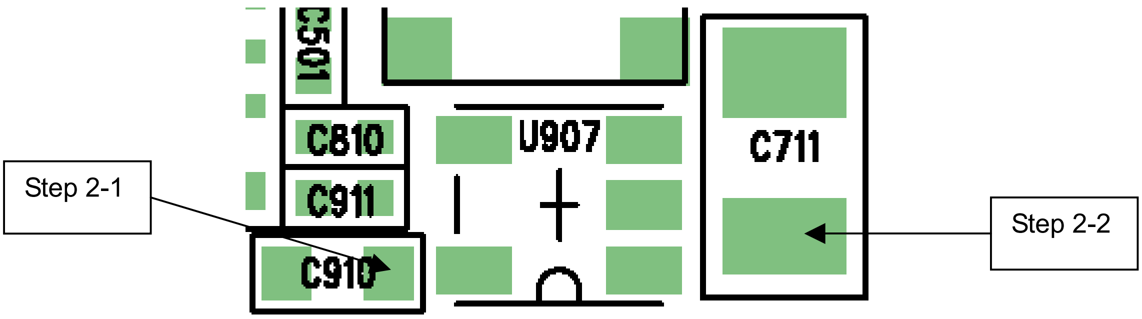


Fig.6-2 U907 Regulator Power Supply PCB Layout

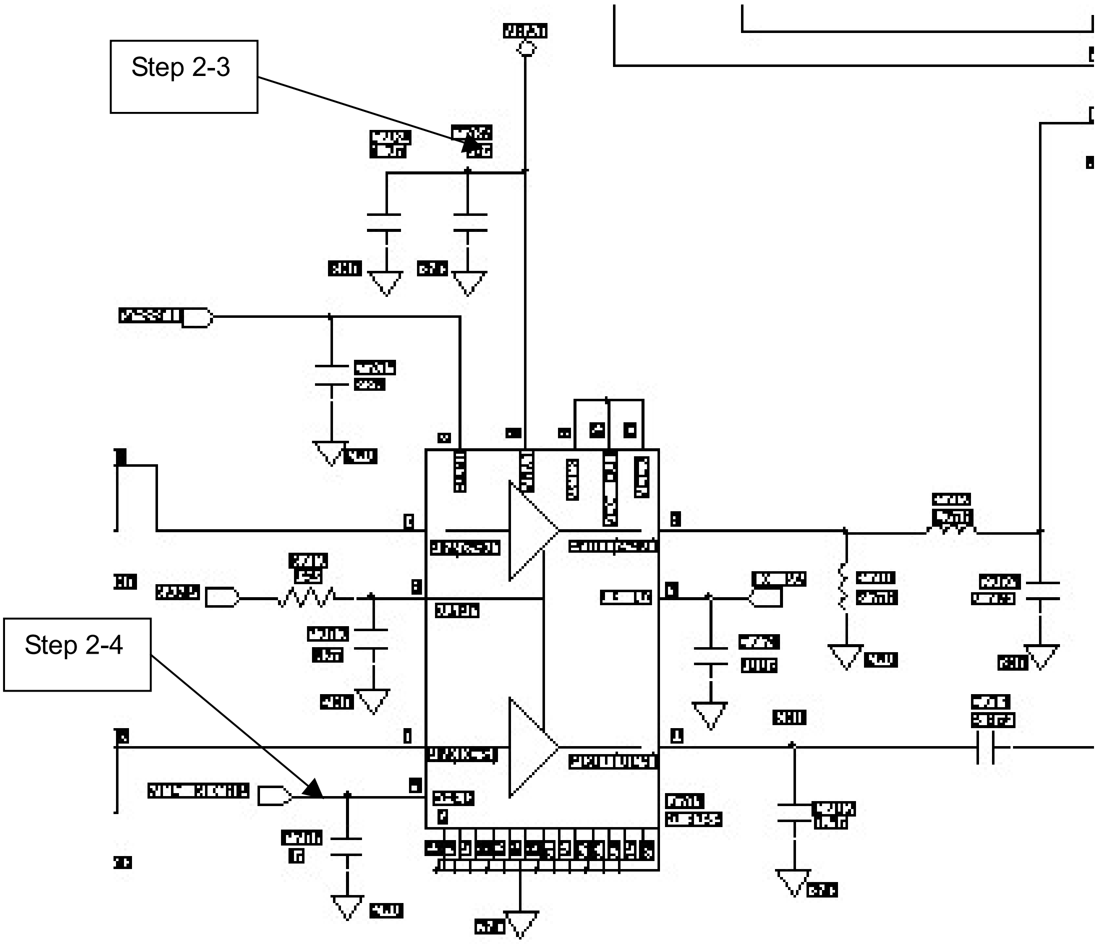


Fig.6-3 Z710 PAM's Power Check Point

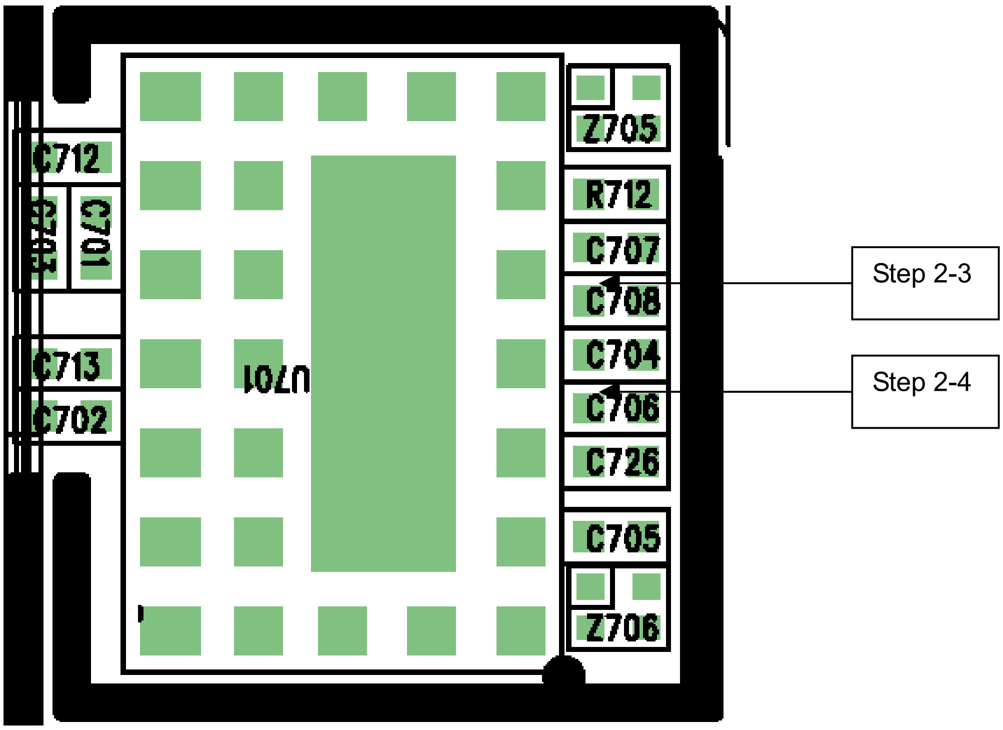


Fig.6-4 Z710 PAM's PCB Layout

6.6.3 Power Amplifier Module

- First check the Power Supply Check point following 6.3.2. Then you can trace the guideline of PAM as follows .

Step	Test point	Typical Value	Condition	Checking Point
3-1	Z710 Pin#3	Logic High	2, 3, 4	Check route connection : TXEN
3-2	Z710 Pin#2	Logic High	3, 4	Check this pin 2, When Logic High, then DCS or PCS Mode. While Logic Low , GSM mode is operating.
		Logic Low	2	

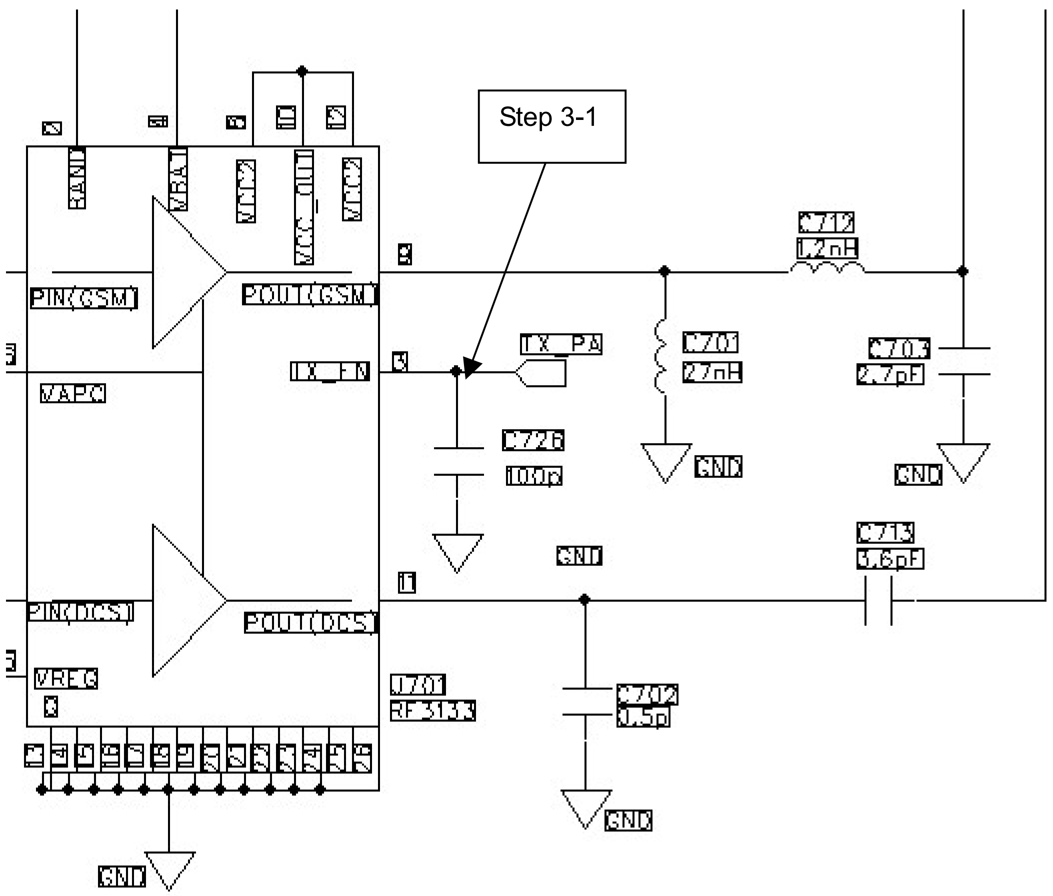


Fig.6-5. PAM TXEN Test Point Circuit

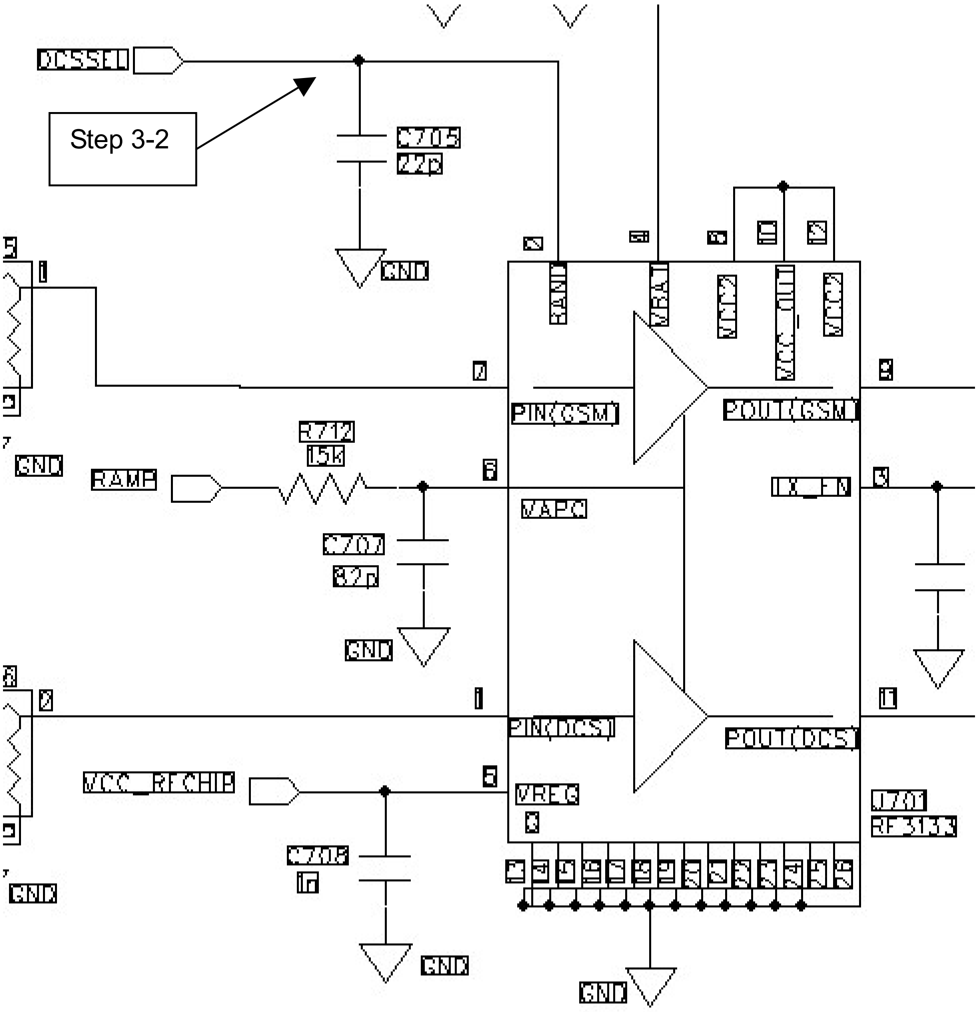


Fig.6-6. PAM DCSSEL Test Point Circuit

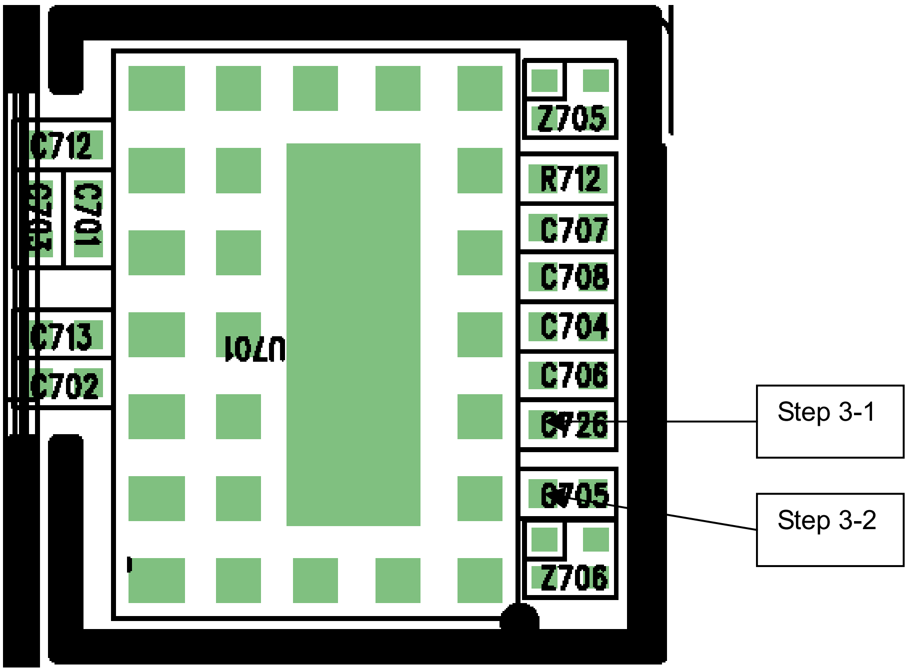


Fig.6-7. PAM TXEN and DCSSEL Test Point on the PCB Layout

6.6.4 VCTCXO

Step	Test point	Typical Value	Condition	Reaction to Abnormality
4-1	V801 Pin#1	0.5V ~ 2.5V	2, 3, 4, 5, 6, 7	Check route connection : AFC
4-2	V801 Pin#4	2.8V	2, 3, 4, 5, 6, 7	Check route connection : VTCXO

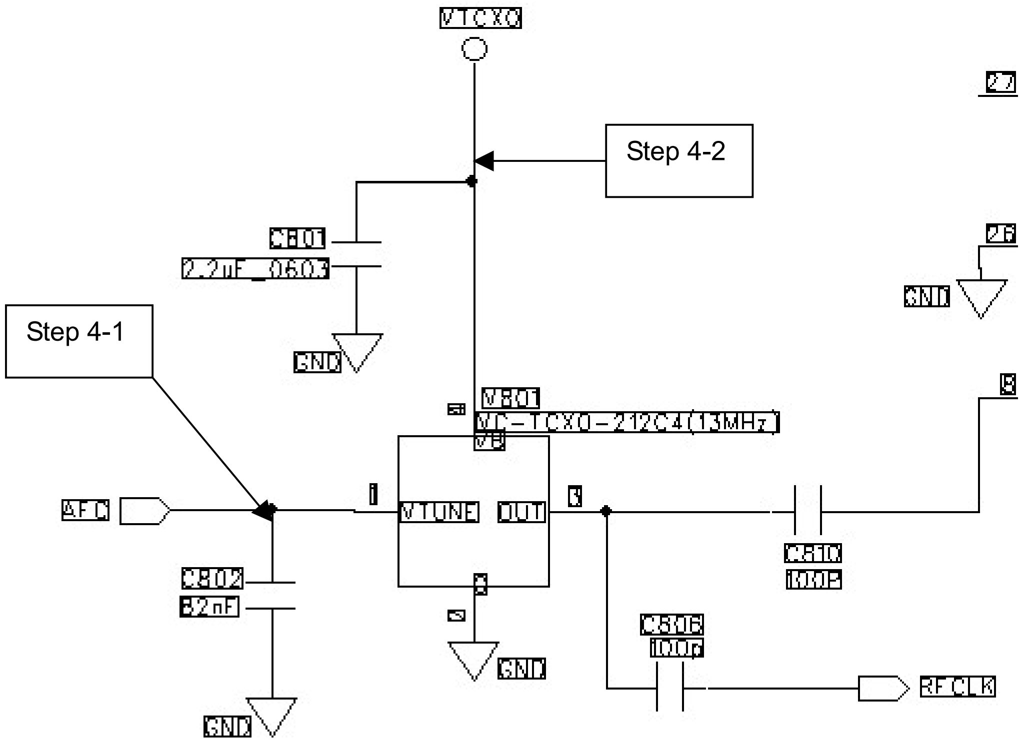


Fig.6-8. VCTCXO Check Point Circuit

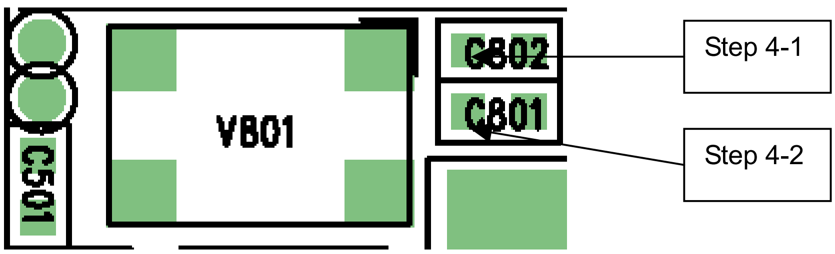


Fig.6-9. VCTCXO Check Point on the PCB Layout

6.6.5 Antenna Switch Module

Step	Test point	Typical Value	Condition	Check point
5-1	Z701 Pin#10	2.8V	2	When Pin#10 is Logic High and Pin#4 and Pin#2 is Logic Low the mode is EGSM Tx.
5-2	Z701 Pin#4	2.8V	3	While Pin#4 is Logic High and Pin#10 and Pin#2 is Logic Low the operating mode is DCS Tx..
5-3	Z701 Pin#2	2.8V	7	While Pin#2 is Logic High and Pin#10 and Pin#4 is Logic Low the operating mode is DCS Rx..
5-4	Z701 Pin#4 & Pin#2	2.8V	4	While Pin#4 and Pin#2 is Logic High and Pin#10 is Logic Low the operating mode is DCS Tx..
5-5	Z701 Pin#10 & Pin#4 & Pin#2	0V	5, 6	While Pin#10, Pin#4 and Pin#2 is Logic Low the operating mode is EGSM Rx or DCS Rx.

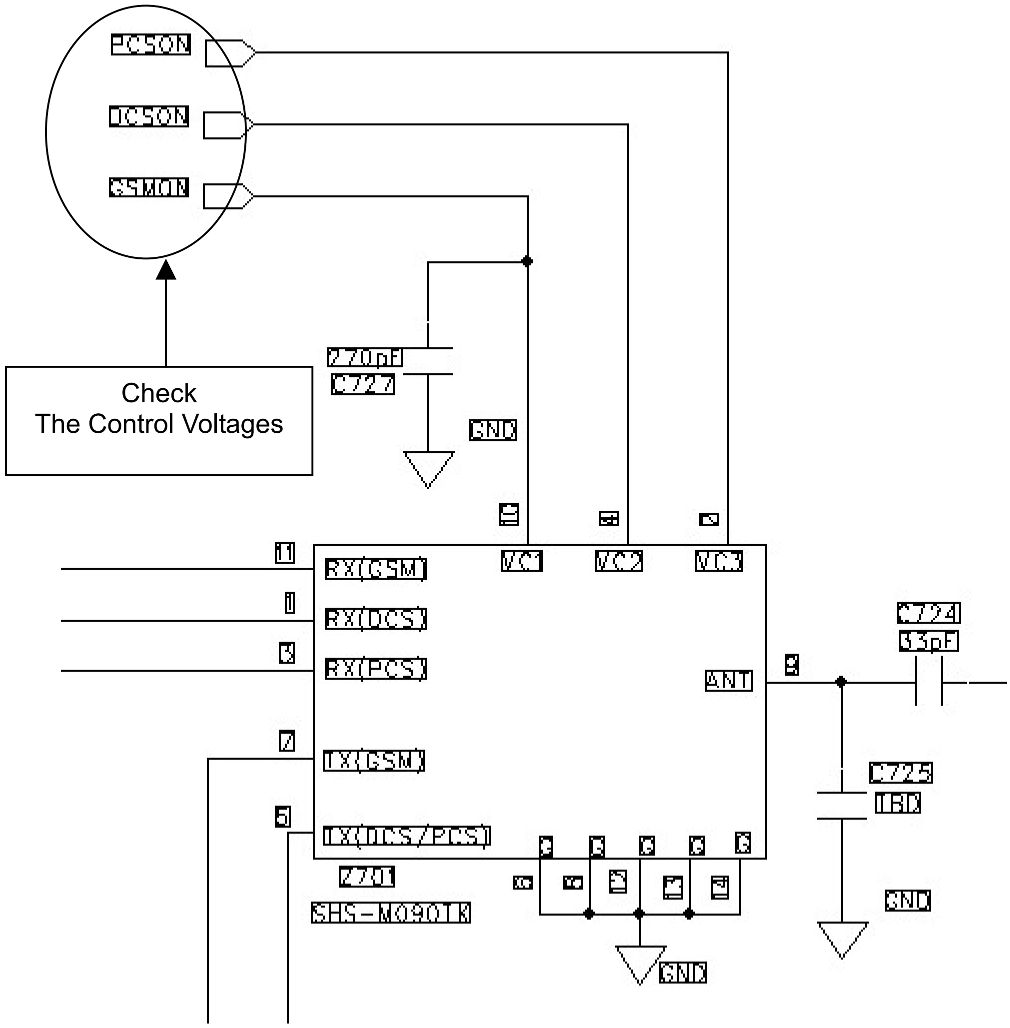


Fig. 6-10 Antenna Switch Module Circuit

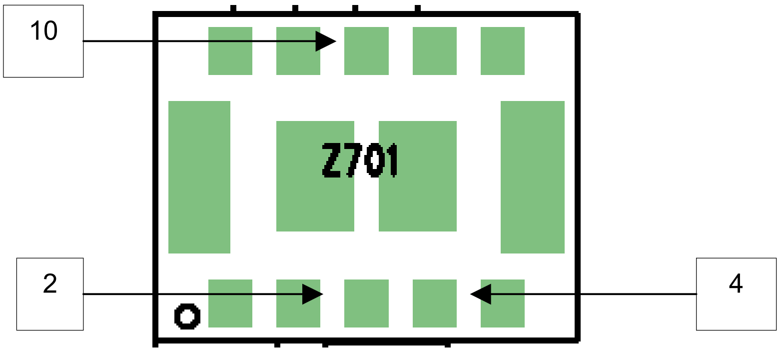


Fig. 6-11 Antenna Switch Module PCB Layout