G310 Service Manual

(GSM Cellular Phone)

Pantech Co., Ltd., Korea

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1st Edition

For Use by Authorized Service/Maintenance Personal Only

Documents to Receive This Addendum:

G310 Maintenance/Repair/Operating Manual

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SECTION 1. Introduction

1.1 An Introduction of GSM Digital Cellular Mobile Communication System

GSM (Global System for Mobile communication) concluded that digital technology working in the Time Division Multiple Access (TDMA) mode would provide the optimum solution for the future system. Specifically , a TDMA system has the following advantage

- ► Offers a possibility of channel splitting and advanced speech coding ,resulting in improved spectrum efficiency.
- ► Offers much greater variety of service than the analog
- ► Allows considerable improvements to be made with regards to the protection of information.

The GSM system is basically designed as a combination of three major subsystem;
The network subsystem, the radio subsystem, and the operation support system.
The functional architecture of a GSM system can be divided into the Mobile Station (MS), the Base Station (BS), and the Network Subsystem (NS). The MS is carried by the subscriber, the BS subsystem controls the radio link with the MS and the NS performs the switching of calls between the mobile and other fixed or mobile network users as well as mobility management. The MS and the BS subsystem communicate across the Um interface also known as radio link
The specifications relating to MS are as follows:

- TS 100 607-1 : Digital cellular telecommunication system(Phase2+)Mobile Station (MS) con Formance specification Part1:Conformance specification

1.2 Frequency Allocation and Its Use

- Transmit frequency band : 880 MHz ~ 915 MHz(For EGSM) , 1850 MHz ~ 1910 MHz(For PCS)
- Receive frequency band: 925 MHz ~ 960 MHz(For EGSM) , 1930 MHz ~ 1990 MHz(For PCS)
- Channel spacing : 200 KHz
- ARFCN(Absolute Radio Frequency Channel Number) : 1~124 and 975~1023 (For EGSM), 512~810 (For PCS)
- Transmit · receive frequency spacing: 45 MHz(For EGSM), 80MHz(For PCS)
- Frequency band and Channel Arrangement

For standard GSM Fl(n)=890+0.2*n 1 ≤n≤ 124 Fu(n)=Fl(n)+45
890 MHz ~915 MHz : Mobile Transmit,Base receive
935 MHz ~960 MHz : Base Transmit, Mobile receive
For Extended GSM Fl(n)=890+0.2*n 1 ≤n≤ 124 Fu(n)=Fl(n)+45 Fl(n)=890+0.2*(n-1024) 975 ≤n≤ 1023
880 MHz ~915 MHz : Mobile Transmit,Base receive
925 MHz ~960 MHz : Base Transmit, Mobile receive
For PCS Band Fl(n)=1850.2+0.2*(n-512) 512 ≤n≤810 Fu(n)=Fl(n)+80
1850 MHz ~1910 MHz : Mobile Transmit,Base receive
1930 MHz ~1990 MHz : Base Transmit, Mobile receive
** Fl(n)= frequency value of the carrier , Fu(n)= corresponding frequency value in upper band

1.3 Item Name and Usage

G310, GSM digital cell phone, is supercompact, superlight mobile communication terminal for personal use. It has a 900MHz and 1900MHz frequency band and adopts GSM and PCS mode having excellent spectrum efficiency, economy, and portability.

This product is GSM Cellular type portable phone, adopting 1-cell Li-ion battery and power saving circuit to maximize its operation time. Also, it is equipped with a fixed antenna (snap-in type) and its color LCD with font built in enables both Chinese and English text service. And power control(basic feature of GSM), security feature, voice symbol feature, and variable data rate feature are used appropriately to ensure its best performance. This product consists of a handset, battery pack, and Travel charger.

1.4 Characteristics

1) All the active devices of G310 are made of semiconductors to ensure excellent performance and semi-permanent use.
2) Surface mounting device (SMD) is used to ensure high reliability, compactness and lightness.
3) G310 adopts the Silabs's AERO RF transceiver, which is CMOS RF front-end for multi-band GSM digital cellular handsets. The Aero's highly-integrated architecture eliminates the IF SAW filter, low noise amplifiers (LNAs) for three bands, transmit and RF voltage-controlled oscillator (VCO) modules, and more than 60 other discrete components found in conventional GSM handsets to deliver smaller, more cost effective GSM solutions that are easier to design and manufacture.
4) G310 is designed to perform excellently even in the worst environment

Section 2. Electrical Specifications

2.1 General E-GSM / PCS Band

Mobile Transmit Frequency	880 MHz ~ 915 MHz/1850 MHz ~1910 MHz
Mobile Receive Frequency	925 MHz ~ 960 MHz/1930 MHz ~1990 MHz
The Number of Time Slot	8
The Number of Channels	174/299
Channel Spacing	200 kHz
Power Supply	Rechargeable Li-Ion Battery 3.7V/680mAh
Operating Temperature	-10℃ ～ +55℃
Dimension	76(H) ×40(W) ×23.5(D) mm (SLIM)
Weight	76 g

2.2 Transmitter E-GSM / PCS Band

Maximum Output Power	33±2 / 30±2 dBm
Frequency Error	±90Hz/±180Hz
Phase Error	RMS < 5°, PEAK < 20°
Minimum Output Power	5±5 / 0±5 dBm
Power Control	5~19(2 dB Step)/0~15(2 dB Step)
Output RF Spectrum	TS 100 910V6.2.0
Switching Transient	TS 100 910V6.2.0
Intermodulation attenuation	
Conducted Spurious Emissions	Idle Mode -57dBm 9KHz~880M/915MHz~1GHz -59dBm 880MHz~915MHz -53dBm 1.8~1.910GHz -47dBm 1~1.715GHz/1.910GHz~13.37GHz
	Allocated Channel -36dBm 9KHz~ 1GHz -30dBm 1GHz~ 13.37GHz

2.3 Receiver

Reference Sensitivity	For GSM900 class4, small MS :-102dBm	
	For PCS1900 class1 MS : -102dBm	
For Adjacent interference For Adjacent(200KHz) interference For Adjacent(400KHz) interference For Adjacent(600KHz) interference	C/Ic	9 dB
	C/Ia1	-9 dB
	C/Ia2	-41 dB
	C/Ia3	-49 dB

Section 3 Operation

3.1 Name of each part

3.2 Display(Dual LCD)

Parameter	Projected Actual (MAIN LCD)
Display	Color TFT LCD with white LED back lighting 262,144 colors European Character : (font size : 16×16) 7 lines x 8 characters Chinese Character : (font size : 16×16) 7 lines × 8 characters
Driver	μPD161691 (NEC)
Module Dimen.	31.6(W) x 48.0(H) x 4.86(D)
View size	26.85(W) x 26.31(H)
Active Area	23.04(W) x 23.04(H)
Dot size	0.60(W) x 1.80(H)
Dot pitch	1.80(W) x 1.80(H)

Parameter	Projected Actual (SUB LCD)
Display	Full Graphic LCD with white LED back lighting Pixels : 96 x 64 European Character : (font size : 16×16) 4 lines x 8 characters Chinese Character : (font size : 16×16) 4 lines × 6 characters
Driver	S1D10605D03E000 (EPSON)
Module Dimen.	31.6(W) x 48.0(H) x 4.86(D)
View size	18.1(W) x 14.3(H)
Active Area	18.1(W) x 12.3(H)
Dot size	0.152(W) x 0.177(H)
Dot pitch	0.167(W) x 0.192(H)

3.3 Keypad

	Market Goal	Projected Actual	Comments
English Keypad	0-9, *,# Send (Color) End/Pwr (Color) Up (Melody), Down (SMS), Left (WAP), Right (Phonebook) MENU, OK, CLR * Key: Vib. Mode # Key: Auto Lock 0/+Key: International 2 Volume Keys	0-9, *,# Send (Color) End/Pwr (Color) Up (Melody), Down (SMS), Left (WAP), Right (Phonebook) MENU, OK, CLR * Key: Vib. Mode # Key: Auto Lock 0/+Key: International 2 Volume Keys	Meets Goal. (Industrial design sample required) Meets Goal Keys for VR and Lock International Volume up/down

Section 4. Theory of Operation

4.1 Logic Section

4.1.1 DC Distribution and Regulation Part

Applying battery voltage and pressing “END” key on the key pad short-circuits “Ground” and “_ PowerON”. ADP3522(U103) control that power manage regarding power on/off in handset Pressing POWERKEY on the key pad is active on the handset.
This will turn on all the LDOs, when POWERKEY is held low. The power of RF Tx power amplifier is supplied directly by the battery.

4.1.2 Logic part

4.1.2.1 Summary

The logic part consists of AD6526 ARM7 microprocessor-combined GSM-ASIC, COMBO(flash ROM & SRAM), AD6521 VBC Chip. AD6526 is GSM-ASIC chipset implemented for GSM terminal’s system control and baseband digital signal processing.

Major parts used in the logic part are as follows:

1) AD6526 : U101, [ARM7 Processor Core + GSM Signal Processing] ASIC
2) AD6521 : U102, Voiceband Baseband Codec
3) COMBO MEMORY(Flash ROM : U104, 128Mbit Flash Memory + 32Mbit SRAM)

4.1.2.2 Baseband Digital Signal Processing

AD6526 is a GSM core device containing ARM7 CPU core. AD6526 is 160 pin LFBGA (mini-BGA) package, consisting of terminal chips. The function and characteristics of clock are as follows:

1) Complete single chip GSM Processor
2) Channel codec sub-system
   - Channel coder and decoder
   - Interleaver and Deinterleaver
   - Encryption and Decryption
3) Control Processor Subsystem including
   - Parallel and serial Display interface
   - Keypad Interface
   - SIM Interface
   - Control of RADIO subsystem
   - Real Time Clock with Alarm

☞ **Configuration by Function of AD6526**

1 Microprocessor Core

AD6526 has a built-in ARM7 microprocessor core, including microprocessor interrupt controller, timer/counter, and DMA controller. And besides, 32bit data path is included, and up to 8Mbyte addressing is enabled and can be extended up to 16Mbyte. Although external clock should be provided to operate the microprocessor, this core uses 13MHz VCTCXO to provide clock.

2 Input Clock

1) Main Clock(13 MHz):
   This is the clock needed for the microprocessor built in AD6526 to operate.
2) VC-TCXO(13 MHz) , 32.768KHz Clock:
   This is the system reference clock to control SLEEP mode.
   This is the clock derived from 13MHz VC-TCXO clock, provided by RF part. It is the timing reference clock for GSM signal processing.

3 DSP Subsystem

This is a GSM signal processing part in GSM mode, consisting of speech transcoding and Channel equalization as follows:

1) Speech transcoding

In full rate, the DSP receives the speech data stream from VBC and encodes data from 104kbps to 13kbps. Using algorithm is Regular Pulse Excitation with Long Term Prediction (RPE-LTP).

2) Equalization

The Equalizer recovers and demodulates the received signal

The Equalizer establishes local timing and frequency references for mobile terminal as well as RSSI calculation.

The equlization algorithm is a version of Maximum Likelihood Sequency Estimation(MLSI) using Viterbi Algorithm.

☞ **GSM Core and RF Interface**

1) Transmitter:
   AD6521 VBC receive data at 270kbps and use an on chip lock-up table to perform GMSK modulation. A pair of 10bit matched differential DACs convert the modulated data and pass I and Q analog data to the transmit section of the radio system.
2) Receiver:
   The receiver I and Q signals are sampled by a pair of ADCs at 270kbps.
   The I and Q samples are transferred to the EGSMP through a dedicated receive path serial port.

4 RF Interface

This interfaces the RF part to control power amplifier, Tx LO buffer amplifier, VC-TCXO, and AGC-end on transmit/receive paths in the RF part.

1) Transmitter Interface:

This transmits TX_AGC signal to Tx AGC amplifier to adjust transmit power level and sends Ramp_DAC signal to the RF part to control power amplifier.

2) Receiver Interface:

This transmits RX_AGC signal to Rx AGC amp. to adjust receive path gain.

5 General Purpose ADC Support

The AD6521 includes a general purpose 10bit auxiliary ADC with four multiplexed input channel These are used for measurment of battery voltage ID , temperature and accessory ID.

6 USC(Universal System Connector) Interface

A Typical GSM handset requires serial connections to provide data during normal phone operation manufacturing,testing and debugging.

7 General Purpose Interface

The AD6526 provides 32 interface pin for control of peripheral devices.
All GPIO pins start up as inputs. Additional purpose inputs and outputs are available under SW control.

8 Speech Transcoding

In full rate mode, the DSP receive the speech data stream from the VBC and encodes data from 104kbps to 13kbps.Using algorithm is Regular Pulse Exitation with Long Term Prediction as specified GSM Recommandation

9 Power Down Control Section

1) Idle Mode Control:

If IDLE/ signal turns ‘Low’, transmitter section becomes disabled.

2) Sleep Mode Control:

If IDLE/ and SLEEP/ signals turn ‘Low’, all the sections except for VC-TCXO circuit become disabled.

3) Receiver & Transmitter Mode Control:

If IDLE/ and SLEEP/ signals turn ‘High’, all the sections become enabled to perform transmit/receive operation.

4.1.3 Memory Part

Memory consists of COMBO (flash ROM & SRAM).

1 Flash ROM

Flash ROM has a capacity of 128Mbit(16MByte). The main programs of the terminal(call processing, user interface, and diagnostic task) and supplemental programs (NAM program and test program) are stored in the flash ROM. Even if the program version may be changed in the future, customers can download the program.

2 Static RAM

SRAM has a capacity of 32Mbit(4MByte) and stores system parameters, data buffer, and stack of each task in it.

3 Key Tone Generation

All alert signals are generated by the DSP and output to the EVBC.

These alert can be used for the earpiece.

4.1.4 Notification Part

The notification of incoming call is given by melody, vibrator, and 7color-LED.

1) Melody:

   This is a device sounding alert/melody tones.

   The melody datas are stored in flash memory (U104) And generated by Melody IC(U105).

2) Vibrator:

   This is a device enabling vibration. The vibrator data is stored in flash memory(U104)

   And generated by C5(GPO_23)pin.

3) 7color-LED:

   This is a device to indicate a notification mode using the lamp.

   U101 Nos. A10, A9 and C9 signal drives the lamp to flash.

4.1.5 Key Pad Part

To enable key operation to input information, the key matrix is configured using strobe signal of KEYPADROW(0-4) and 5 input ports of KEYPADCOL(0-4). Also, to use the key even at light, the backlight circuit is provided for LED 6s.

4.1.6 LCD Module(Display Part)

LCD module consists of LCD, controller, LED-Backlight, and LCD reflector.using dual LCD

Main LCD: 1S/W Icon x 1 lines[(128x3)x128] can be displayed on the LCD panel. 6 icons could be provided by S/W. Controller with English font built in has been used.

Sub LCD: 1S/W Icon x 1 lines(96x64) can be displayed on the LCD panel. 6 icons are provided. Controller with English font built in has been used.

LED-backlight Using illuminates the LCD panel, and LCD reflector enhances LCD display effect.

4.2 Radio Transceiver Section

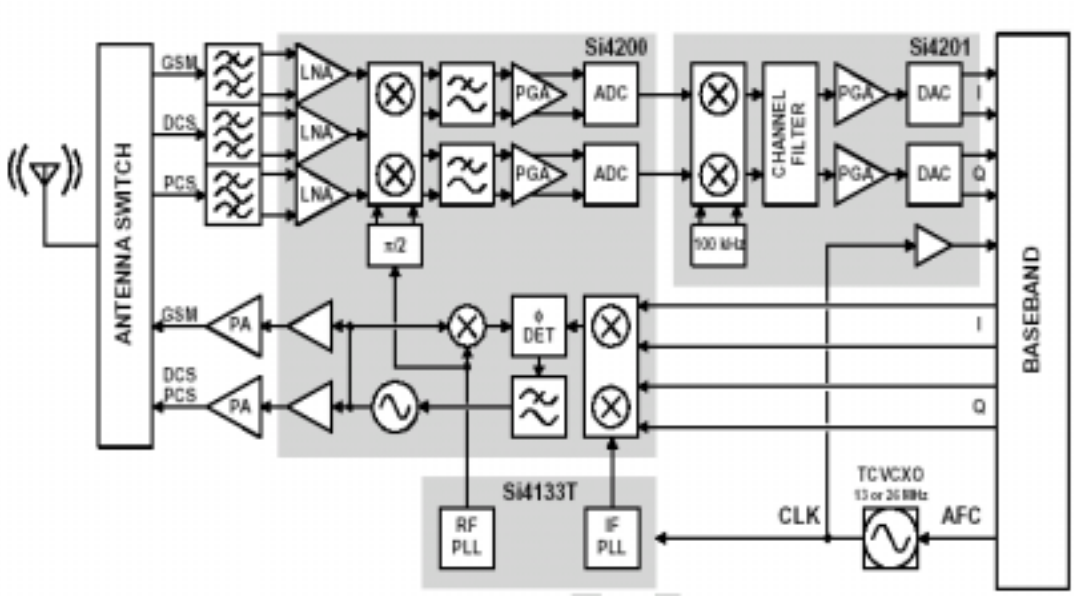


Fig.4-1. RF Transceiver block diagram

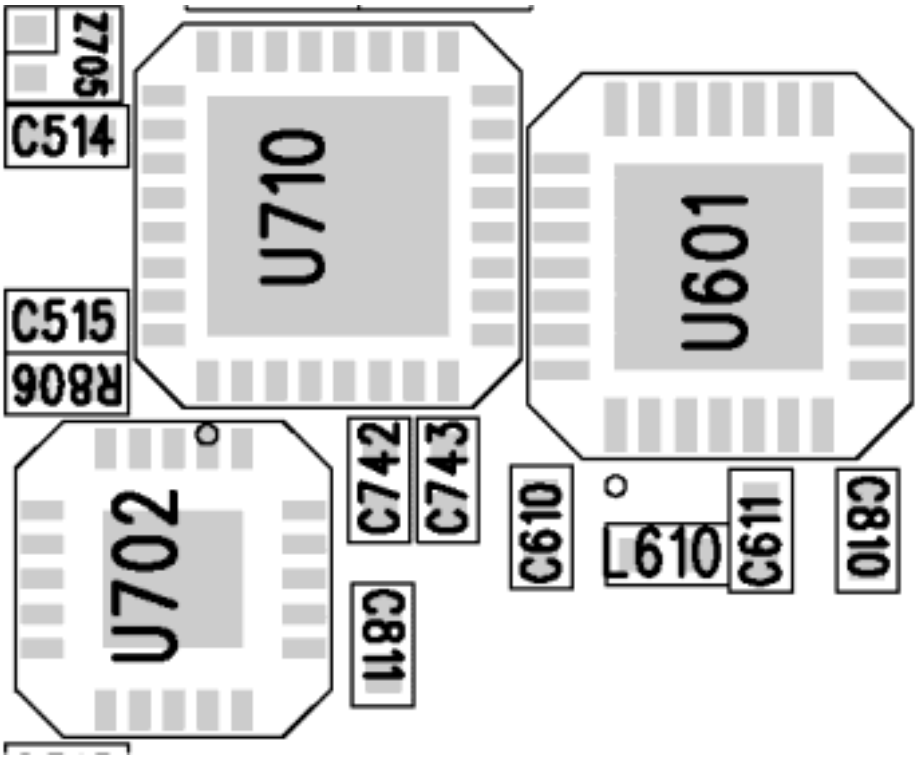


Fig.4-2. Top view of RF Transceiver PCB Layout

The G310's RF Transceiver, which is AERO, consists of the Si4200 GSM transceiver (U710), Si4201 universal baseband interface (U702), and Si4133T dual RF synthesizer (U601). The highly integrated solution eliminates the IF SAW filter, external low noise amplifiers (LNAs) for three bands,

transmit and RF voltage controlled oscillator (VCO) modules, and more than 60 other discrete components found in conventional designs.

The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduced complexity. The universal baseband interface (Z710) is compatible with any supplier's baseband subsystem.

The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifer (Z710) and uses an offset phase locked loop (PLL) with a fully integrated transmit VCO.

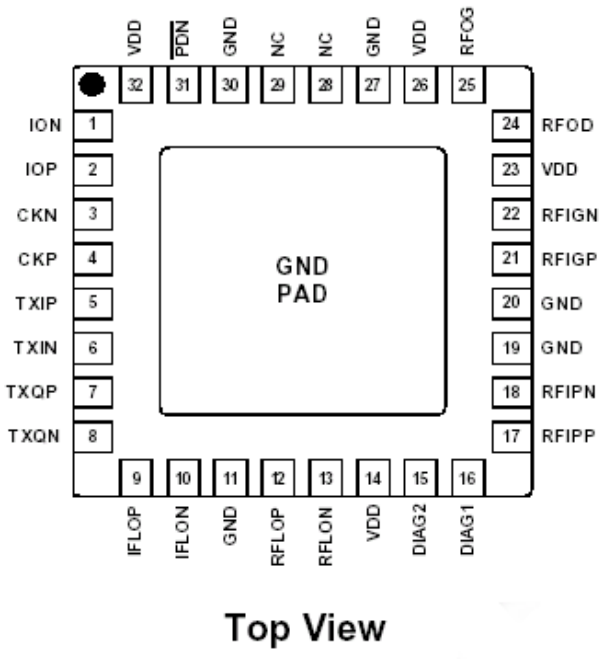
The frequency synthesizer (U601) includes integrated RF and IF VCO's, Varactors, and Loop filters.

The unique integer-N PLL architecture used in the Si4133T (U601) produces a transient response that is superior in speed to fractional architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

4.2.1 DC Distribution and Regulation Part

The battery voltage, in return, is applied to the logic part and RF part via LDO(Low Drop-Out) regulator. As several LDO regulators are used, power can be supplied for each necessary part efficiently. Audio/Logic parts use +2.8V. RF parts such as U702(Si4201 universal baseband interface), U710(Si4200 GSM Transceiver) and U601(Si4133T Dual RF synthesizer) also use +2.8V DC voltage.

4.2.2 Transciever pin description



Top View

Fig.4-3. Top View of Si4200DB-BM

Pin Number(s)	Name	Description
1, 2	ION, IOP	Data output to Si4201 (differential).
3, 4	CKN, CKP	Clock input from Si4201 (differential).
5, 6	TXIP, TXIN	Transmit I input (differential).
7, 8	TXQP, TXQN	Transmit Q input (differential).
9, 10	IFLOP, IFLON	IFLO Input from Si4133T (differential).
11, 19, 20, 27, 30, GND pad	GND	Ground. Connect to ground plane on PCB.
12, 13	RFLOP, RFLON	RFLO Input from Si4133T (differential).
14, 23, 26, 32	VDD	Supply voltage.
15, 16	DIAG2, DIAG1	Diagnostic output. Can be used as digital outputs to control antenna switch functions.
17, 18	RFIPP, RFIPN	PCS LNA input (differential). Use for DCS 1800 or PCS 1900 bands.
21, 22	RFIGP, RFIGN	GSM LNA input (differential). Used for GSM 850 or E-GSM 900 bands.
24	RFOD	DCS and PCS transmit output to power amplifier. Used for DCS 1800 and PCS 1900 bands.
25	RFOG	GSM transmit output to power amplifier. Used for GSM 850 and E-GSM 900 bands.
28, 29	NC	These pins should be left disconnected.
31	$\overline{\text{PDN}}$	Powerdown input (active low).

Table 4-1. Pin Description of Si4200DB-BM

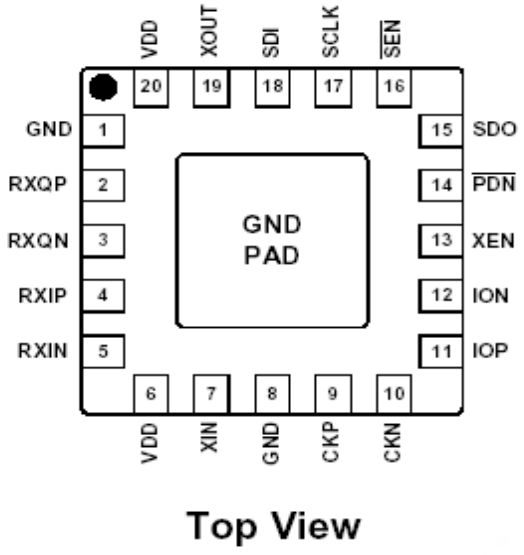


Fig.4-4. Top View of Si4201-BM

Pin Number(s)	Name	Description
1, 8, GND pad	GND	Ground. Connect to ground plane on PCB.
2, 3	RXQP, RXQN	Receive Q output (differential).
4, 5	RXIP, RXIN	Receive I output (differential).
6, 20	VDD	Supply voltage.
7	XIN	Reference frequency input from crystal oscillator.
9, 10	CKP, CKN	Clock output to Si4200 (differential).
11, 12	IOP, ION	Data input from Si4200 (differential).
13	XEN	XOUT pin enable
14	$\overline{\text{PDN}}$	Powerdown input (active low).
15	SDO	Serial data output.
16	$\overline{\text{SEN}}$	Serial enable input (active low).
17	SCLK	Serial clock input.
18	SDI	Serial data input.
19	XOUT	Clock output to baseband.

Table 4-2. Pin Description of Si4201-BM

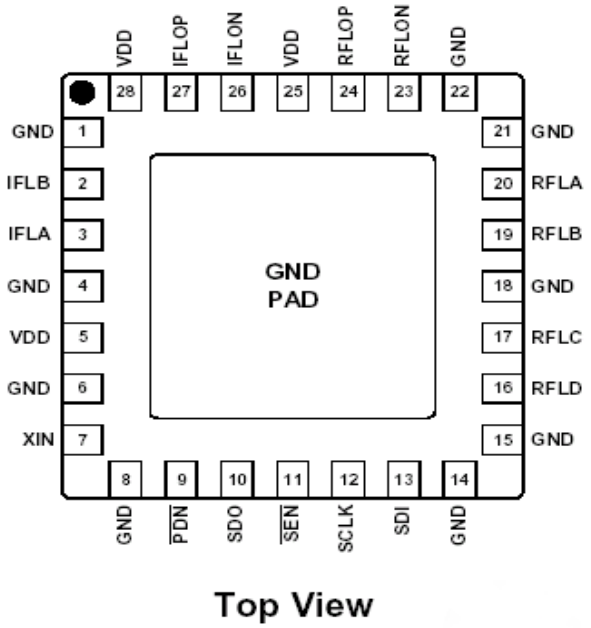


Fig.4-5. Top View of Si4133T-BM

Pin Number(s)	Name	Description
1, 4, 6, 8, 14, 15, 18, 21, 22, GND pad	GND	Ground. Connect to ground plane on PCB.
2, 3	IFLB, IFLA	Tuning inductor connection for IF VCO.
5, 25, 28	VDD	Supply voltage.
7	XIN	Reference frequency input from crystal oscillator.
9	$\overline{PDN}$	Powerdown input (active low).
10	SDO	Serial data output.
11	$\overline{SEN}$	Serial enable input (active low).
12	SCLK	Serial clock input.
13	SDI	Serial data input.
16, 17	RFLD, RFLC	Tuning inductor connection for RF2 VCO.
19, 20	RFLB, RFLA	Tuning inductor connection for RF1 VCO.
23, 24	RFLON, RFLOP	RF PLL output to Si4200 (differential).
26, 27	IFLON, IFLOP	IF PLL output to Si4200 (differential).

Table 4-3. Pin Description of Si4133T-BM

4.2.3 Receiver Section

4.2.3.1 An Overview of Receive section

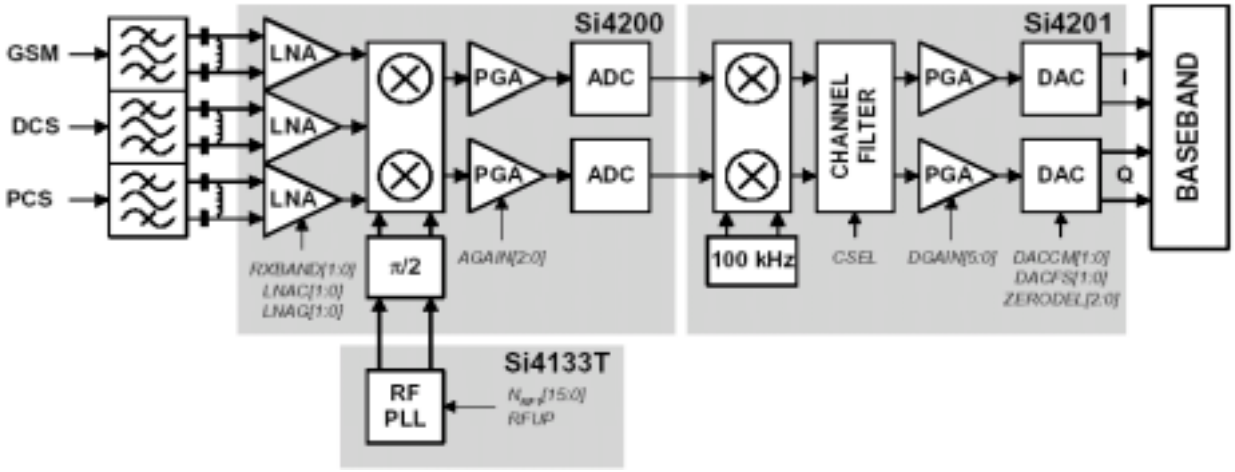


Fig.4-6. Receiver block diagram

The G310 model's Aero transceiver uses a low-IF receiver architecture that follows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF SAW filter required in conventional superheterodyne architectures. Compared to a direct conversion architecture, the low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, 2nd order distortion of blockers, and device 1/f noise. This relaxes the common-mode balance requirements on the input SAW filters and simplifies PC board design and manufacturing.

The Si4200 integrates three differential-input LNAs(At G310, we only used two inputs that are EGSM and PCS). The GSM input supports EGSM 900 (925– 960 MHz) band. The PCS input supports the PCS 1900 (1930 – 1990 MHz).

A quadrature image-reject mixer downconverts the RF signal to a 100 kHz intermediate frequency (IF) with the RFLO from the Si4133T frequency synthesizer. The RFLO frequency is between 1737.8 and 1989.9 MHz, and is divided by two in the Si4200 for GSM 850 and EGSM 900 modes. The mixer output is amplified with an analog programmable gain amplifer (PGA), which is controlled with the AGAIN[2:0] bits in register 05h. The quadrature IF signal is digitized with high resolution A/D converters (ADCs).

The Si4201 downconverts the ADC output to baseband with a digital 100 kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN[5:0] bits in register 05h.

These analog and digital gain resigters must be set to provide a constant amplitude signal to the baseband receive inputs.

DACs drive a differential analog signal onto the RXIP,RXIN,RXQP and RXQN pins to interface to standard analog-input baseband Ics.

4.2.3.2 Receiver Part

A. Diplexer: Z701

Diplexer consists of Tx filter, having an antenna port, and dual configuration with the transmitting path isolated from the receiving path. A signal receives from the antenna of frequency band which is 942.5±17.5MHz for EGSM bands, 1960.2±30 MHz forPCS bands and transmits it to dual saw filter. The Tx filter passes through the output signals of frequency band that is 897.5MHz ±17.5MHz for EGSM bands, 1880.2 ±30 MHz for PCS bands from the power amplifier and transmits it to the antenna. The maximum insertion loss is about 0.8 dB for the receiving bands at 25° C and about 1.35 dB for the transmitting bands at 25° C.

B. SAW filter (BPF / Band select filter): Z510, Z511

The **Z510** filter is for the EGSM band signals which range 942.5±17.5MHz with low insertion loss. And the **Z511** filter passes the PCS bands that cover 1960.2±3MHz.

These filters degrade other band signals with high passing loss of 30~60 dB. The EGSM and PCS's maximum insertion loss is 3.2 dB.

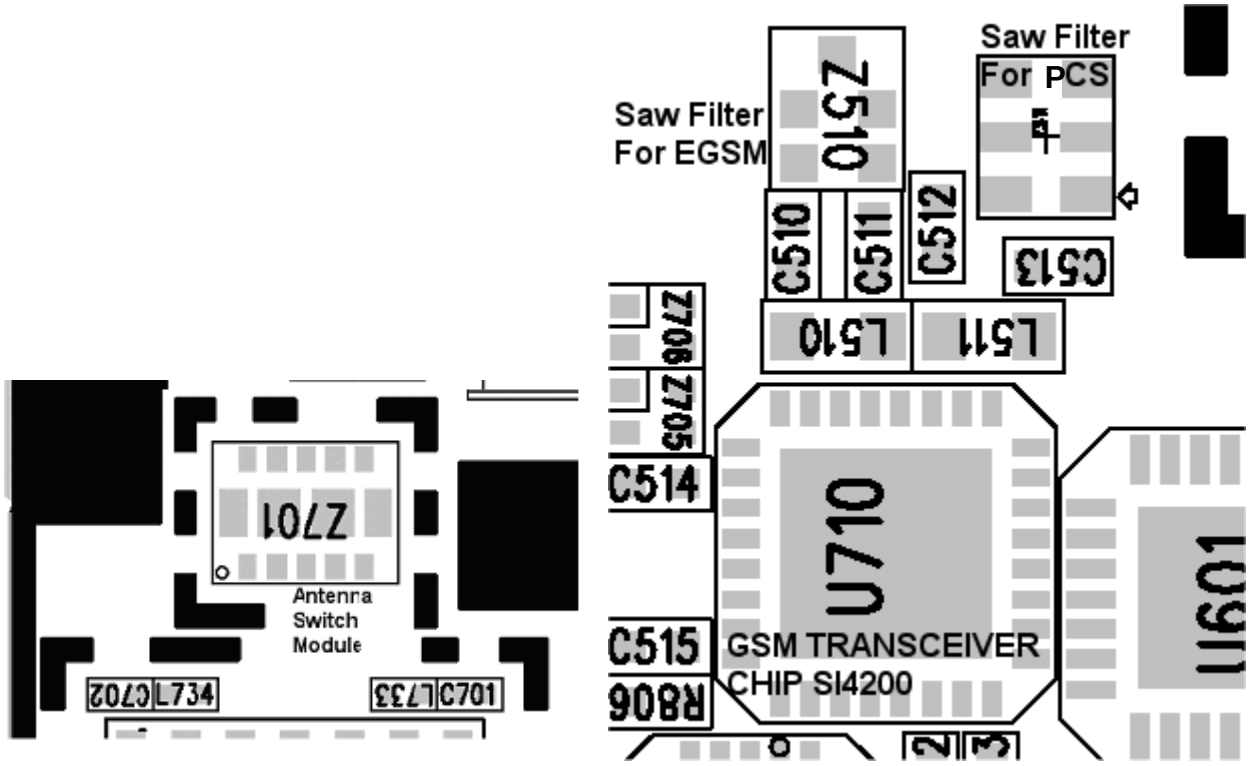


Fig.4-7. Receiver part PCB Layout

4.2.4 Transmit Section

4.2.4.1 An Overview of Transmit Section

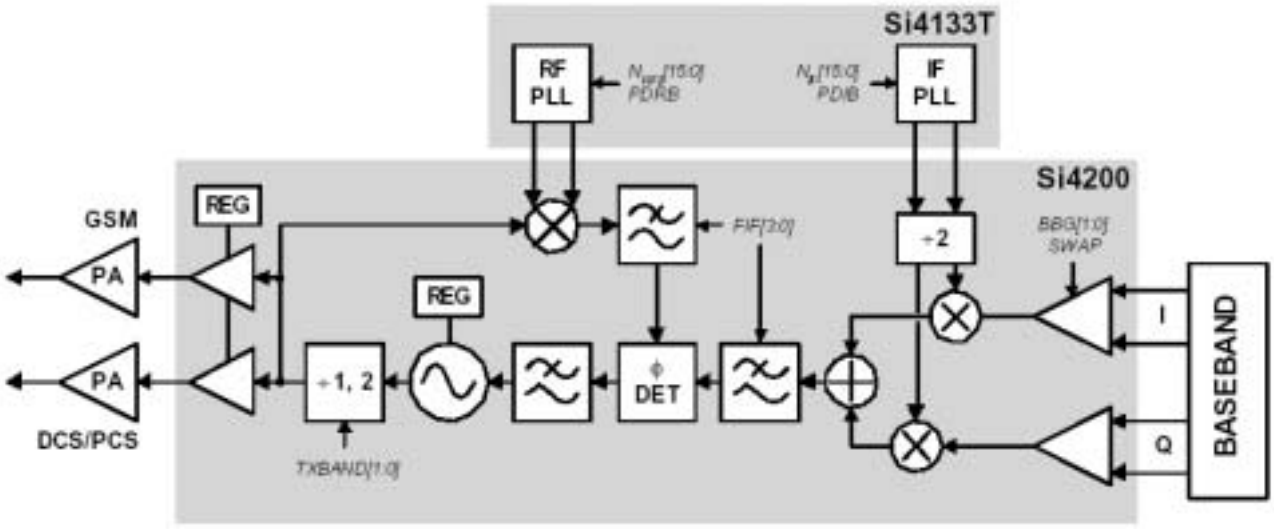


Fig.4-8. Transmitter block diagram

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two 50 ohms output buffers that can drive external power amplifiers (PA), one for the EGSM 900 (880 – 915 MHz) bands and one for the PCS 1900 (1850 – 1910 MHz) bands. The OPLL requires no external duplexer to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power. Additionally, the output of the transmit VCO (TXVCO) is a constant-envelope signal which reduces the problem of spectral spreading caused by nonlinearity in the PA.

A quadrature mixer upconverts the differential in-phase (TXIP,TXIN) and quadrature(TXQP,TXQN) signals with the IFLO to generate a SSB IF signal which is fitered and usesd as the reference input to the OPLL. The Si4133T generates the IFLO frequency between 766 and 896 MHz. The IFLO is divided by two to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz.

The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the DCS 1800 and PCS 1900 bands, and its output is divided by two for the generate the RFLO frequency between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the EGSM 900 bands, and low-side injection is used for the DCS 1800 and PCS 1900 bands. The I and Q signals are automatically swapped within the Si4200 when switching bands.

Low-pass fitlers before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. The cutoff frequency of the filters is programmable.

4.2.4.2 Transmitter Part

A. 6 dB attenuator : Z705, Z706

These passive components are adopted for PAM to operate in a stable output power.

B. ASM(Antenna Switch Module / built in LPF): Z701

These filters pass through the signals of which frequency band of 880~915MHz, 1850 – 1910 MHz which is the transmit frequency of GSM, PCS system terminal, and it suppresses other images and spurious frequencies when the terminal transmits GMSK modulated frequencies.

C. Power AMP Module(PAM): Z710

This device amplifies signals ahead of transmiting them through the antenna to provide a sufficient RF power. It has amplification factor of 28dB and efficiency of about 55% typically in GSM band and amplification of 27dB and efficiency of about 52% typically PCS band.

D. RF Switch connector: J701

RF Swithc connector used to test Mainboard's RF characteristics.

E. Antenna: Antenna Contact Plate

This device enables signals to be transmitted and received from BTS by Um interface.

External Antenna can be contacted with Mainboard through Antenna Contact Plate.

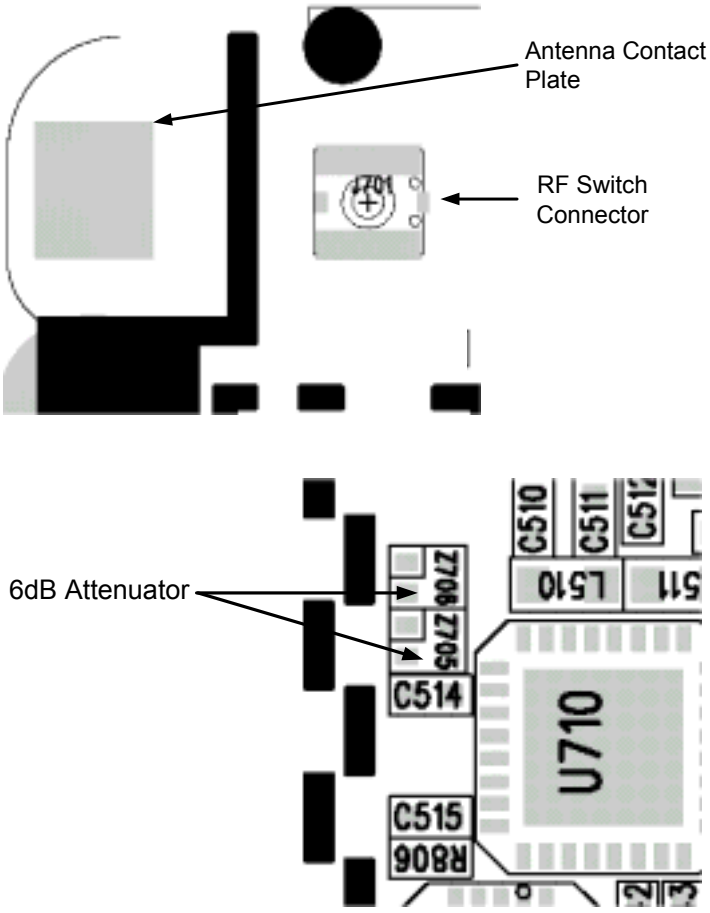


Fig.4-9. Transmit part PCB Layout

4.2.5 Offset PLL

4.2.5.1 An Overview of Offset PLL

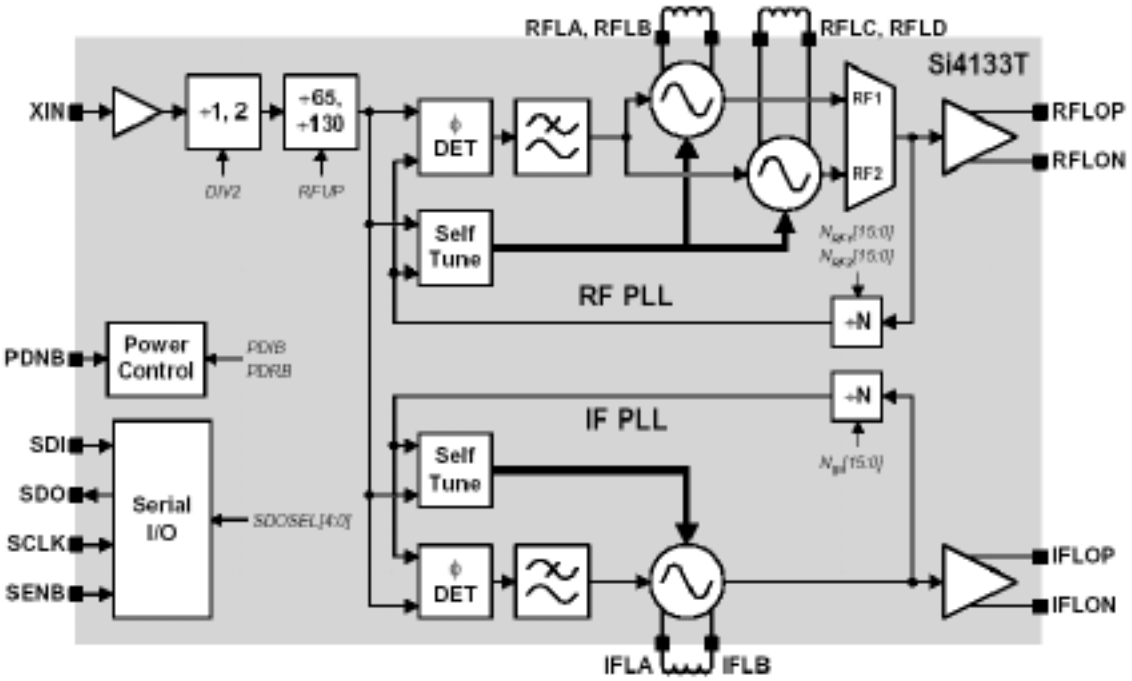


Fig.4-10. Si4133T Frequency Synthesizer Block Diagram

The Si4133T dual frequency systhesizer is a monolithic CMOS integrated circuit that performs IF and RF synthesis. Two complete PLLs are integrated including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. Differential outputs for the IF and RF PLLs are provided for direct connection to the Si4200 transceiver IC. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for Receive mode, and RF2 VCO is used for Transmit mode. The IF PLL is used only during Transmit mode and uses a single VCO.
The frequency synthesizer uses VC-TCXO(13MHz) as reference frequency. 13MHz of VC-TCXO is sent to the frequency synthesizer as a reference input.

4.2.5.2 VC-TCXO(Voltage Controlled Temperature Compensated Crystal Oscillator): V801

This is the mobile station's reference frequency source. Its frequency is 13MHz, this signal is applied to Si4133T(U601)_pin7, Si4201(U702)_ pin7 and AD6526(U101).

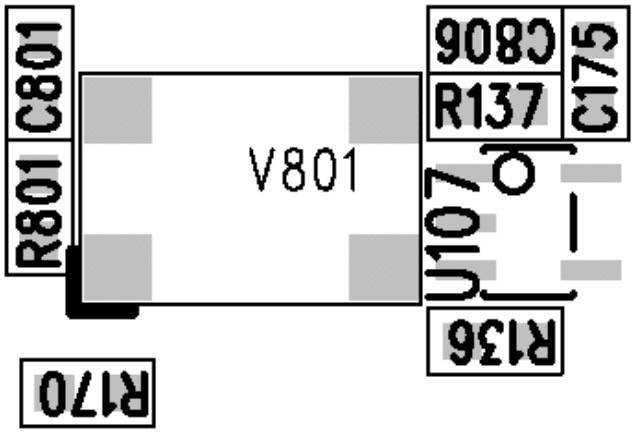


Fig.4-11. Top view of VCTCXO part on the PCB artwork

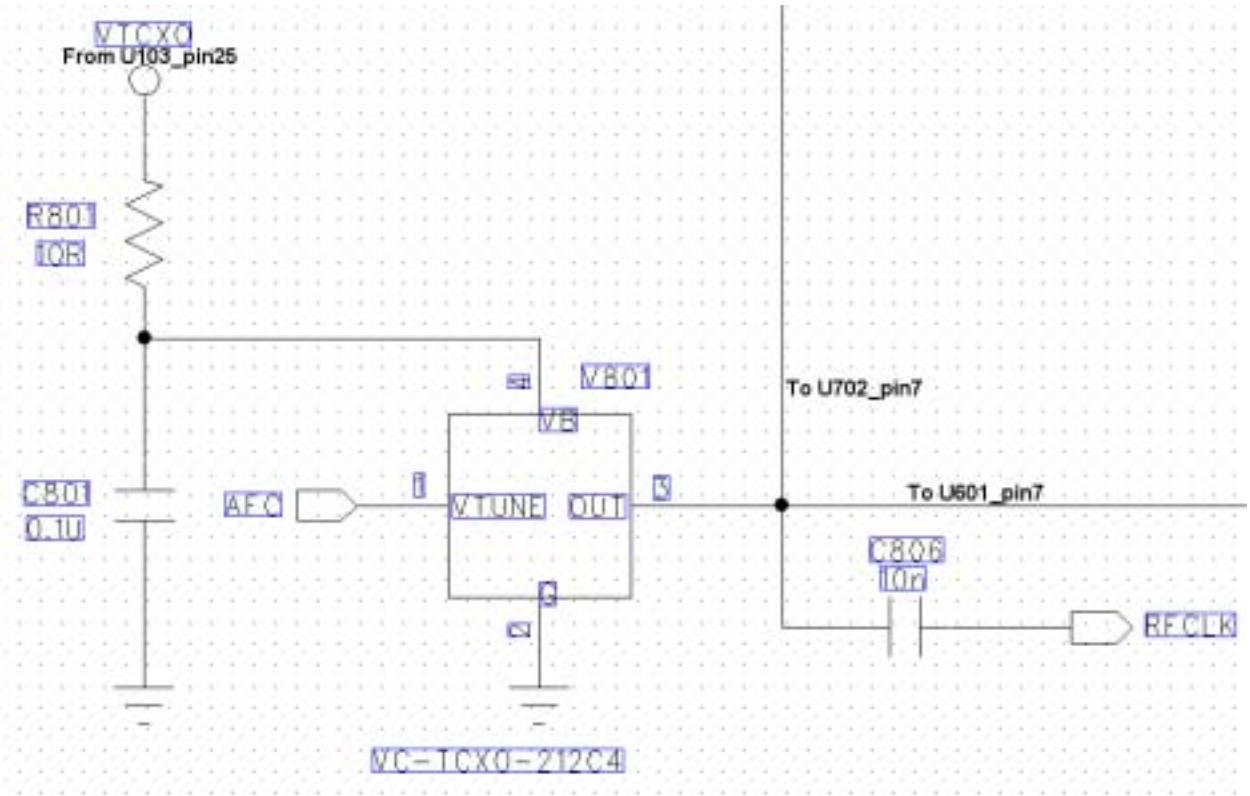


Fig.4-12. VCTCXO schematic circuit

Section 5. Alignment Procedure

5.1 Recommended Test Equipment

Model No.	Description	Maker	Remark
8960	GSM Mobile Station Test Set	Agilent Technologies	
8593E	Spectrum Analyzer	Hewlett Packard	
TDS 340A	Oscilloscope	Tektronix	
FLUKE 87	Digital Multimeter	Fluke	
E3630A	DC Power Supply	Hewlett Packard	
Others	Accessory		Interface Connectors RF Connectors

5.2 Connection of Test Equipment

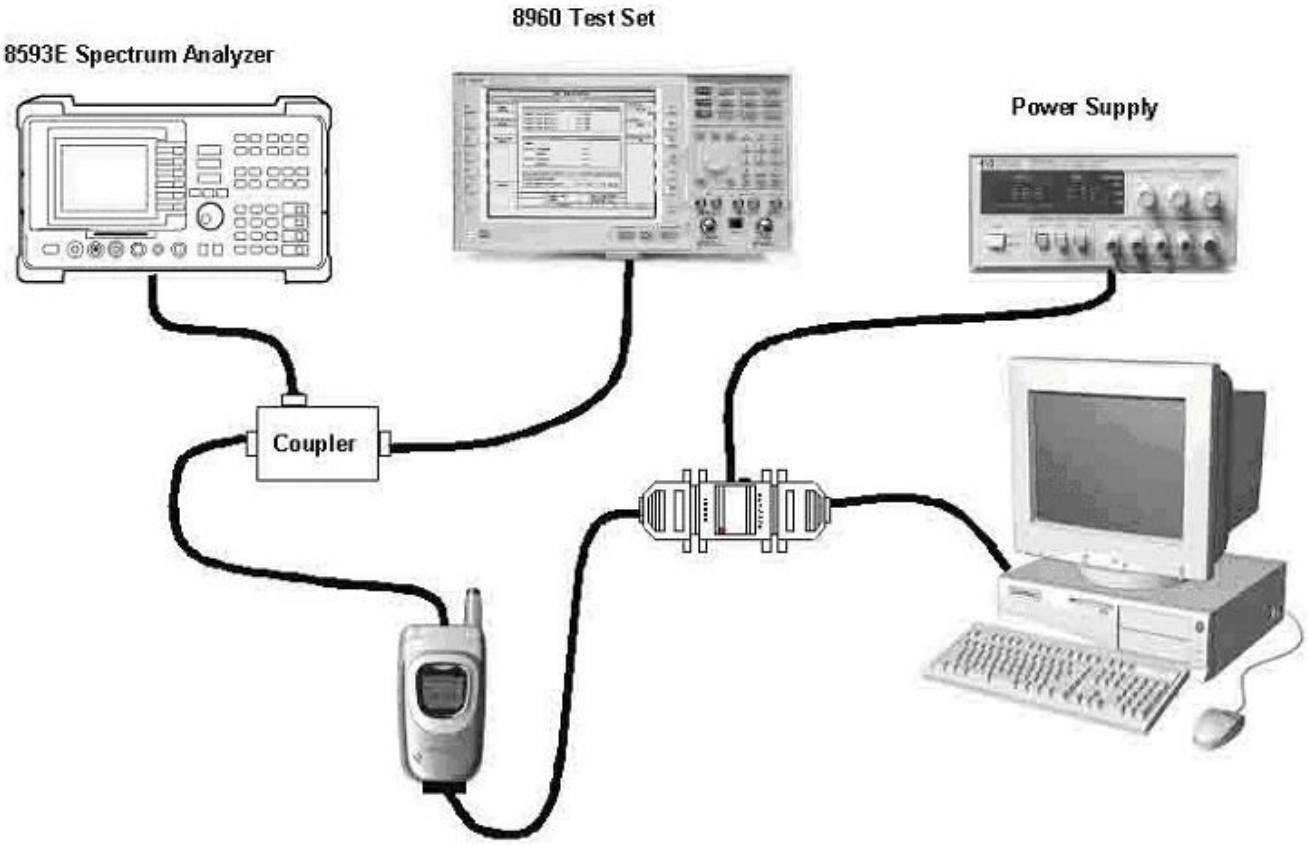


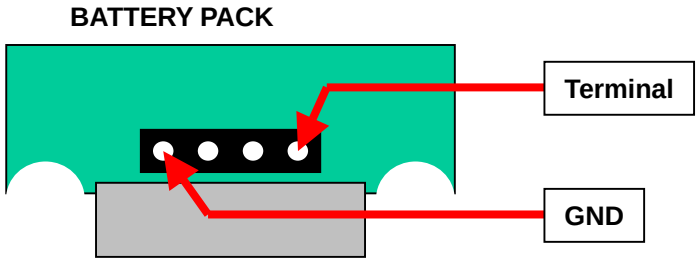
Fig.5-1. Test Set Configuration

SECTION 6. Equipment Repair Procedure

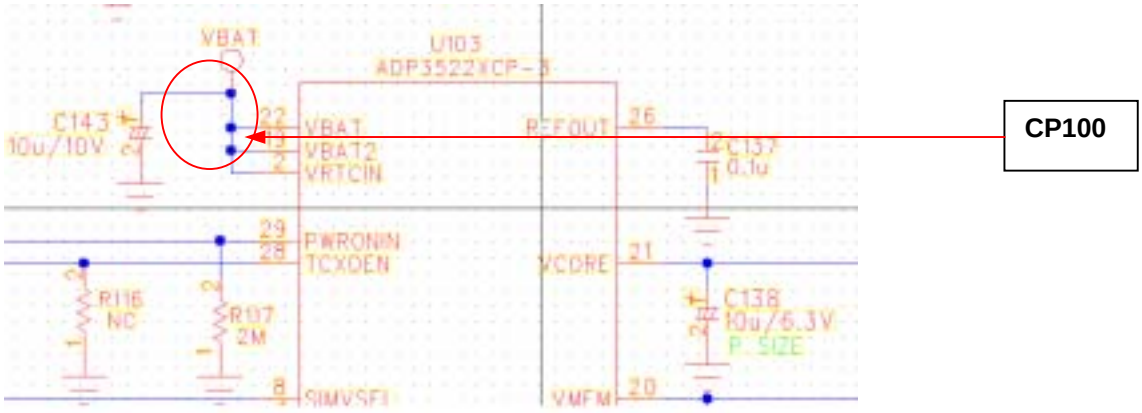
6.1 No Power On with battery Applied.

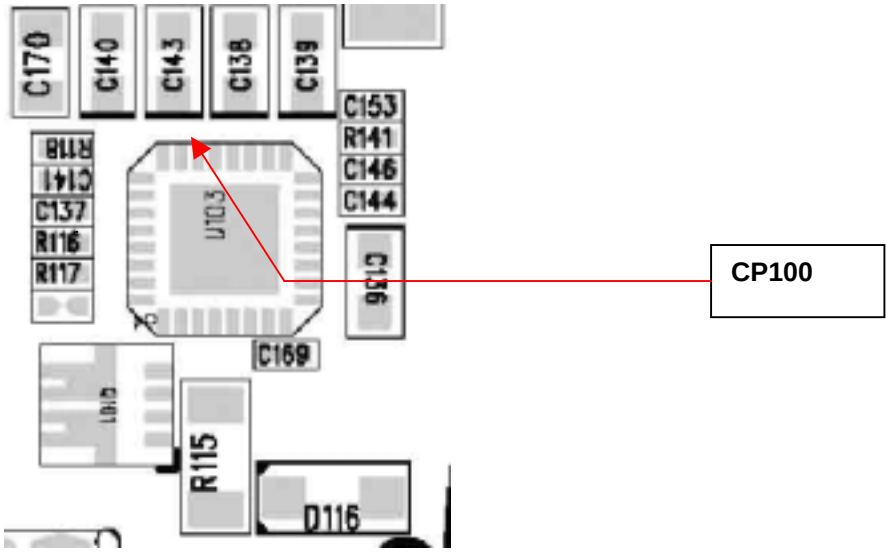
6.1.1 Power CHECK

1. Check battery power : 3.5V~4.2V.

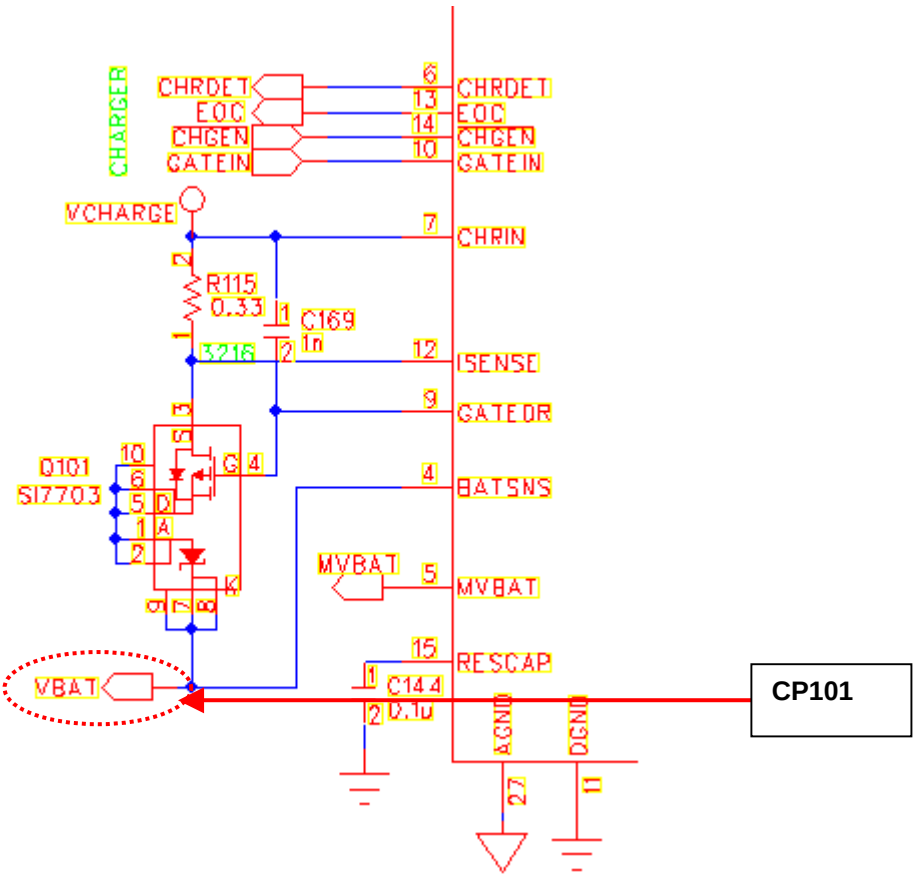


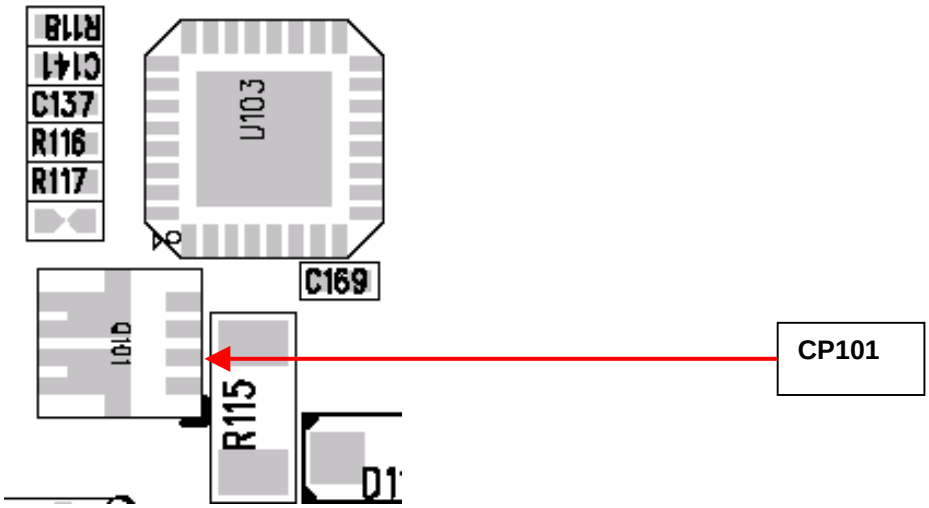
2. Check to see if U103.22 pin voltage is same with battery power : CP100



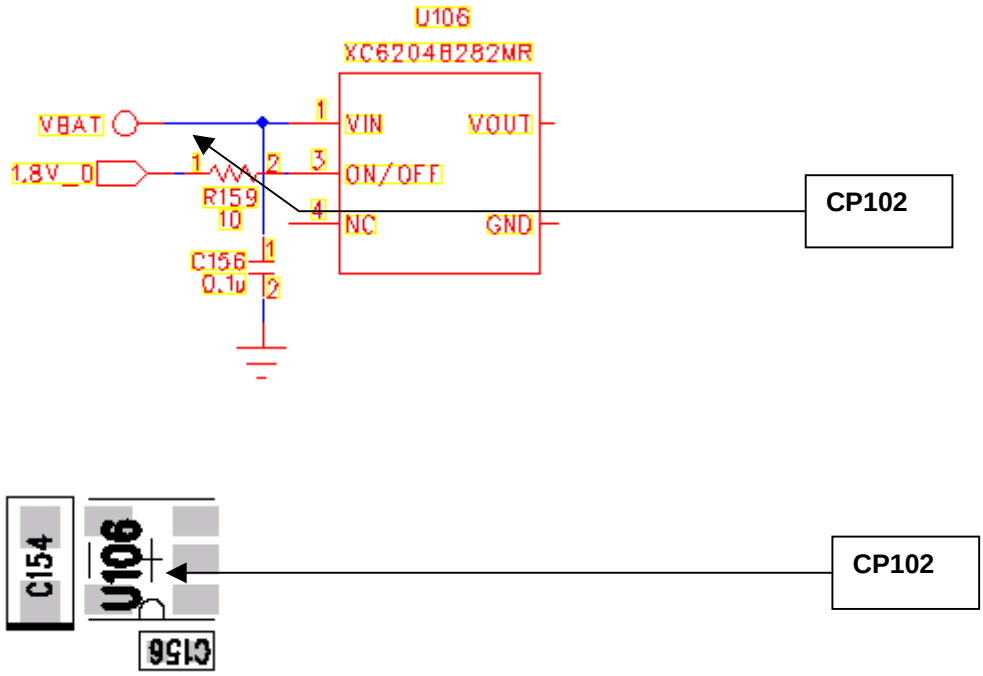


3. Check to see if Q101.7.8 and 9 pin is same with battery power : CP101

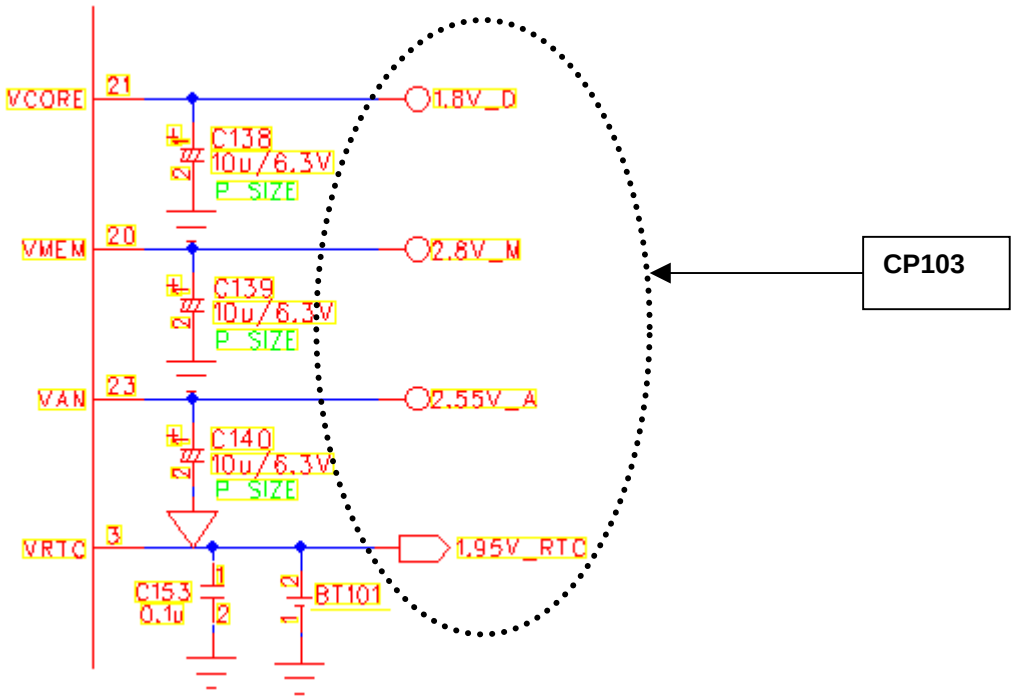


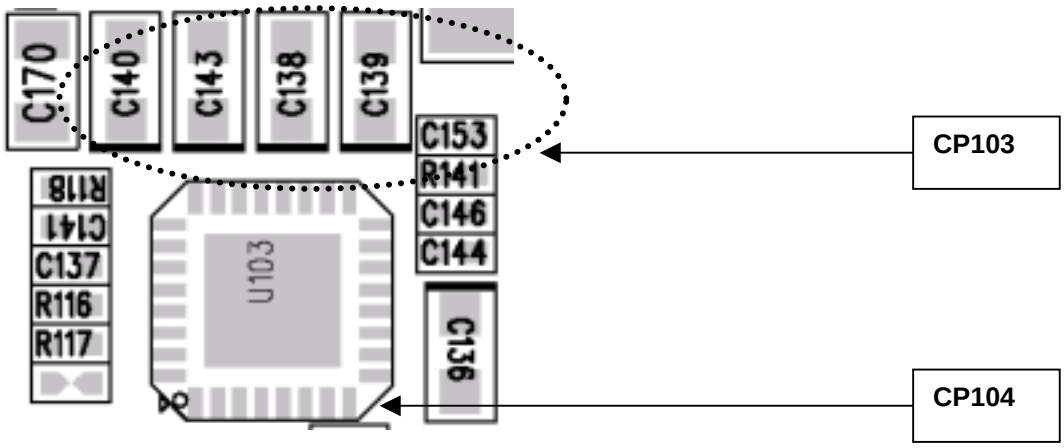


4. Check to see if U106 .1 pin is same with battery power : CP102



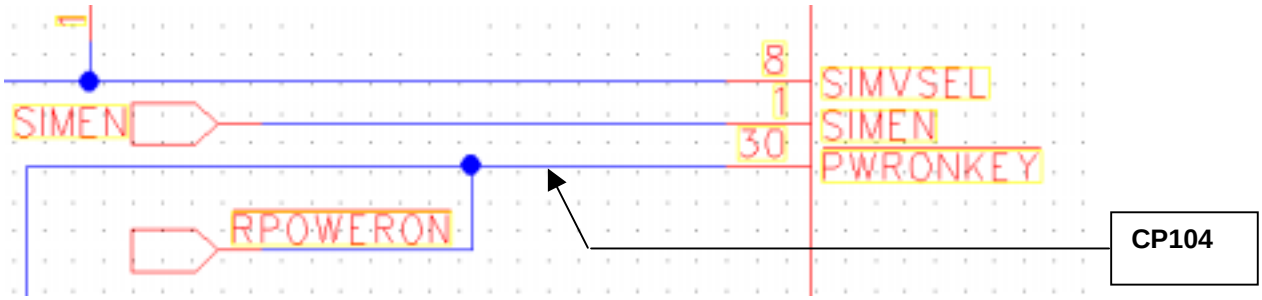
5. Check to see if U103. 21,20.23 and 3 pin is 1.8V, 2.8V, 2.55V and 1.95V : CP103



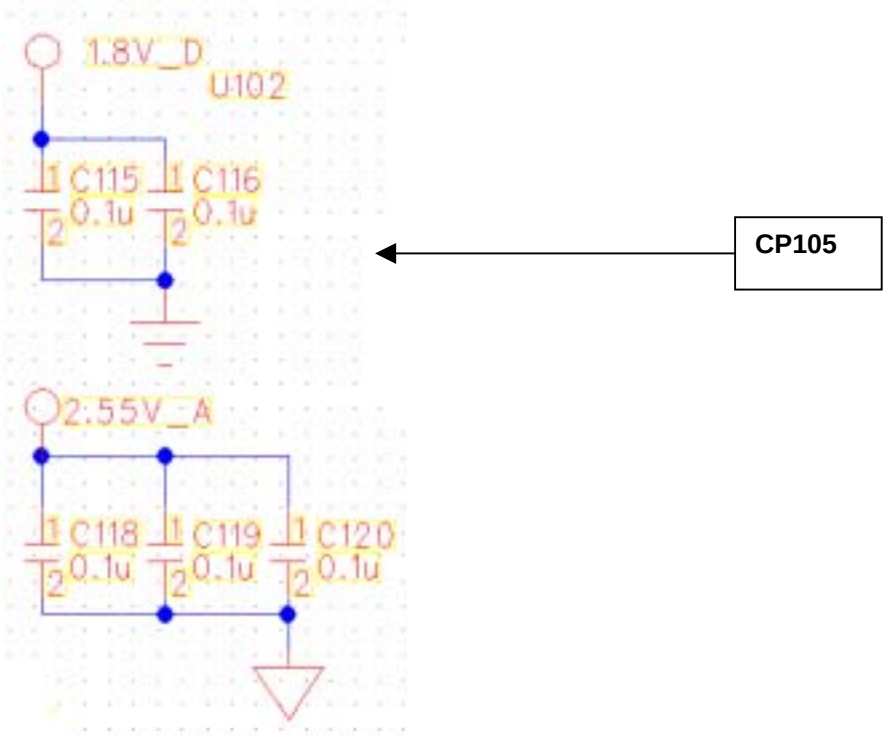


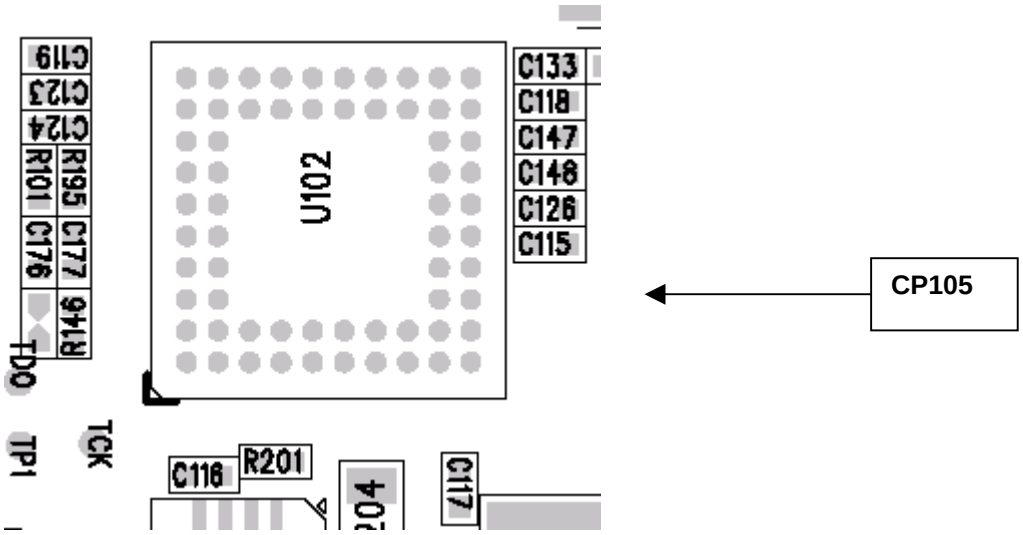
6. Check to see if U103.30 pin becomes to 0V : CP104

Pressing “END” key to turn on equipment.

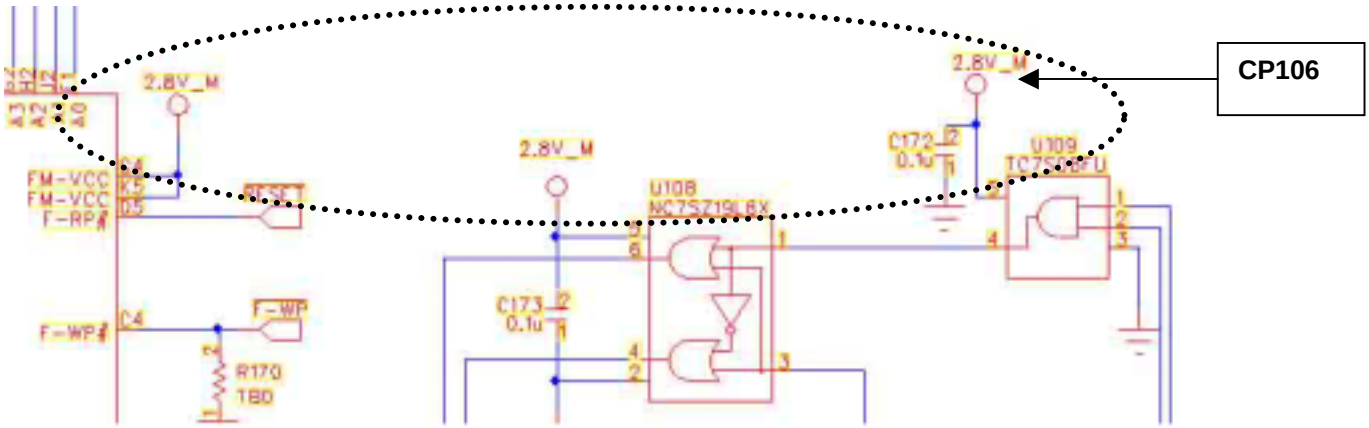


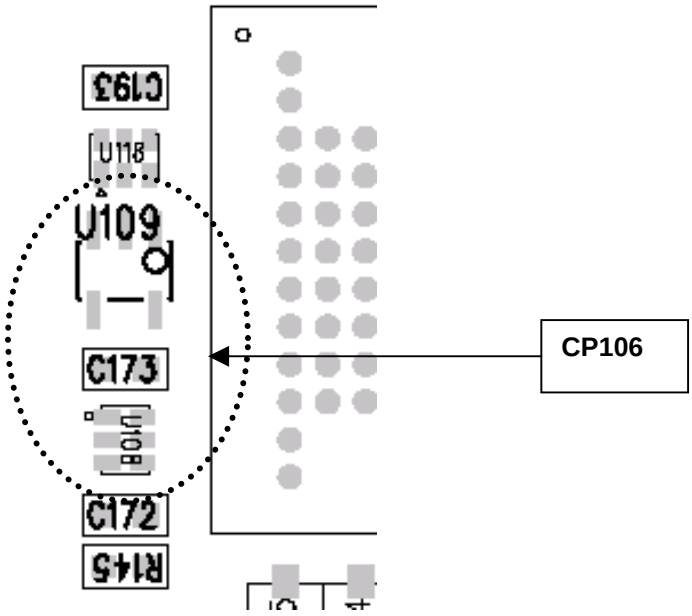
7. Check to see if C115 and C116 is 1.8V, C118, C119 and C120pin is 2.45V : CP105



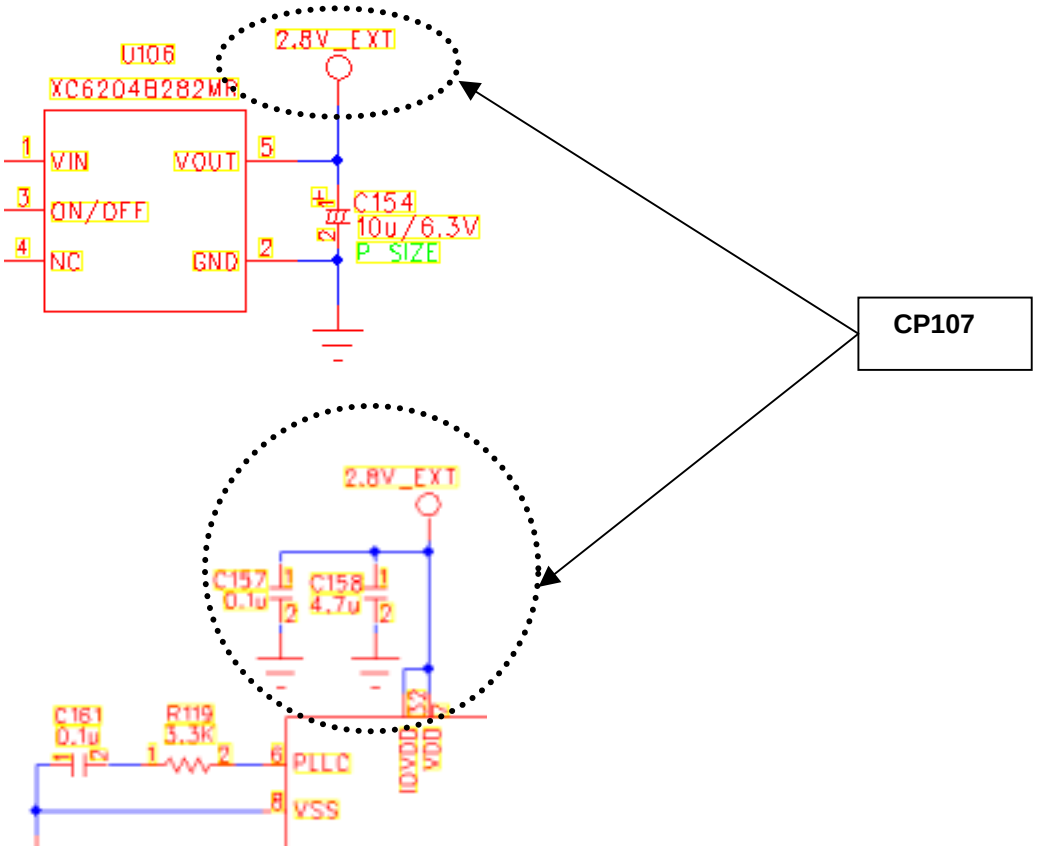


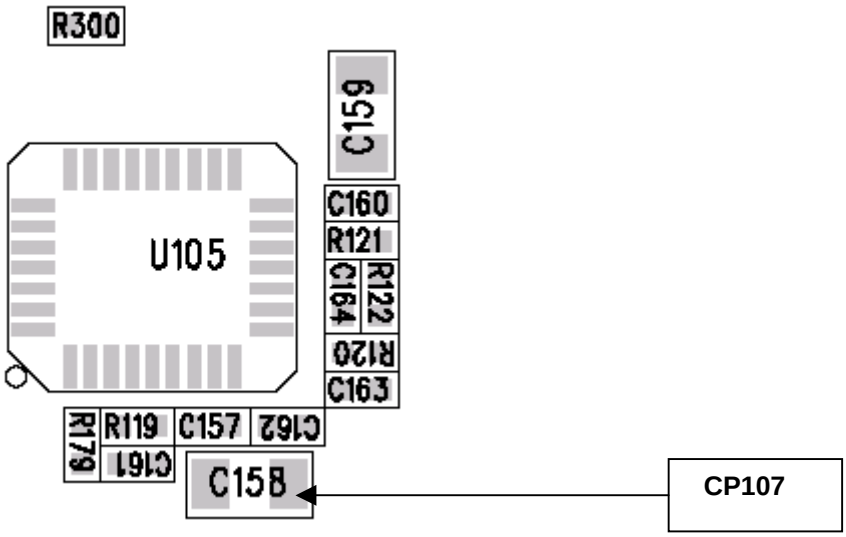
8. Check to see if U104.39,12 pin , U117.5pin and U122.5 pin is 2.8V : CP106





9. Check to see if U106.5 pin and U105.7.32 pin is 2.8V : CP107

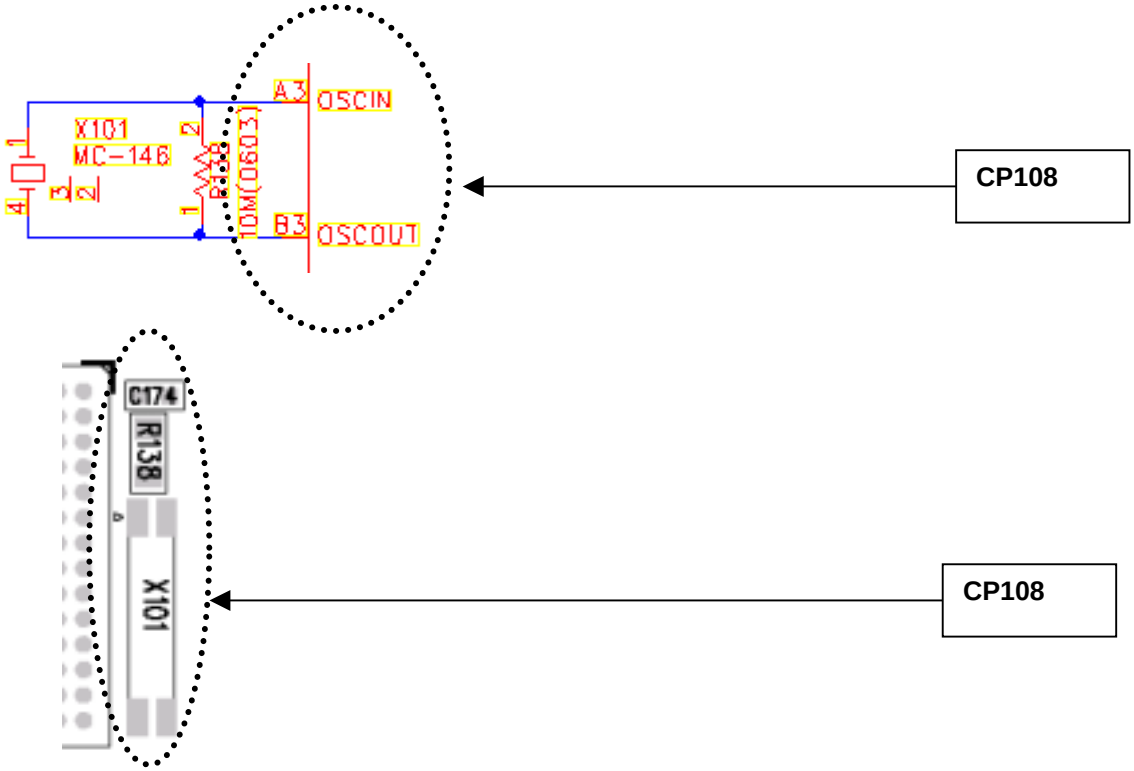




6.1.2 Oscillation CHECK

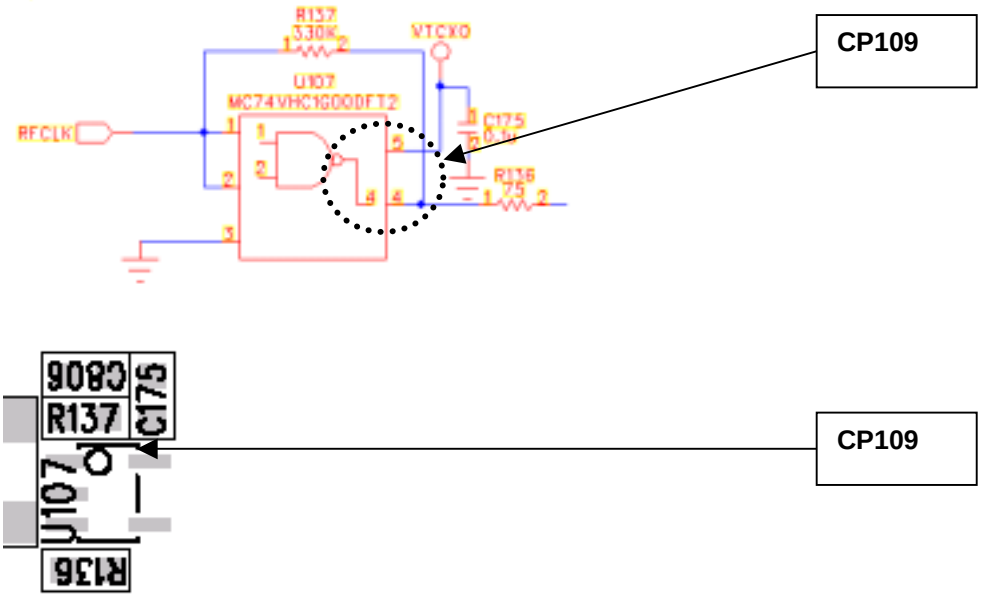
1. Check to see if U101 No. A3 and B3 pin is oscillated(32.768KHz) : CP108

NO → Check R138 and then replace X101



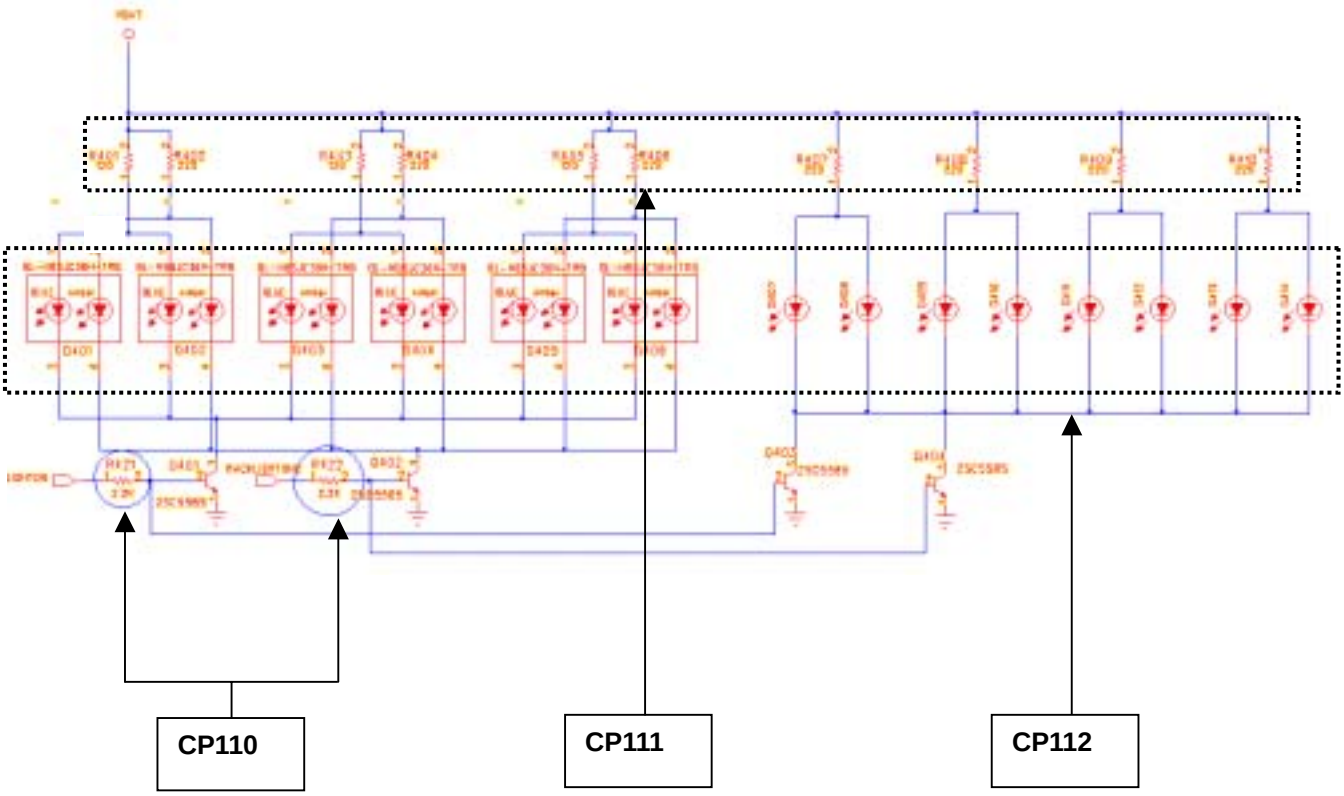
2. Check to see if U107.4 pin Master Clock(13MHz). : CP109

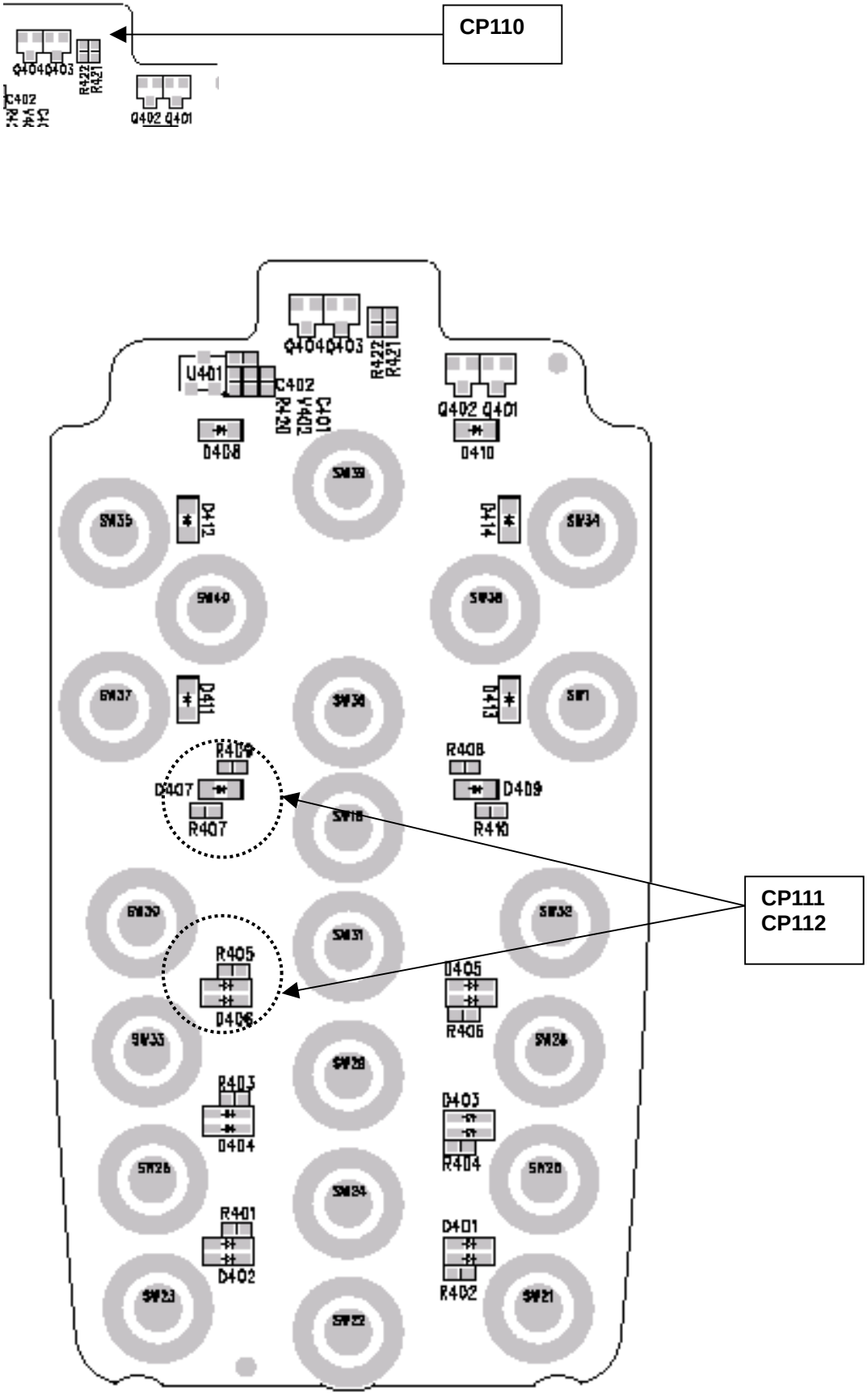
NO → Check U107 No. 1.2 pin and then check the PCB pattern, soldering



6.1.3 KEYPAD LED Not in Operation (3-color and blue)

1. Check to see if R421 and 422.1 are around 2.8V (duty: 80%, 256Hz) : CP110
   NO → Check R421, 422, Q401, 402, 403 and 404, and then replace those.
2. Check to see if R401 ~ R410 are same with battery voltage : CP111
   NO → Check the PCB pattern between battery and the resistors.
   NO → Replace the resistors.
3. Check to see if D401 ~ 414 are well operated by multimeter : CP112
   NO → Replace the LEDs.

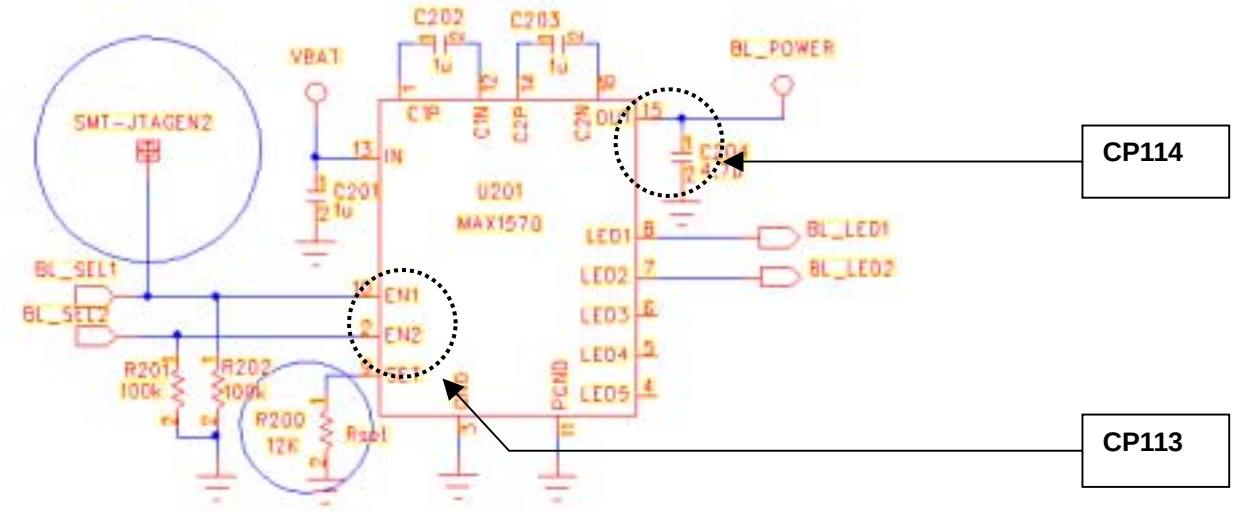


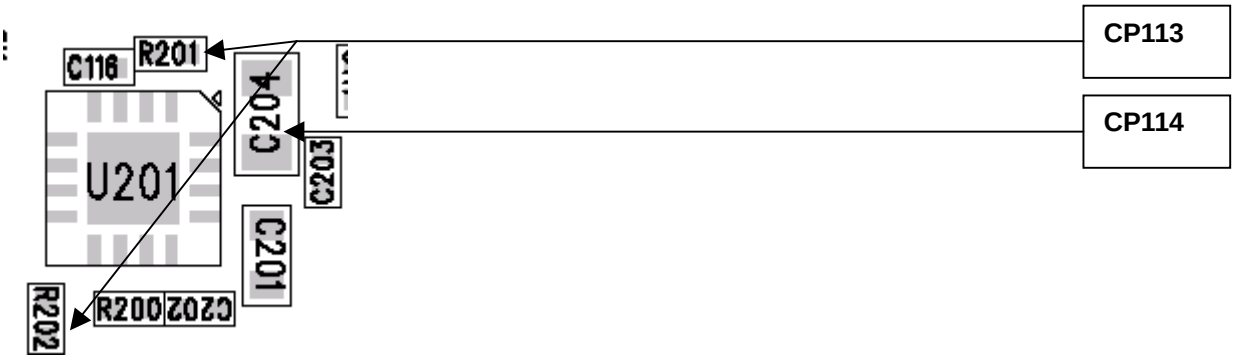

CP110
CP111
CP112
Q404 Q403
R422
R421
U401
C402
C401
R420
Q402 Q401
D408
D410
D412
D414
D411
D413
R409
D407
R407
R408
D409
R410
R405
D406
D405
R406
R403
D404
D403
R404
R401
D402
D401
R402

6.1.4 LCD Backlight Not in Operation (White)

1. Check to see if U201.2 and 10 pins are 2.8V: CP113
2. Check to see if U201.15 pin (C204) is over 3V : CP114

   NO → Replace the U201.





6.1.5 Power indicated LED & Status LED

During Stand By Mode

Status → LED Should be flashing during Stand By (Blue).

1. Check to see if Q202.2 pin voltage is around 2.8V : CP115

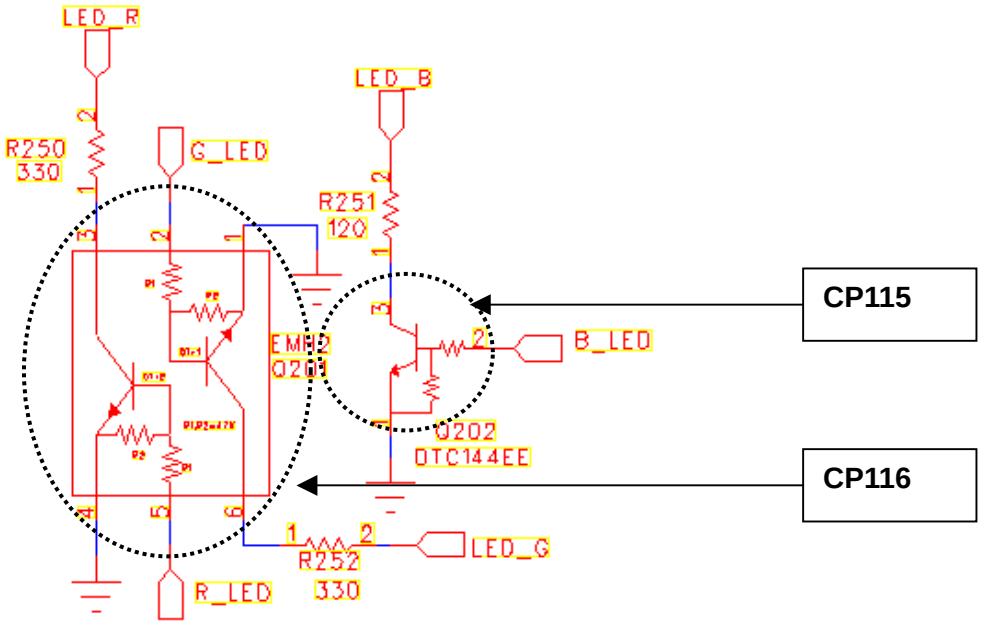
   NO → Replace the Transistors.

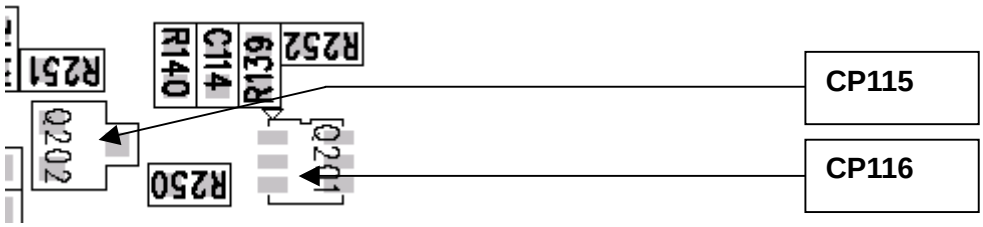
During Incoming Call Mode.

Status → LED should be blinking during Incoming Call (all colors: Green, Red, Blue).

1. Check to see if Q201 and Q202 are well operated. : CP115, CP116

   NO → Replace the Transistors.





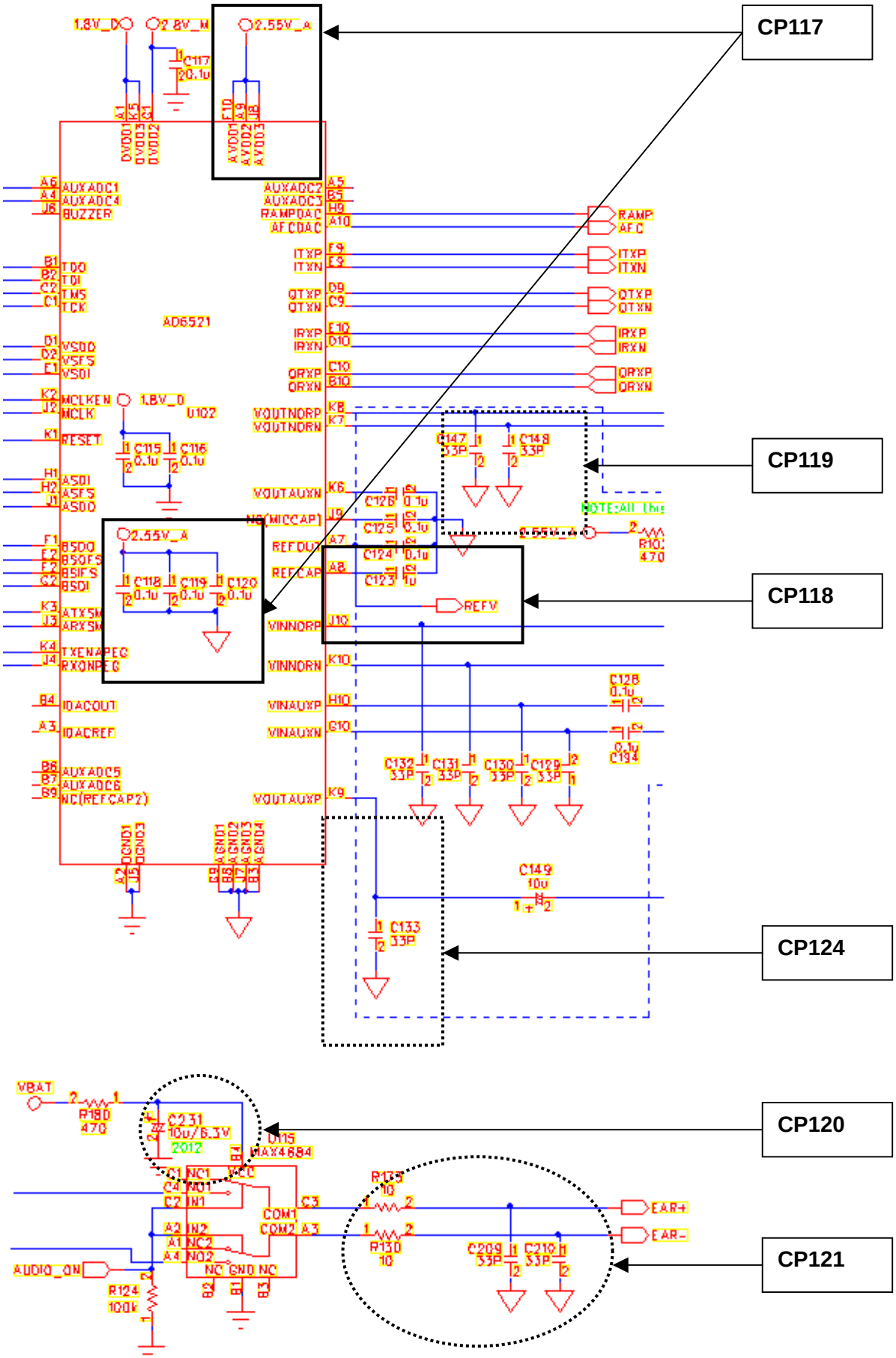
6.2 Audio Part (Earpiece, Hands-free Earphone, Microphone, Hands-free Mic)

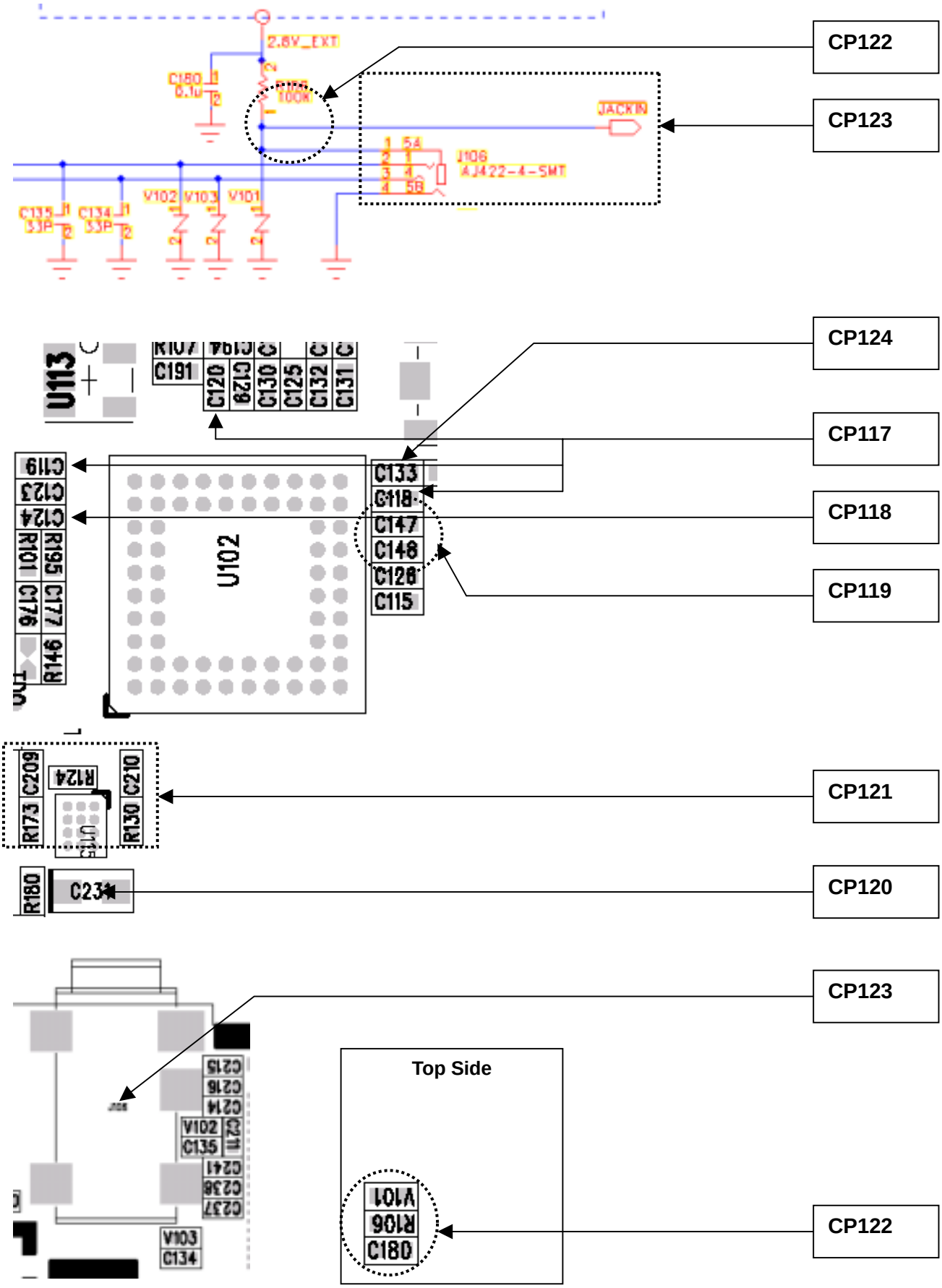
6.2.1 No receiving tone heard (Ear-piece)

1. Check to see if U102.F10, A9 and J8 (C118, C119, C120) is 2.55V_A : CP117
2. Check to see if U102.A7 (C124) is around 1.2V : CP118
   Set to HP8922M to connect a call and then set to 1kHz.
3. Check U102.K8 and K7 (C147, C148) pins (Ear Signal) for waveform : CP119
   NO → Replace U102.
4. Check to see if U115.B4 (C231) pin is battery voltage : CP120
   NO → Replace U115.
5. Check U115.A3 and C3 (R130 and R173) pin for waveform : CP121
   NO → Replace U115.

6.2.2 No Receivng tone heard (Hands-free Earphone)

1. Check to see if U102.F10, A9 and J8 (C118. C119. C120) is 2.55V_A: CP117
2. Check to see if U102.A7 (C124) is around 1.2V : CP118
3. Check to see if U101.B11 (V101) is around 0V: CP122
   NO → Check to see J106 : CP123
   Set to HP8922M to connect a call and then set to 1kHz.
4. Check C133.1 pin for waveform : CP124
5. Check Hands-free Earphone


CP117
CP119
CP118
CP124
CP120
CP121
1.8V_D
2.8V_M
2.55V_A
AD6521
U102
AUXADC1
AUXADC4
BUZZER
AUXADC2
AUXADC3
RAMPDAC
AFCDAC
RAMP
AFC
ITXP
ITXN
QTXP
QTXN
IRXP
IRXN
QRXP
QRXN
TDO
TDI
TMS
TCK
VSDO
VSFS
VSDI
MCLKEN
MCLK
RESET
ASDI
ASFS
ASDO
BSDO
BSFS
BSIFS
BSDI
ATXSM
ARXSM
TXENABLE
RXONABLE
IDACOUT
IDACREF
AUXADC5
AUXADC6
NC(REFCAP2)
VOUTNORP
VOUTNORN
VOUTAUXN
NC(MICCAP)
REFOUT
REFCAP
VINNORP
VINNORN
VINAUXP
VINAUXN
VOUTAUXP
REFV
DGND1
DGND2
DGND3
AGND1
AGND2
AGND3
AGND4
C117
C115
C116
C118
C119
C120
C147
C148
C126
C125
C124
C123
C128
C194
C132
C131
C130
C129
C149
C133
R10
470
VBAT
R180
470
C231
10u/6.3V
2012
U15
MAX4684
NC1
NO1
C1
C4
IN1
C2
IN2
A2
A1
NC2
A4
NO2
NC
GND
NC
COM1
COM2
C3
A3
R123
10
R130
10
C209
33P
C210
33P
EAR+
EAR-
AUDIO_ON
R124
100K


CP122
CP123
CP124
CP117
CP118
CP119
CP121
CP120
CP123
CP122
Top Side
2.8V_EXT
JACKIN
J106
AJ422-4-SMT
U113
U102

6.2.3 Side Tone Not transmitted (Ear-piece)

Repeat 6-2-1 No receiving tone heard.(Ear-piece)

1. Check to see if Mic + pin is around 1.8V : CP125

NO → Check that R102, C181 and R104 is cold solder, broken, short to the other PCB pattern or not

If you find out any defective part, you replace it.

Set to HP8922M to connect a call and then set to 1kHz with Echo audio mode.

2. Check U102.J10 (C132) pins for wave form : CP126

NO→ Replace MIC

6.2.4 Side Tone Not transmitted (Hands-free Mic.)

Repeat 6-2-2 No receiving tone heard.(Hands-free Earphone).

1. Check to see if U102. H10 (C130) pin is 2.5V : CP127

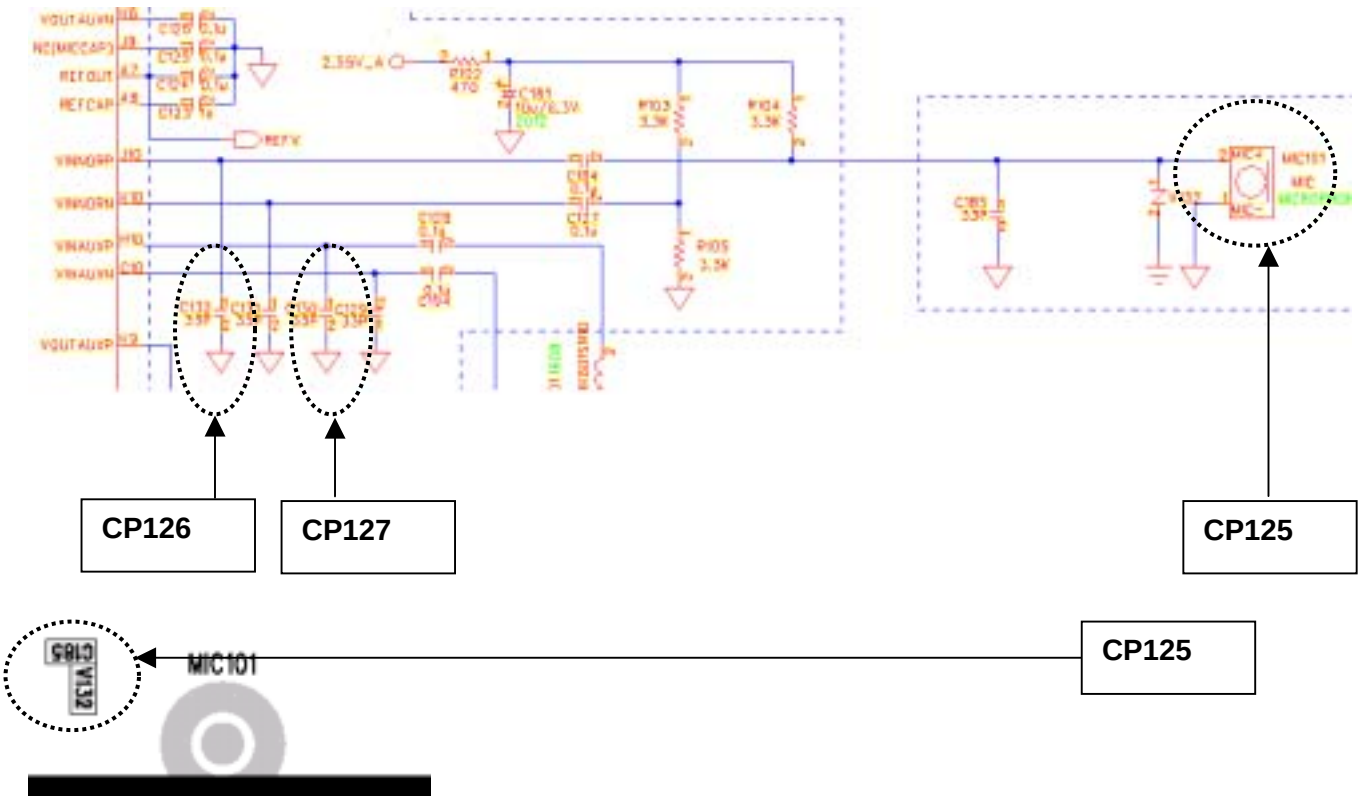
NO → Check that R107, R108, C150 and C151 is cold solder,broken,short to the other PCB pattern or not.

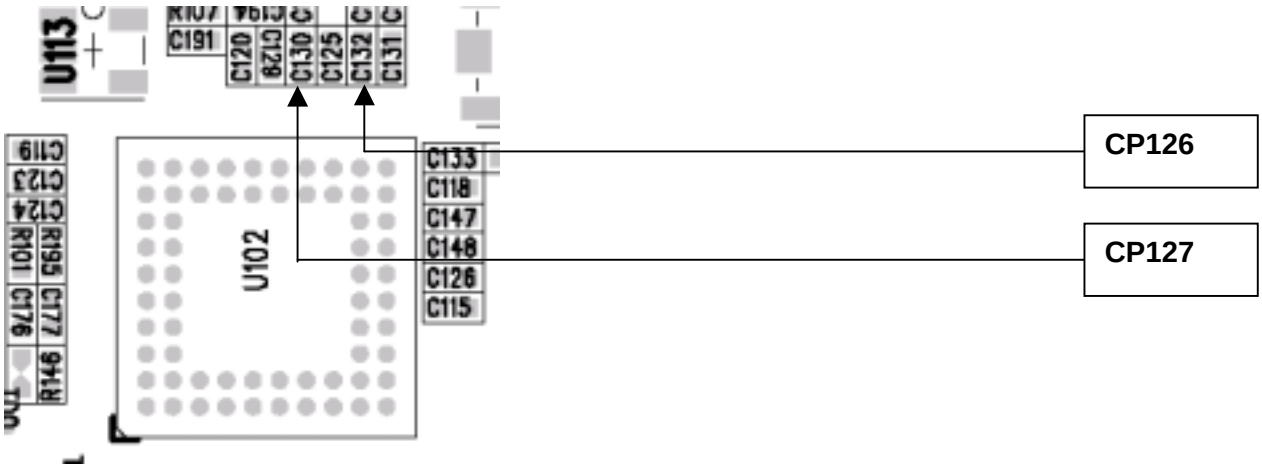
If you find out any defective part, you replace it.

Set to HP8922M to connect a call and then set to 1kHz with Echo audio mode.

3. Check U102. H10 (C130) pins for wave form : CP127

NO → Replace Handsfree Mic.





6.2.5 Hook Switch not working

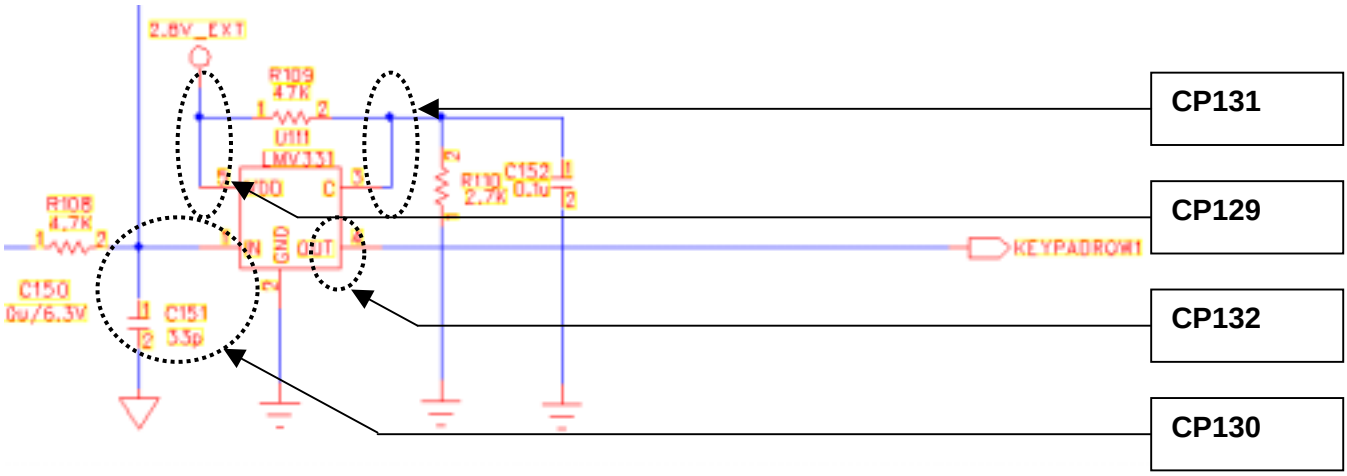
1. Check to see if U111.5 pin is 2.8V : CP129
2. Check to see if U111.1 pin is 0V during pressing Hook Switch : CP130
3. Check to see if U111.3 pin is around 0.3V : CP131

   NO → Check that R109 and R110 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it
4. Check to see if U111.4 pin is around 0V, when you press Hook Switch : CP132

   NO→ Check that U111 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it



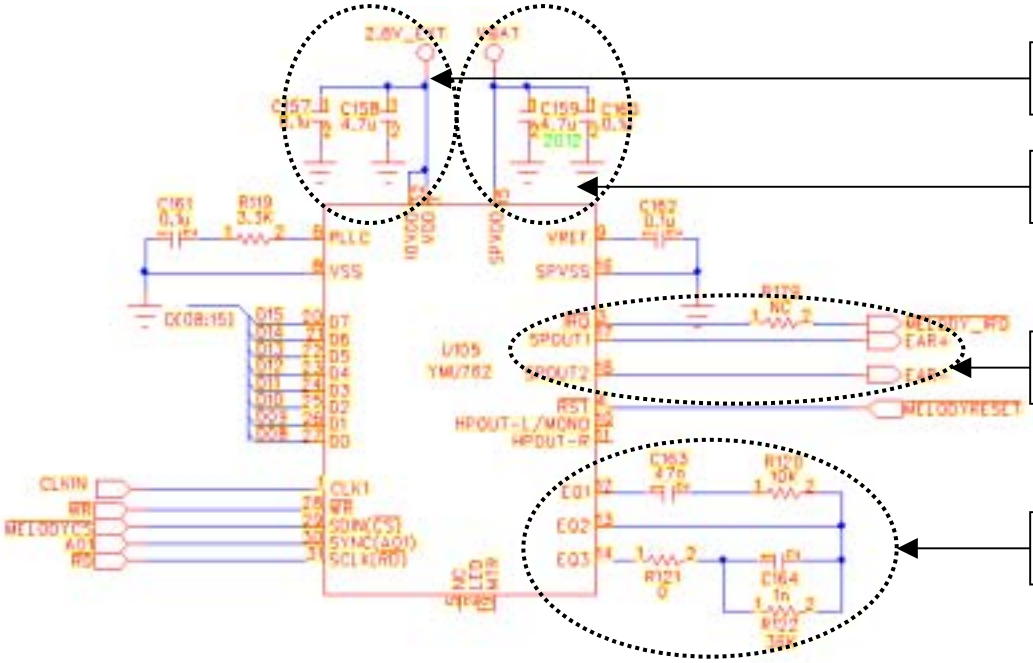
6.2.6 Melody not ringing

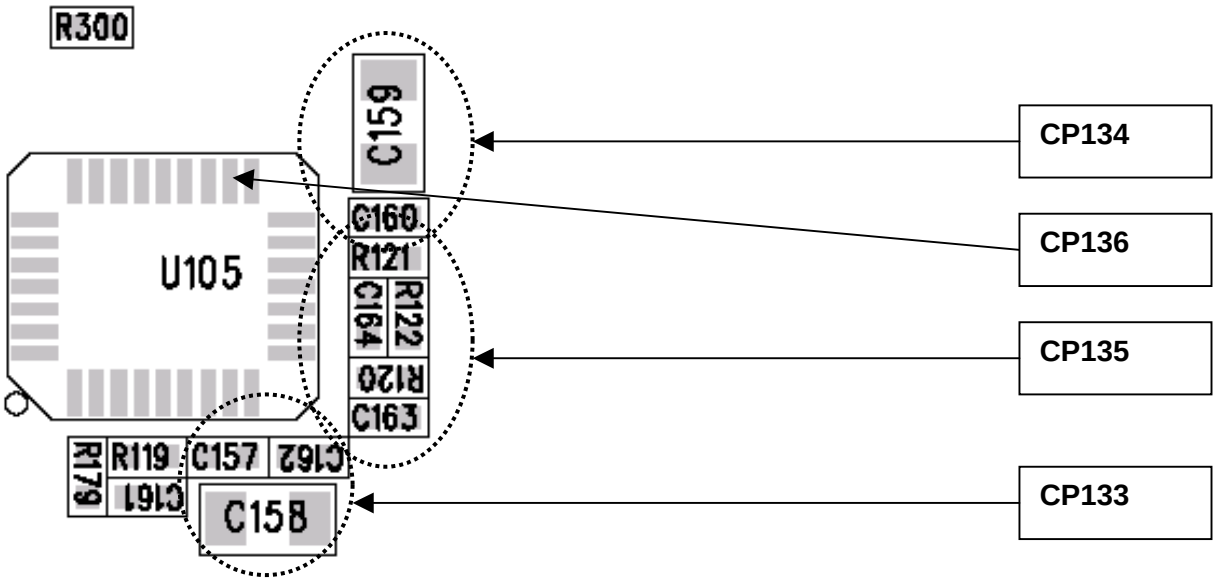
1. Check to see if U105.32, 7 is 2.8V : CP133
2. Check to see if U105.15 is Vbat : CP134
3. Check U105.12, 13, and 14 pin for waveform : CP135

   NO → Check that C163, R120, C164, R121 and R122 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it
4. Check SPK. SPOUT1 and SPOUT2 for waveform : CP136

   NO → Replacd SPK





6.2.7 Vibrator not working

1. Check to see if Q105.1 pin is 2.8V (duty : 60%, 70Hz) : CP137

   NO → Check to see Q105 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

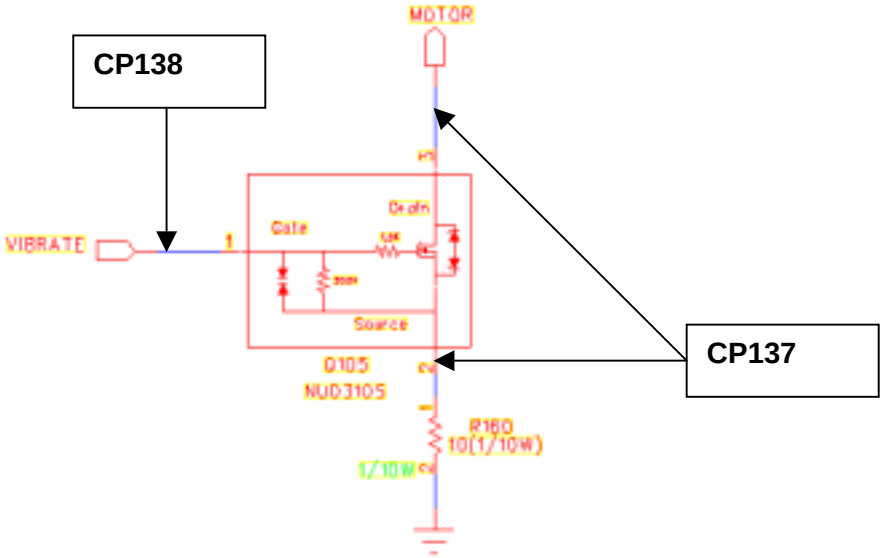
2. Check to see Q105.3 is same with battery power : CP138

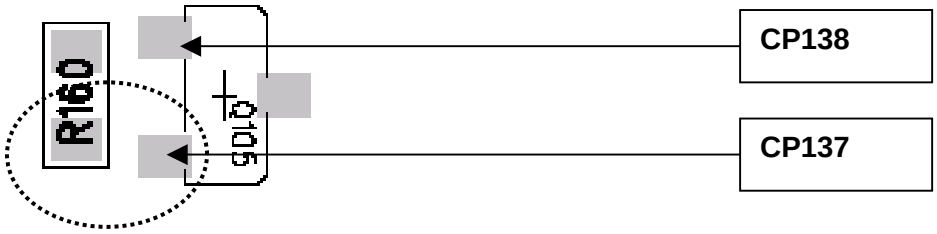
   NO → Check to see Q105 and R160 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it

3.Check to see Vibrator

   If you find out any defect, you replace it





6.3 SIM card part

6.3.1 SIM error

1. Check to see if J103.1 pin is around 2.85V : CP140

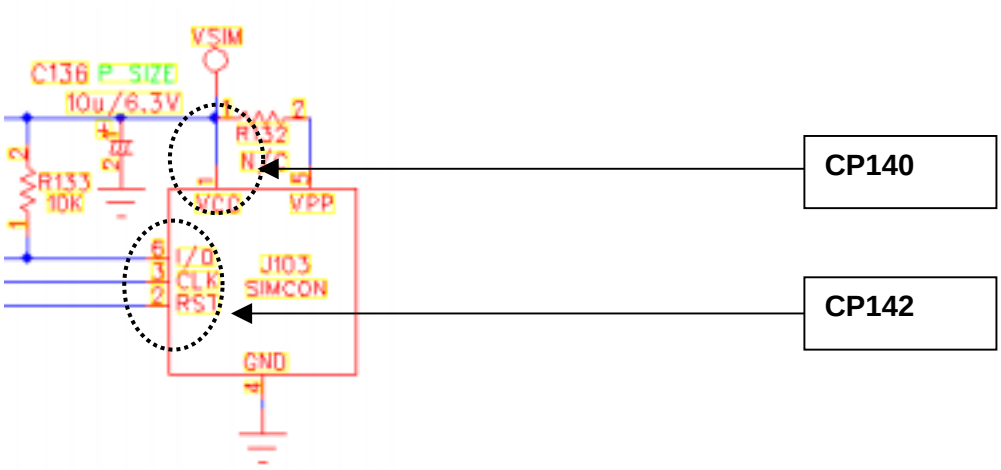
   NO → Check to see U103.18 pin cold solder, broken, short to the other PCB pattern or not : CP141

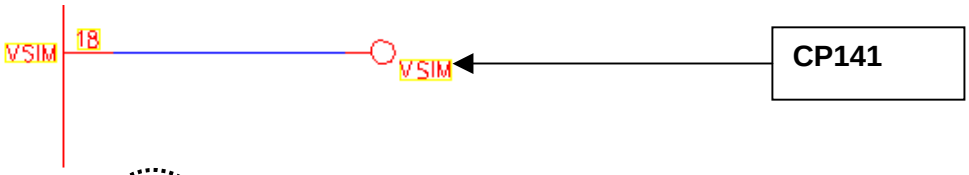
   If you find out any defect, you replace it

2.Check to see J103.2, 3, 6 for wave form : CP142

   NO → Check to see J103, R133 and C136 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it





6.4 Charger part

6.4.1 Charging error

Insert adaptor into I/O jack.

1. Check to see if U103.7 pin is 5.2V : CP143

   NO → Check to see J101.23, 24 pin and D116.1 cold solder, broken, short to the other PCB pattern or not : CP144

   If you find out any defect, you replace it

2. Check to see U103 No.14 pin is low (0V) : CP145

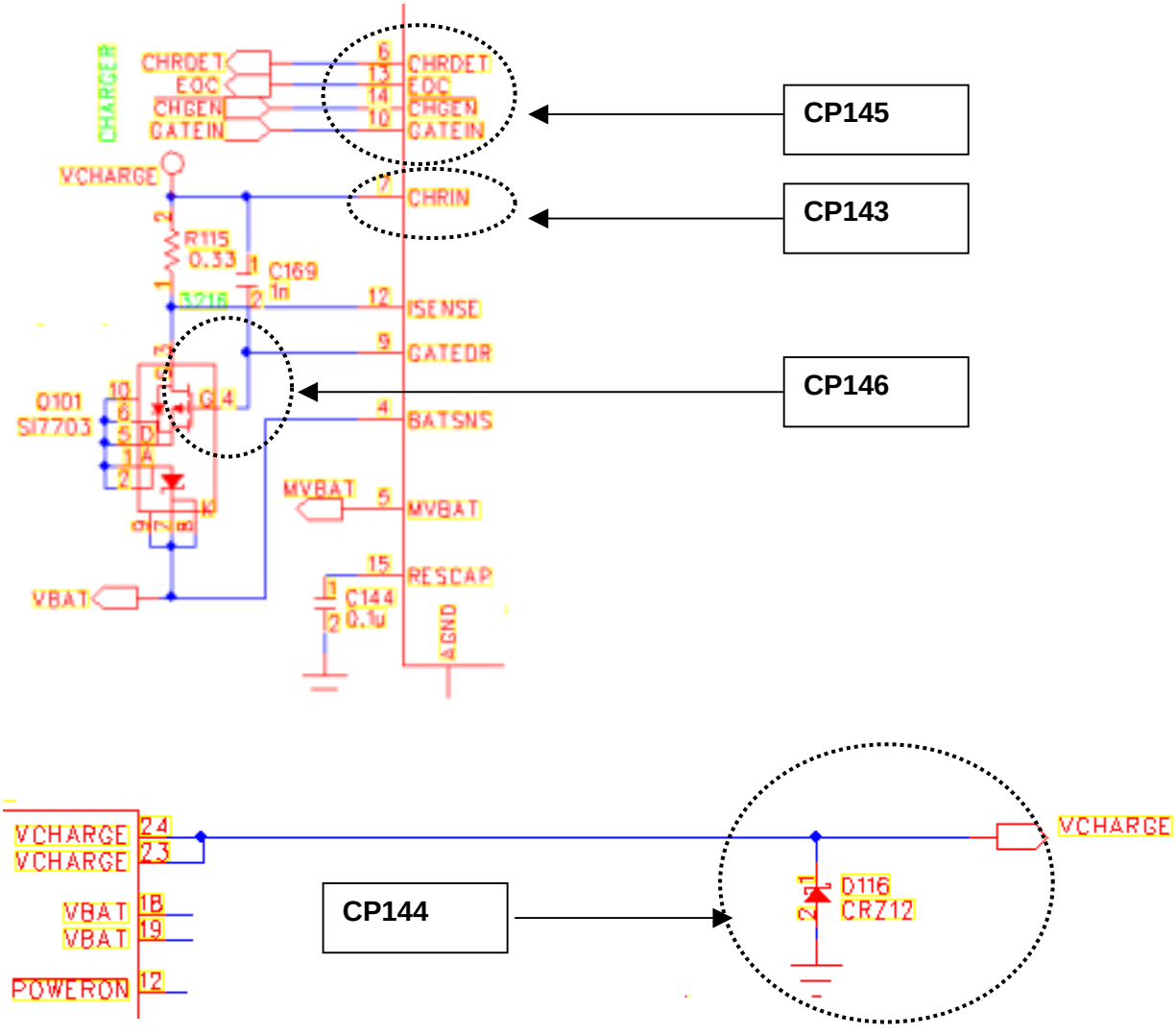
   NO → Check to see U103 cold solder, broken, short to the other PCB pattern or not

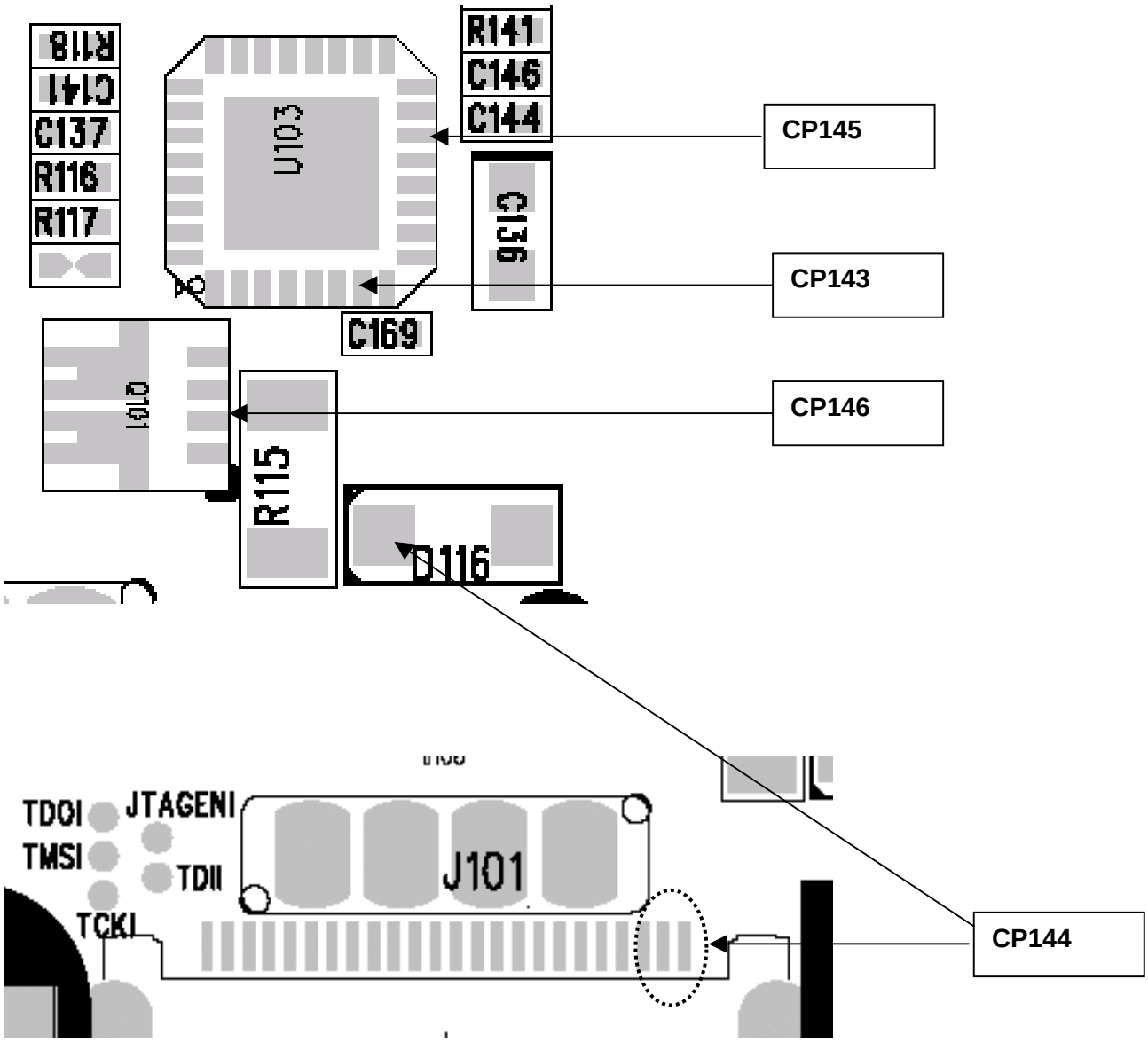
   If you find out any defect, you replace it

3. Check to see Q101 No.4 pin is 4.2V : CP146

   NO → Check to see Q101, R115, C169 cold solder, broken, short to the other PCB pattern or not

   If you find out any defect, you replace it




R118
C141
C137
R116
R117
U103
R141
C146
C144
C136
C169
CP145
CP143
CP146
C161
R115
D116
TDOI
JTAGENI
TMSI
TDII
TCKI
J101
CP144

6.5 RF Part

6.5.1 Test conditions

1. Test condition 1 : VBAT = 3.8V during all tests

2. Test condition 2 : Traffic channel :EGSM Band
   Tx mode
   Ch62
   Power Level : 13

3. Test condition 3 : Traffic channel : PCS Band
   Tx mode
   Ch661
   Power Level : 10

4. Test condition 4 : Traffic channel :GSM Band
   Rx mode
   Ch62
   Input power : -70dBm

5. Test condition 5 : Traffic channel : PCS Band
   Rx mode
   Ch661
   Input power : -70dBm

6. RF power values are measured using 50Ω coaxial cable.

6.5.2 Power Supply Check Point

Step	Test point	Typical Value	Condition	Checking Point
2-1	U907 Pin#1	3.8V	2, 3, 4, 5	Check route connection : VBAT
2-2	U907 Pin#5	2.8V	2, 3, 4, 5	Check route connection : VBAT
2-3	Z710 Pin#4	3.8V	2, 3, 4, 5	Check route connection : VBAT
2-4	Z710 Pin#5	2.8V	2, 3, 4, 5	Check route connection : VCC_RFCHIP

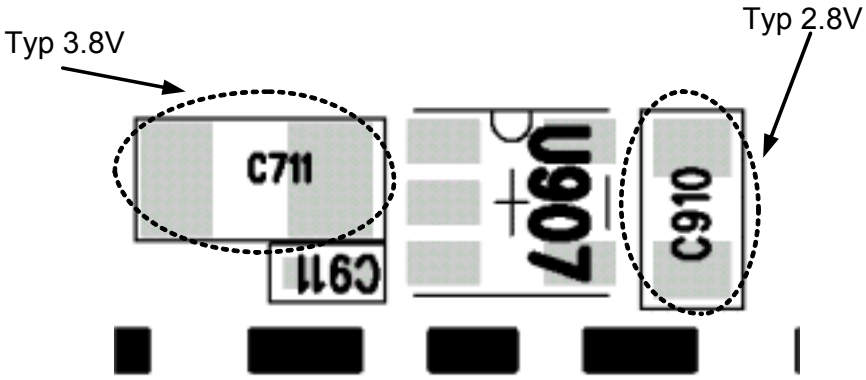


Fig.6-1 U907 Regulator Power Supply PCB Layout

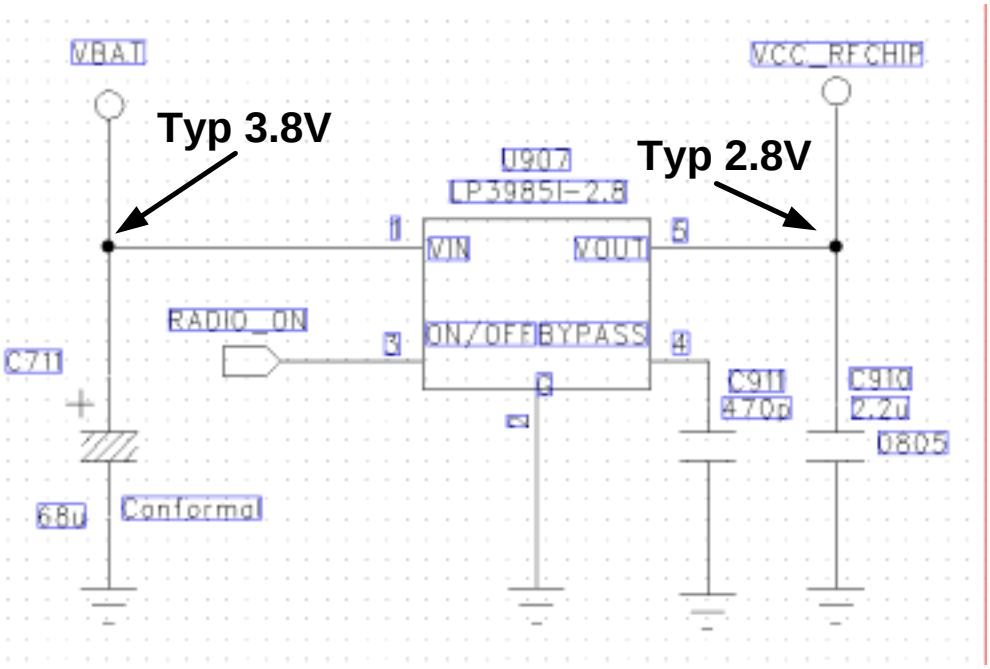


Fig.6-2 U907 Regulator Power Supply Schematic

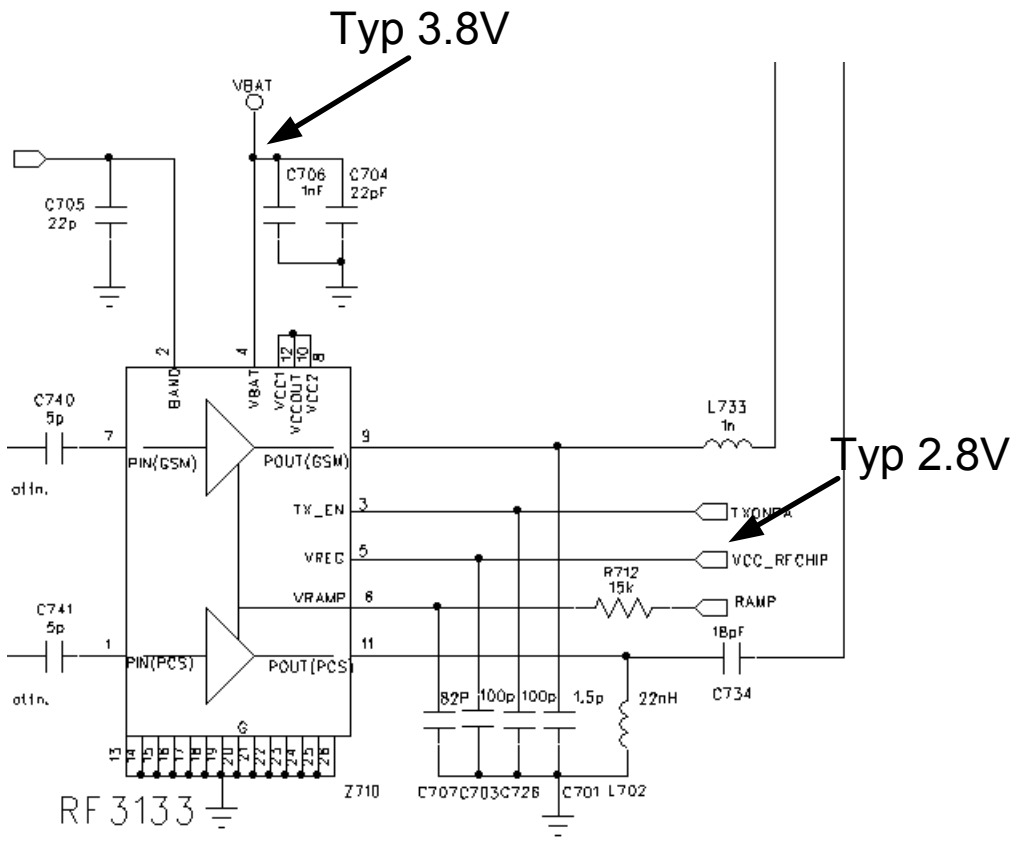


Fig.6-3 Z710 PAM's Power Check Point

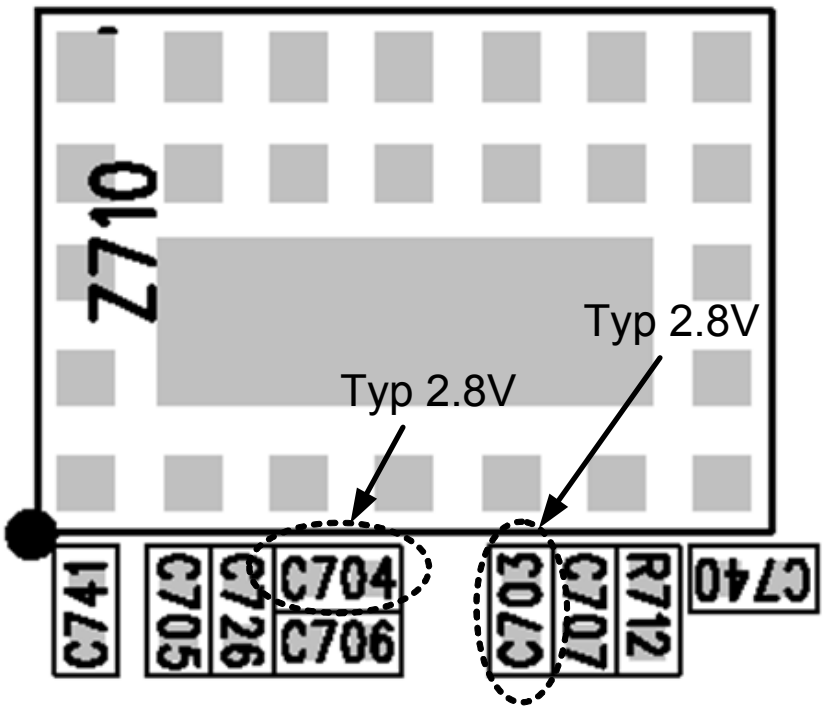


Fig.6-4 Z710 PAM's PCB Layout

6.5.3 Power Amplifier Module

- First check the Power Supply Check point following 6.5.2. Then you can trace the guideline of PAM as follows .

Step	Test point	Typical Value	Condition	Checking Point
3-1	Z710 Pin#3	Logic High	2, 3	Check route connection : TXEN
3-2	Z710 Pin#2	Logic High	3, 5	Check this pin 2, When Logic High, then PCS Mode. While Logic Low , GSM mode is operating.
		Logic Low	2, 4	

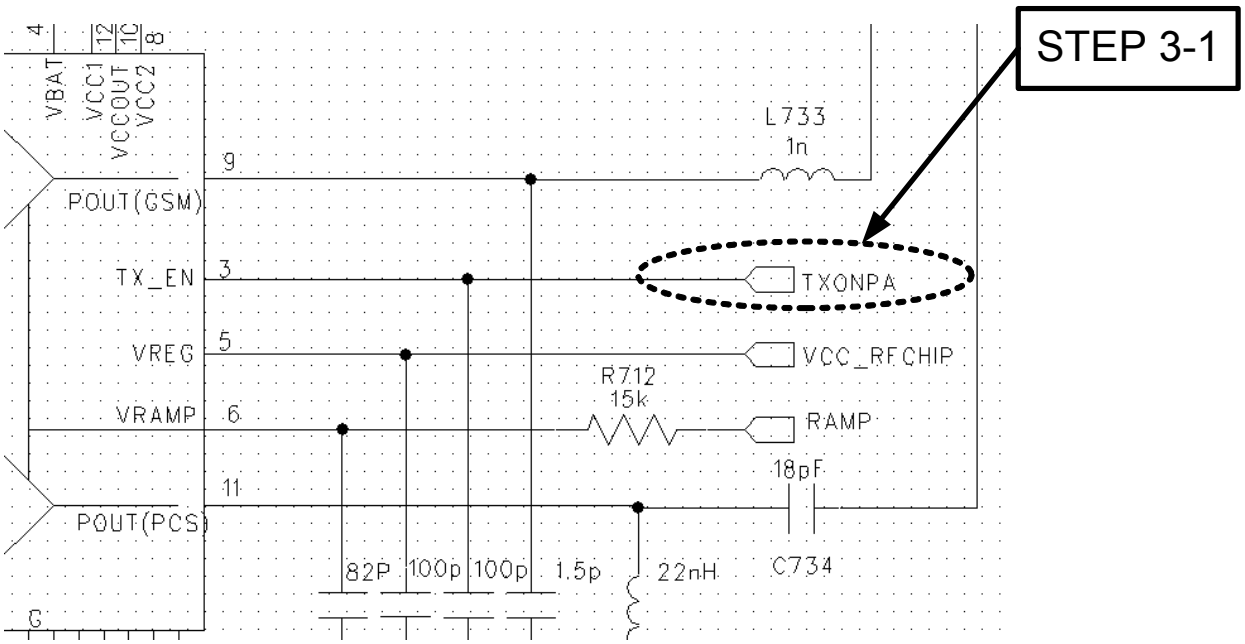


Fig.6-5. PAM TXONPA Test Point Circuit

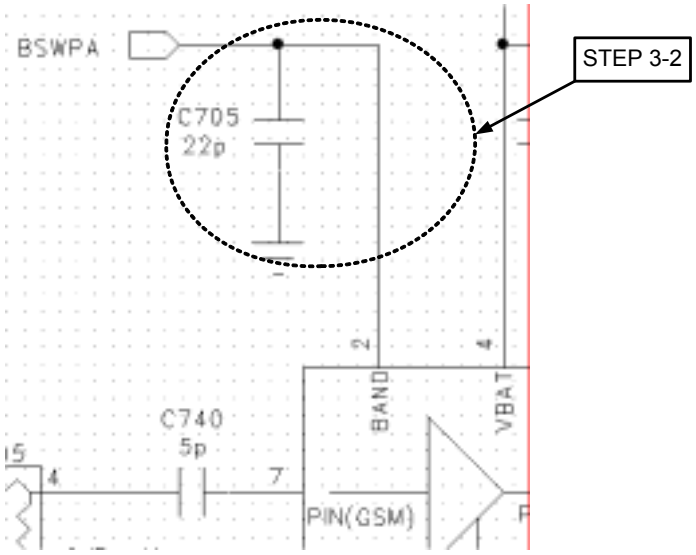


Fig.6-6. PAM PCSSEL Test Point Circuit

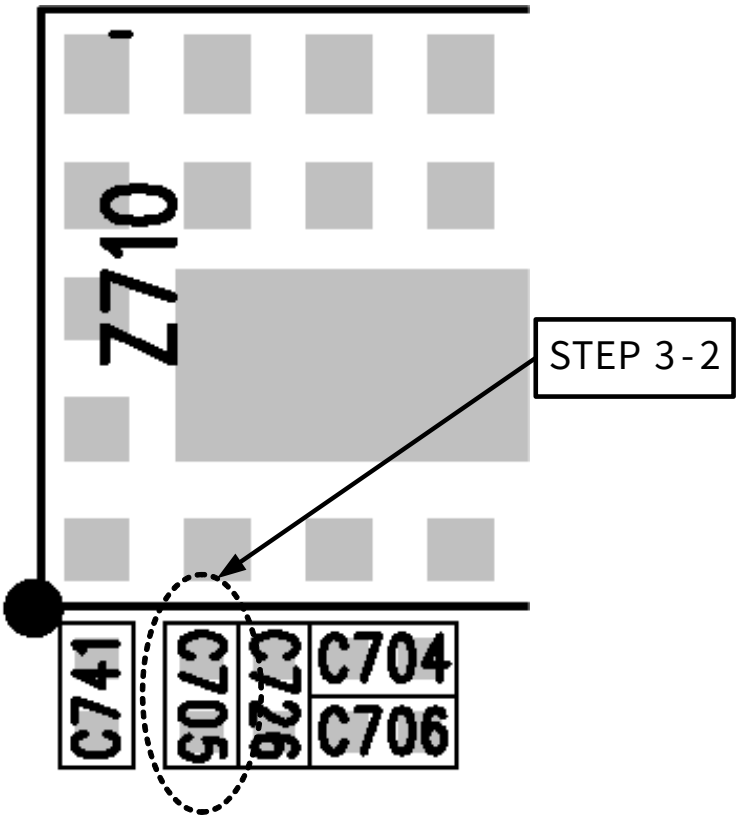


Fig.6-7. PAM TXONPA and PCSSEL Test Point on the PCB Layout

6.5.4 VCTCXO

Step	Test point	Typical Value	Condition	Reaction to Abnormality
4-1	V801 Pin#1	0.5V ~ 2.5V	2, 3, 4, 5	Check route connection : AFC
4-2	V801 Pin#4	2.8V	2, 3, 4, 5	Check route connection : VTCXO

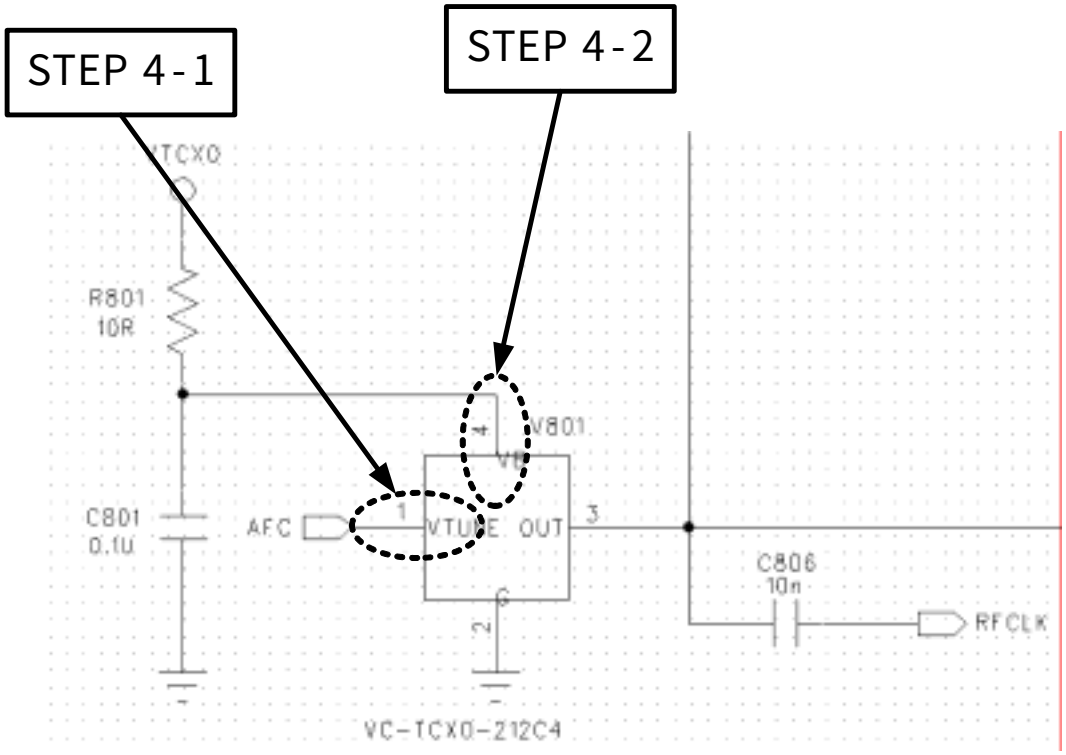


Fig.6-8. VCTCXO Check Point Circuit

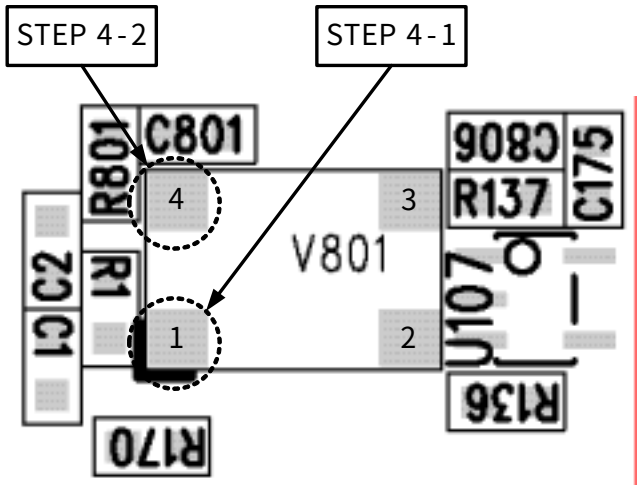


Fig.6-9. VCTCXO Check Point on the PCB Layout

6.5.5 Antenna Switch Module

Step	Test point	Typical Value	Condition	Check point
5-1	Z701 Pin#11	2.8V	2	When Pin#11 is Logic High and Pin#2 is Logic Low the mode is EGSM band. While Pin#2 is Logic High and Pin#11 is Logic Low the operating mode is PCS band.
5-2	Z701 Pin#2	2.8V	3	

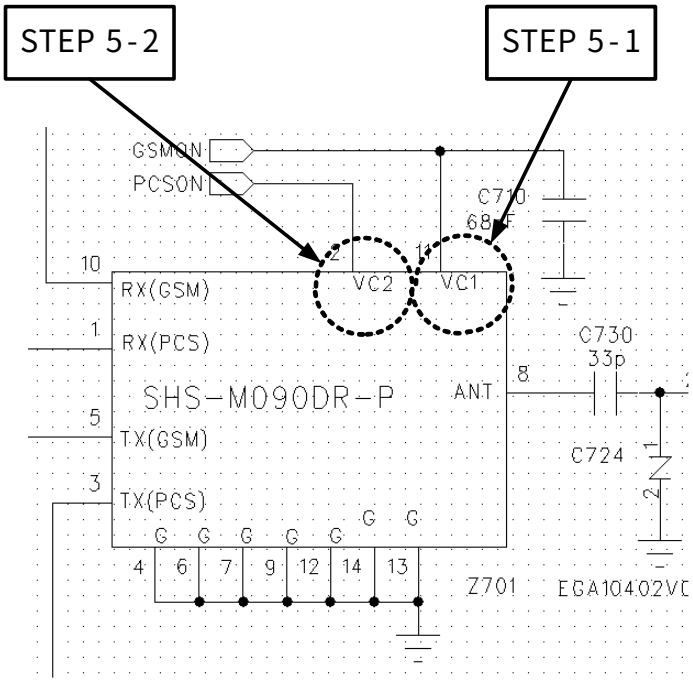


Fig. 6-10 Antenna Switch Module Circuit

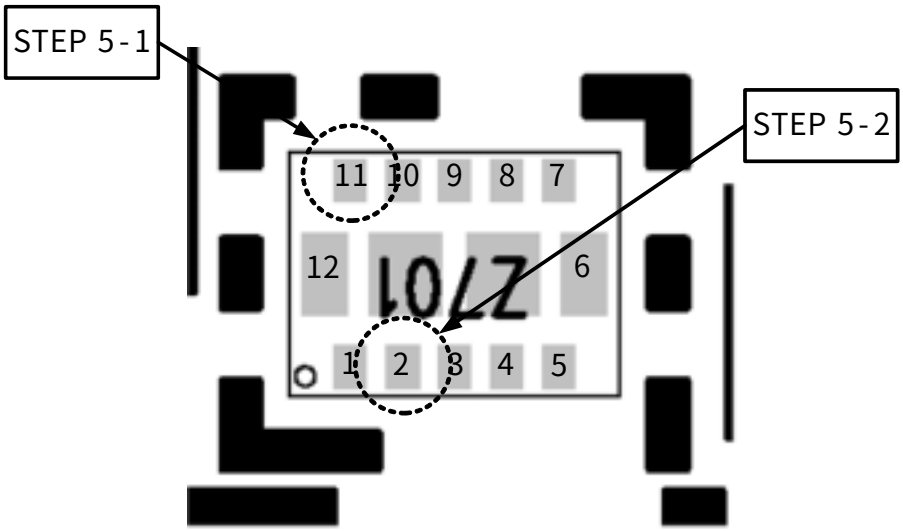


Fig. 6-11 Antenna Switch Module PCB Layout