M100 Circuit Operation Theory (BaseBand)

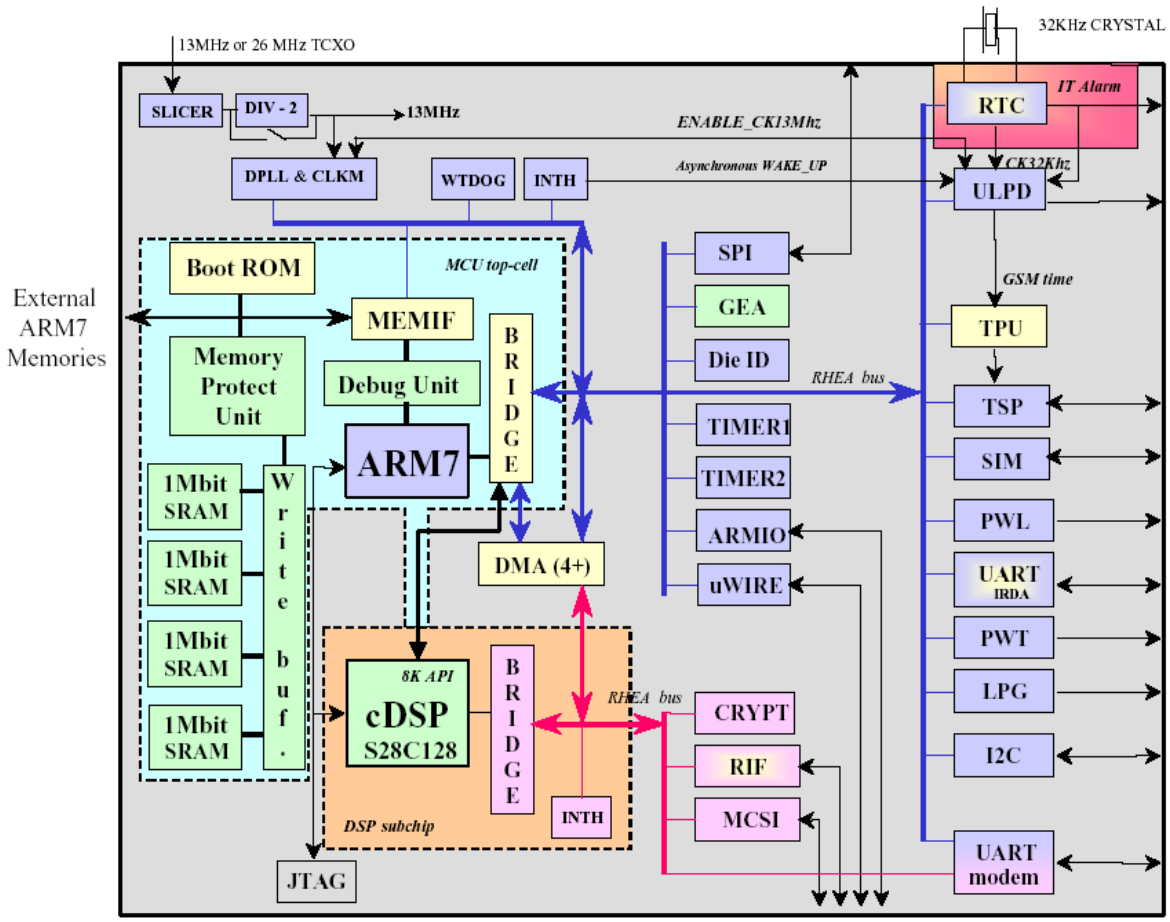
1. Introduction:

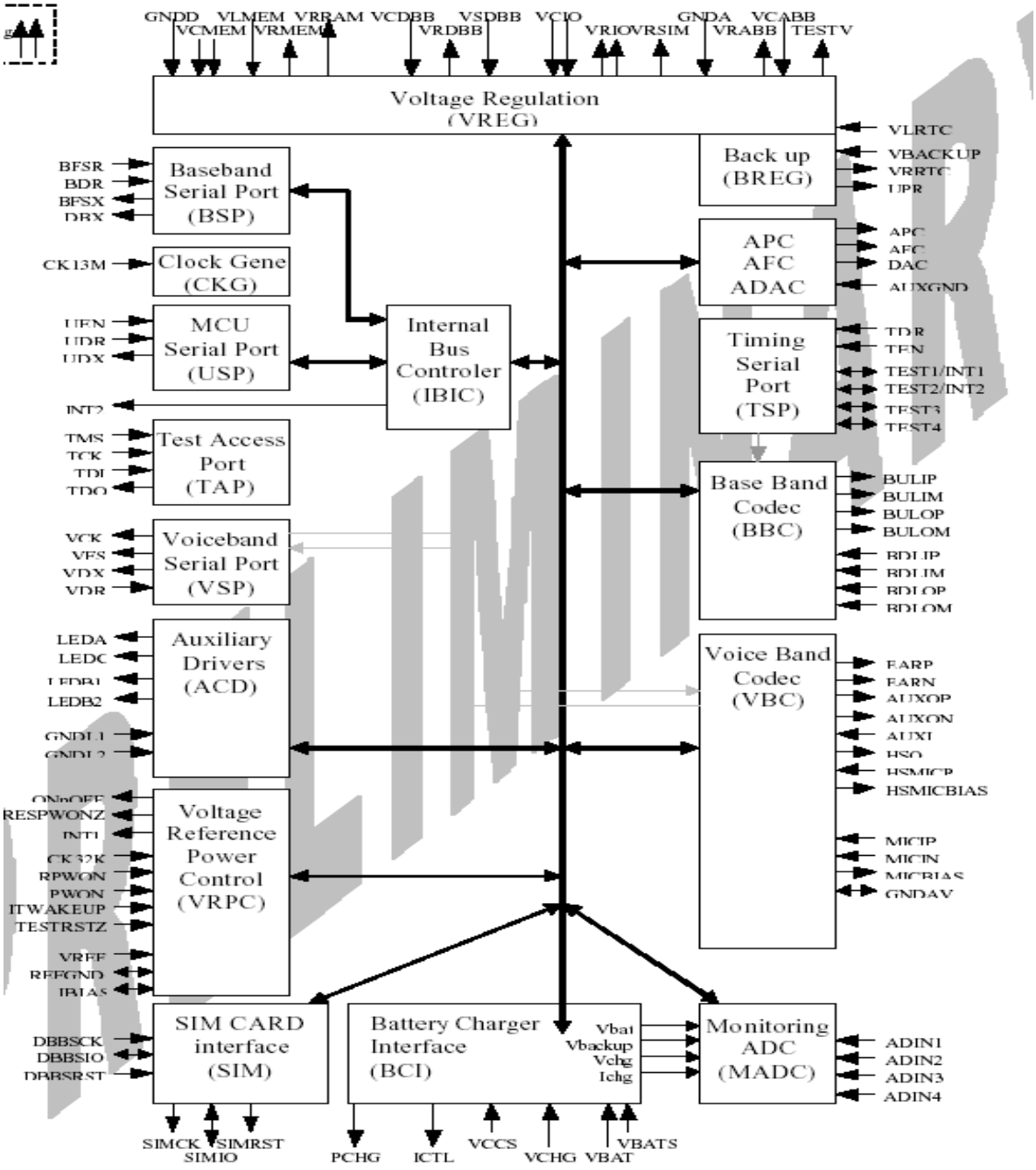
56F52 utilizes TI's chipsets (CALYPSO-Lite and IOTA) as base-band solution. Base-band is composed with two potions: Logic and Analog/Codec. CALYPSO-Lite is a GSM/GPRS digital base-band logic solution included microprocessor, DSP, and peripherals. IOTA is a combination of analog/codec solution and power management which contain base-band codec, voice-band codec, several voltage regulators and SIM level shifter etc. In addition, 56E11 integrates with other features such as LED backlight, color LCD display , vibration, melody tone and charging etc. The following sections will present the operation theory with circuitry and descriptions respectively.

2. Block Diagram

2.1 CALYPSO (HERCROM40)

2.2





3. Operation theory:

3.1 Calypso-Lite

CALYPSO-Lite (HERCROM400) is a chip implementing the digital base-band processor of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE) and an internal 2M-bit RAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.

Major functions of this chip are as follows:

3.1.1 Real Time Clock (RTC)

The RTC block is an embedded RTC module fed with an external 32.768KHz Crystal. Its basic functions are:

1. Time information (seconds/minutes/hours)
2. Calendar information (Day/Month/Year/ Day of the week) up to year 2099
3. Alarm function with interrupts (RTCINT is generated to wake up ABB)
4. 32KHz oscillator frequency gauging

3.1.2 Pulse Width Light (PWL)

This module allows the control of the backlight of LCD and keypad by employing a 4096 bit random sequence .In the 56E11, we use the LT/PWL function to turn on the keypad light LED.

3.1.3 MODEM-UART

This UART interface is compatible with the NS 16C750 device which is devoted to the connection to a MODEM through a standard wired interface. The module integrates two 64 words (9 and 11 bits) receive and transmit FIFOs which trigger levels are programmable. All modem operations are controllable either via a software interface or using hardware flow control signals. In 56F52 , we implement software flow control by only two signals: TXD0 and RXD0.

3.1.4 General Purposes I/O (GPIO)

Calypso-Lite provides 16 GPIOs configurable in read or write mode by internal registers. In 56F52, we utilize 9 of them as follows, others are used in the dual function mode or N/A:

IO0: N/A
IO1: N/A
IO2: Interrupt from Melody IC
IO3: N/A
IO4: N/A
IO5: N/A
IO6: Detection of earphone or download cable plugged-in
'H'：no accessory plugged-in
'L'： accessory plugged-in
IO7: Reset of external device such as melody IC and CSTN and DSC backend IC
IO8: N/A
IO9: Backlight of CSTN switch 'H'：ON ,'L'：OFF
IO10: N/A
IO11: N/A
IO12: N/A
IO13: N/A

IO14: SRAM high-byte enable

IO15: SRAM low-byte enable

3.1.5 Serial Port Interface (SPI)

The SPI is a full-duplex serial port configurable from 1 to 32 bits and provides 3 enable signals programmable either as positive or negative edge or level sensitive. This interface is working on 13MHz and is used for the GSM/GPRS baseband and voice A/D, D/A with IOTA

3.1.6 Memory Interface and internal Static RAM

For external memory device (Flash and SRAM), this interface performs read and write access with adaptation to the memory width. It also provides 6 chip-select signals corresponding each to an address range of 8 mega bytes. One of these chip-select is dedicated to the selection of an internal memory. In 56E11, we employ nCS0 (NROM_CS0) for external 64 Mbits Flash and nCS1 (NRAM_CS1) for external 16Mbits SRAM. A 2Mbit SRAM is embedded on the die and memory mapped on the chip-select nCS6 of the memory interface .The access cycle is guaranteed with 0 wait-state for any cycle frequency up to 39MHz. About others chip selects allocation are nCS3 (NLCDM_CS3) for LCDM driver and nCS4 for melody IC ..

3.1.7 SIM Interface

The Subscriber Identity Module interface will be fully compliant with the GSM 11.11 and ISO/IEC 7816-3 standards. Its external interface is 3 Volts only. 5 Volts adaptation will be based on external level shifters.

3.1.8 JTAG

In 56F52, JTAG is used for software debugging.

3.1.9 Time Serial Port (TSP)

The TPU is a real-time sequencer dedicated to the monitoring of GSM/GPRS baseband processing. The TSP is a peripheral of the TPU which includes both a serial port (32 bits) and a parallel interface. The serial port can be programmed by the TPU with a time accuracy of the quarter of GSM bit. The serial port is uni-directional (transmit only) when used with IOTA. The serial port provides 4 enable signals programmable either as positive or negative edge or level sensitive. This serial port is derived from 6.5MHz and used to control the real time GSM windows for the baseband codec and the windows for ADC conversion.

3.1.10 TSP Parallel interface (ACT)

The parallel interface allows control 13 external individual outputs and 1 internal signal with a time accuracy of the quarter of GSM bit. These parallel signals are mainly used to control the RF activity. In 56F52, we employ 5 of them to control RF activity.

TSPACT1: GSM_T/R

TSPACT2: DCS_T/R
TSPACT3: PCS_RX
TSPACT6: TX_ON
TSPACT9: Band Select
TSPACT10: Latch enable

3.1.11 Radio Interface (RIF)

The RIF (Radio Interface) Module is a buffered serial port derived from the BSP peripheral module of the defined for TMS320C5X. The external serial data transmission is supported by a full-duplex double-buffered serial port interface. The interface is used for transfer of baseband transmit and receive data and also to access all internal programmation registers of the device.

3.1.12 Miscellaneous:

Some important Baseband /RF interface signals are defined as follows:
CLKTCXO: 13MHz VTCXO Clock from RF circuit
TCXOEN: 13MHz VTCXO Clock Enable signal

3.2 IOTA

Together with a digital base-band device (Calypso-Lite), IOTA is part of a TI DSP solution intended for digital cellular telephone applications including GSM 900, DCS 1800 and PCS 1900 standards (dual band capability).
It includes a complete set of base-band functions to perform the interface and processing of voice signals, base-band in-phase (I) and quadrature (Q) signals which support single-slot and multi-slot mode, associated auxiliary RF control features, supply voltage regulation, battery charging control and switch ON/OFF system analysis. IOTA interfaces with the digital base-band device through a set of digital interfaces dedicated to the main functions of Calypso-Lite, a base-band serial port (BSP) and a voice-band serial port (VSP) to communicate with the DSP core (LEAD), a micro-controller serial port to communicate with the micro-controller core and a time serial port (TSP) to communicate with the time processing unit (TPU) for real time control.
IOTA also includes on chip voltage reference, under voltage detection and power-on reset circuits.

Major functions of this chip are as follows:

3.2.1 Baseband Codec (BBC)

The baseband codec includes a two-channel uplink path and a two-channel downlink path.
The baseband uplink path (BUL) modulates the bursts of data coming from the DSP via the baseband serial port (BSP) and to be transmitted at the antenna. Modulation is performed by a GMSK modulator.

The GMSK modulator implemented in digital technique generates In-phase (I) and Quadrature (Q) components, which are converted into analog base-band by two 10 bits DACs filters. It also includes secondary functions such as DC offset calibration and I/Q gain unbalance.
The baseband downlink path (BDL) converts the baseband analog I & Q components coming from the RF receiver into digital samples and filters these resulting signals through a digital FIR to isolate the desired data from the adjacent channels. During reception of burst I & Q digital data are sent to the DSP via the baseband serial port (BSP) at a rate of 270 KHz.

3.2.2 Automatic Frequency control (AFC)

The automatic frequency control function consists of a digital to analog converter optimized for high resolution DC conversion. Its purpose is to control the frequency of the GSM 13MHz oscillator to maintain mobile synchronization on the base station and allow proper transmission and demodulation.

3.2.3 Automatic Power Control (APC)

Purpose of the Automatic Power Control (APC) is to generate an envelope signal to control the power ramping up, ramping down and power level of the radio burst.
The APC structure is intended to support single slot and multi-slots transmission with smooth power transition when consecutive bursts are transmitted at different power level. It includes a DAC and a RAM in which the shape of the edges (ramp-up and ramp-down) of the envelope signals are stored digitally. This envelope signal is converted to analog by a 10 bits digital to analog converter. Timing of the APC is generated internally and depends of the real time signals coming from the TSP and the content of two registers which control the relative position of the envelope signal versus the modulated I & Q.

3.2.4 Time serial port (TSP)

Purpose of the time serial port is to control in real time the radio activation windows of IOTA which are BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration and BDL receive and the ADC conversion start.
These real time control signals are processed by the TPU of DBB and transmitted serially to ABB via the TSP, which consists in a very simple two pins serial port. One pin is an enable (TEN) the other one the data receive (TDR). The master clock CK13M divided by 2 (6.5MHz) is used as clock for this serial port.

3.2.5 Voice band Codec (VBC)

The VBC processes analog audio components in the uplink path and transmits this signal to DSP speech coder through the voice serial port (VSP). In the downlink path the VBC converts the digital samples of speech data received from the DSP via the voice serial port into analog audio signal. Additional functions such as programmable gain, volume control and side-tone are performed into the voice band codec.

3.2.6 Micro-controller serial port (USP)

The micro-controller serial port is a standard synchronous serial port. It consists in three terminals, data transmit (UDX), data receive (UDR) and port enable (UEN). The clock signal is 13MHz clock. The USP

receives and sends data in serial mode from and to the external micro-controller and in parallel mode from and to the internal GSM Baseband a Voice A/D D/A modules. The micro-controller serial port allow read and write access of all internal registers under the arbitration of the internal bus controller.

3.2.7 SIM card shifters (SIMS)

The SIM card digital interface in ABB insures the translation of logic levels between DBB and SIM card, for transmission of 3 different signals; a clock derived from a clock elaborated in DBB, to the SIM card (DBBSCK➔SIMCLK). a reset signal from DBB to the SIM card (DBBSRST➔SIMRST), and serial data from DBB to SIM card (DBBSIO➔SIMIO) and vice-vera.

The SIM card interface can be programmed to drive a 1.8V and 3 V SIM card

3.2.8 Voltage Regulation (VREG)

Linear regulation is performed by several low dropout (LDO) regulators to supply analog and digital baseband circuits.

(1) LDO VRDBB generates the supply voltage (1.85V, 1.5V,and 1.35V) for the digital core of DBB. In 56F52, it is programmed to 1.5V. This regulator takes power from the battery voltage
(2) LDO VRABB generates the supply voltage 2.8V for the analog function of ABB. It is supplied by the battery.
(3) LDO VRIO generates the supply voltage 2.8V for the digital core of ABB and digital I/O's of DBB and ABB. It is supplied from battery voltage.
(4) LDO VRMEM generates the supply voltages 2.8V for DBB memory interfaces I/O's.
(5) LDO VRRAM generates the supply voltages 2.8V for DBB memory interfaces I/O's
(6) LDO VRRTC generates the supply voltages (1.85,1.5, or 1.35V) and supply voltage 1.5V for the following block of DBB (real time clock and 32K oscillator). It's supplied by UPR
(7) LDO VRSIM generates the supply voltages (1.8V, 2.9V) for SIM card interface I/O's

3.2.9 Baseband Serial Port (BSP)

The BSP serial interface is used for both configuration of the GSM baseband and voice A/D D/A (read and write operation in the internal registers), and transmission of the radio data to the DSP during reception of a burst by the downlink part of the GSM baseband & voice A/D D/A. Four pins are used by the serial port: BFSR and BDR for receive, BFSX and BDX for transmit. BDX is the transmitted serial data output. BFSX is the transmit frame synchronization and is used to initiate the transfer of the transmit data. BDR is the received serial input. BFSR is the receive frame synchronization and is used to initiate the reception data.

3.2.10 Battery charger Interface (BCI)

The main function of the ABB charger interface is the charging control of either a 1-cell Li-ion Battery or 3-serie Ni-MH cell batteries with the support of the micro-controller. The battery monitoring uses the 10 bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage. The magnitude of the charging current is set by the

10 bits of a programming register converted by an 10 bit Digital to Analog Converter, whose output sets the reference input of the charging current control loop. The battery charger interface performs also some auxiliary functions. They are battery pre-charge, battery trickle charge and back-up battery charge if it is rechargeable.

3.2.11 Monitoring ADC (MADC)

The MADC consists in a 10-bit analog to digital converter combined with a nine inputs analog multiplexer. Out of the nine inputs five are available externally, the four remaining being dedicated to main battery voltage, back up battery voltage, charger voltage and charger current monitoring. On the five available externally three are standard inputs intended for battery temperature, battery type measurements.

3.2.12 Reference Voltage / Power on Control (VRPC)

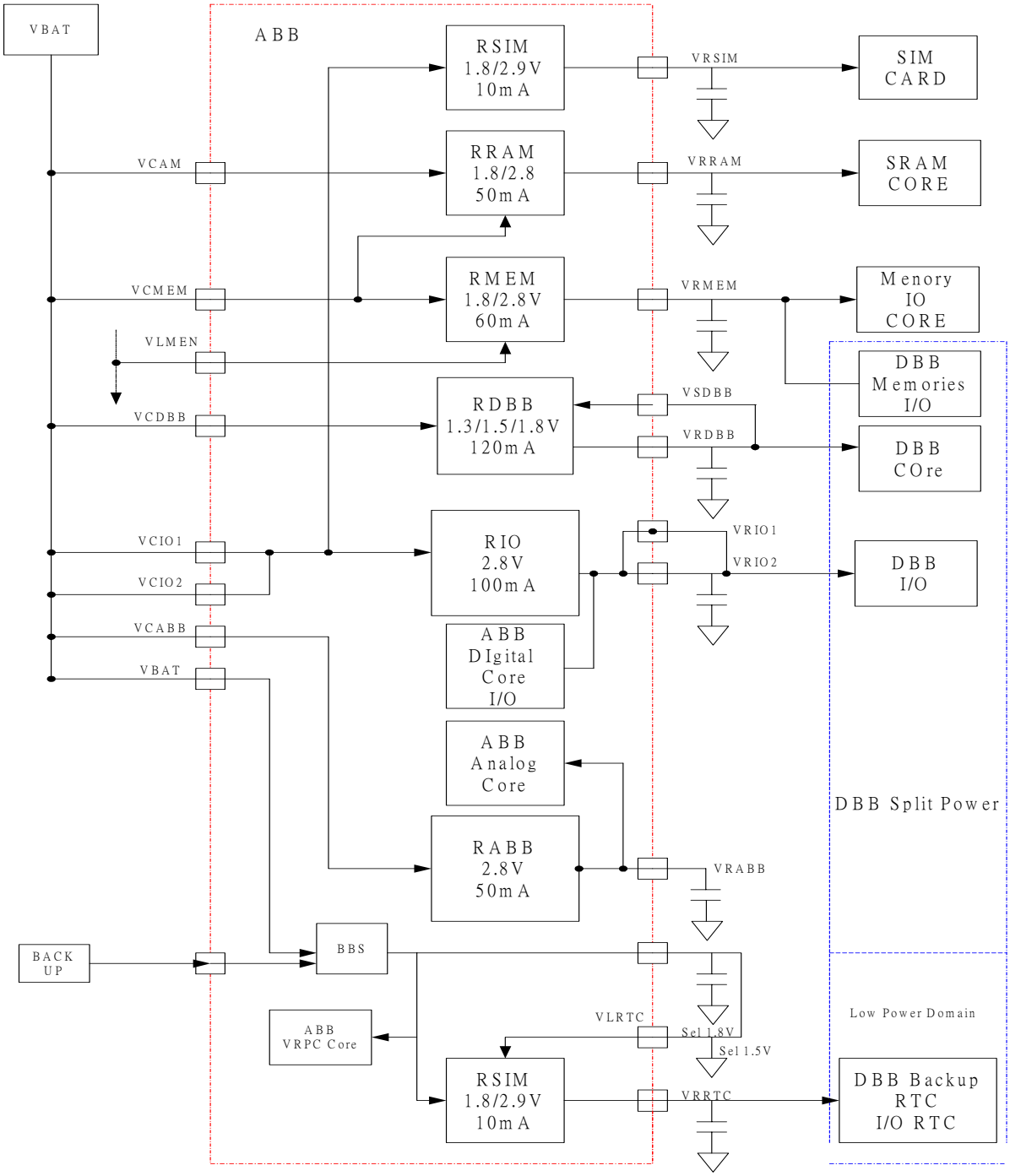
An integrated band-gap generates a reference voltage. This reference is available on an external pin for external filtering purpose only. This filtered reference is internally used for analog functions. The external resistor connected between pin IBIAS and GNDREF sets, from the band-gap voltage, the value of the bias currents of the analog functions. The VRPC block is in charge to control the Power ON, Power OFF, Switch On, and Switch OFF sequences. Even in Switch OFF state some blocks functions are performed. These “permanent” functions are functions, which insure the wake-up of the mobile such as ON/OFF button detection or charger detection. Interrupts are generated at power-down detection of the PWON button and when abnormal voltage conditions are detected.

3.2.13 Internal bus and interrupt controller (IBIC)

Read and write access to all internal registers being possible via both the BSP and USP, purpose of the internal bus controller is to arbitrate the access on the internal bus and to direct the read data to the proper serial port. During reception of a burst the internal bus controller assign the transmit part of the BSP to the base-band downlink to transfer the I & Q samples to the DSP.

This block also handles the internal interrupts generated by the MADC, BCI and VRPC blocks and generates the micro-controller interrupt signal INT2.

3.3 Power Supply diagram



3.3.1 Description:

The voltage regulators embedded in IOTA consists of seven sub blocks. Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators supply power to internal analog and digital

circuit, to DBB processor, and to external memory.

· LDO (VRDBB) is a programmable regulator that generates the supply voltages(1.8V,1.5V and 1.3V) for the core of the DBB processor. The main battery supplies VRDBB.

· LDO (VRIO) generate the supply voltage (2.8V) for the digital core and I/O of the TWL3014 device. The main battery supplies VRIO.

· LDO (VRMEM) is a programmable regulator that generates the supply voltages(2.8V and 1.8V) for external memories (typically flash memories) and DBB memory interface I/O. The main battery supplies VRMEM.

· LDO(VRRAM) is a programmable regulator that generate the supply voltages(2.8V and 1.8V) the external memory (typically SRAM memories) and DBB memory interface I/Os. The main battery supplies VRRAM.

· LDO (VRABB) generates the supply voltage (2.8V) for the analog functions of the TWL 3014 devices. The main battery supplies VRABB.

· LDO (VRSIM) is a programmable regulator that generates the supply voltages (2.9V and 1.8V) SIM card and SIM card devices. The main battery supplies VRSIM.

· LDO (VRTC) is a programmable regulator that generate the supply voltage (1.8V.1.5Vand 1.3V) for real time clock and the 32-KHZ oscillator located in the DBB device during all modes. The main or backup battery supplies VRTC.

3.4 System power on/off Sequence

3.4.1 Power on mode

On the plug-in of the valid main battery or backup battery, an internal reset is generated (POR). After a power-on sequence, the TWL3014 device is in the BACKUP or OFF state.

When these conditions occur in the power on state, the hardware power on sequence starts:

1. Enable band-gap (VREF and IREF)
2. Check if Main Battery voltage is greater than 3.2V

3. Enable charge VRDBB-VRABB-VRMEM-VRRAM
4. Regulator OK.
5. ON_nOFF=1, ABB RSTz=1
6. NRESET pin is set from ‘L’ to ‘H’
7. 13MHz clock oscillator is enabled

3.4.2 Power off mode

This state is reached when there is not enough voltage in the main battery and backup battery or when both batteries are disconnected.

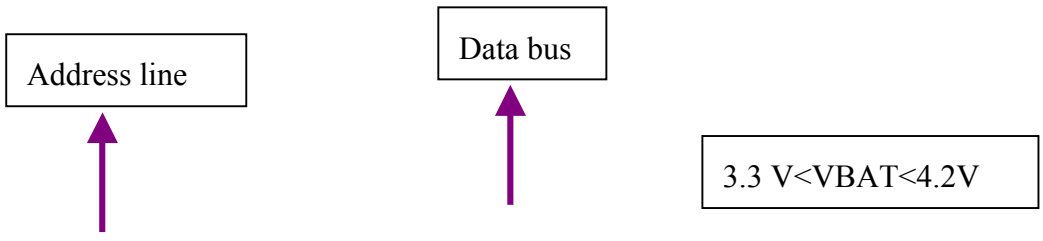
1. Send INT1
2. Start 5*T watchdog Timer , T= 32K period
3. ON_nOFF=0
4. ABB RSTz=0
5. Disable the LDO’s using MSKOFF content and the band-gap
6. “MBATLOW”=0

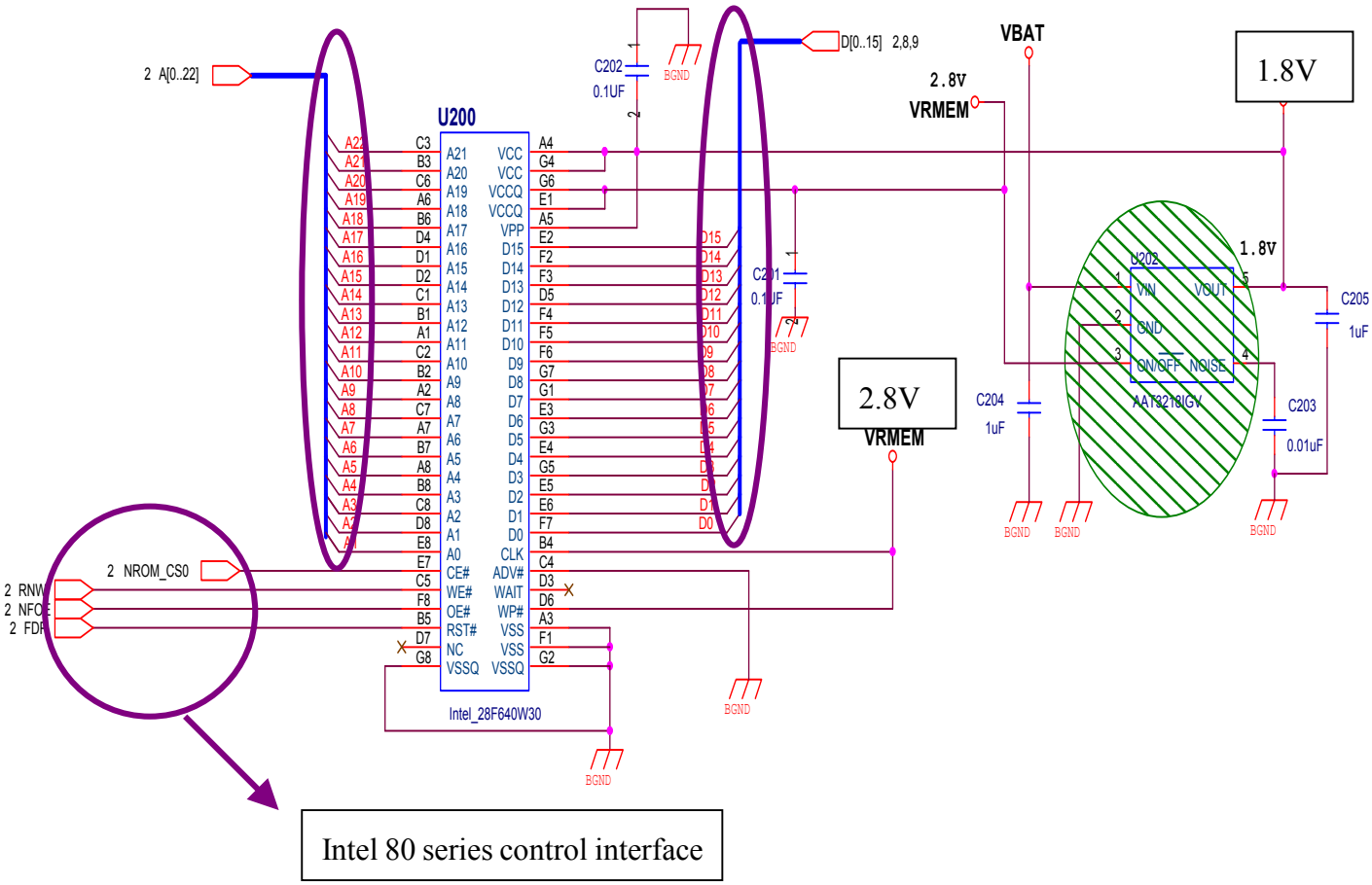
3.5 Memory circuit

3.5.1 Description:

Above diagrams show the memory circuit of 56F52 .One is 64-Mbit core 1.8 Volt , I/O 2.8Volt Intel Wireless Flash Memory W30 series, another is 16M bit 1-T SRAM

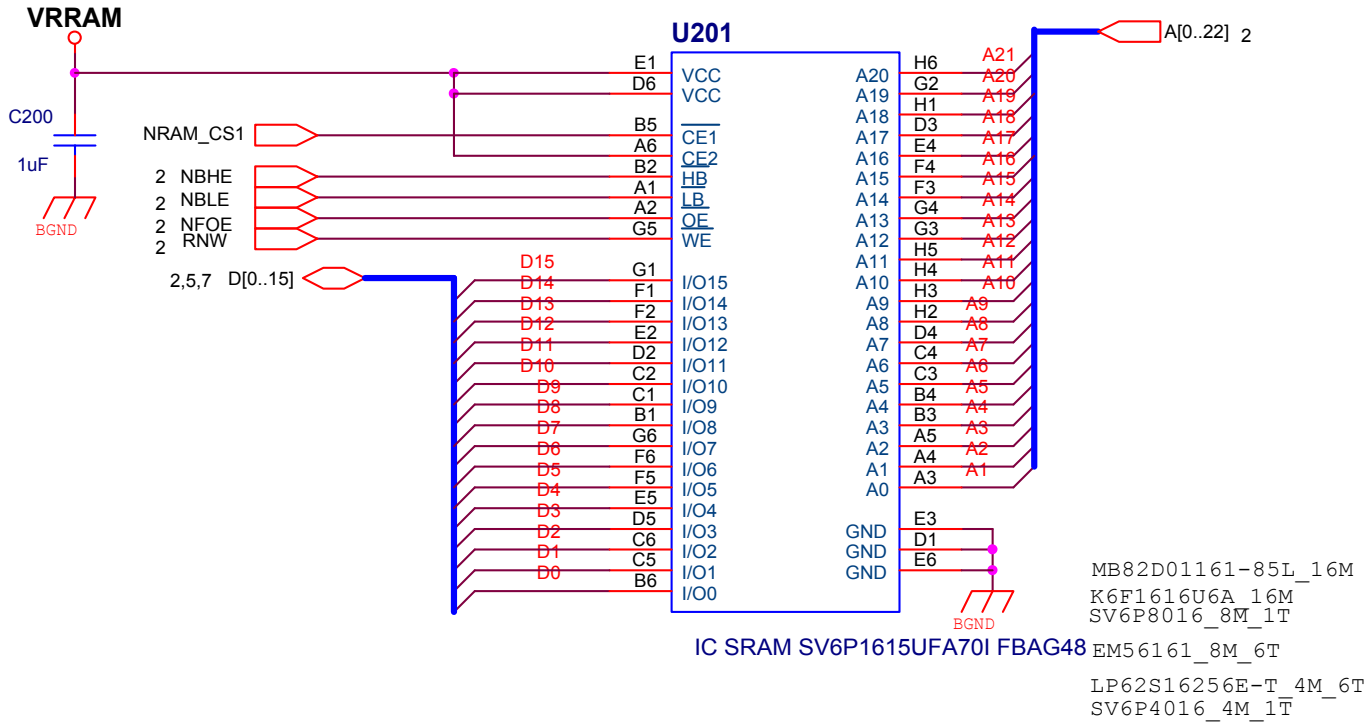
3.5.2 Schematic





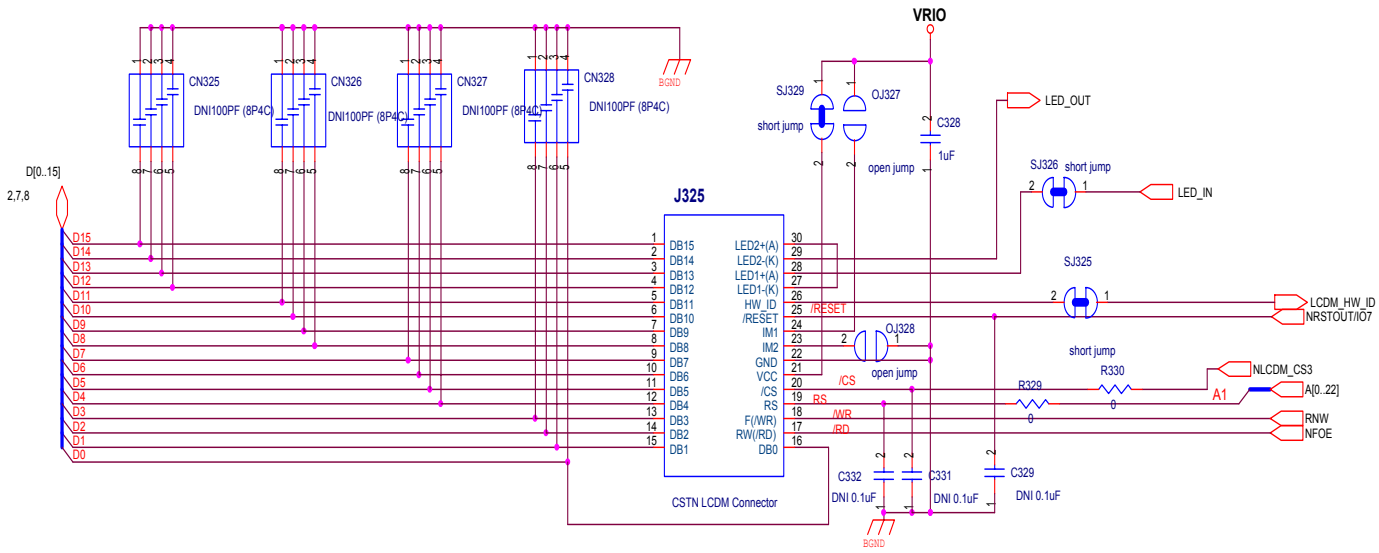
Above schematic is the Flash , below is the 1-T SRAM schematic

2.8V



3.6 LCD module (LCDM)

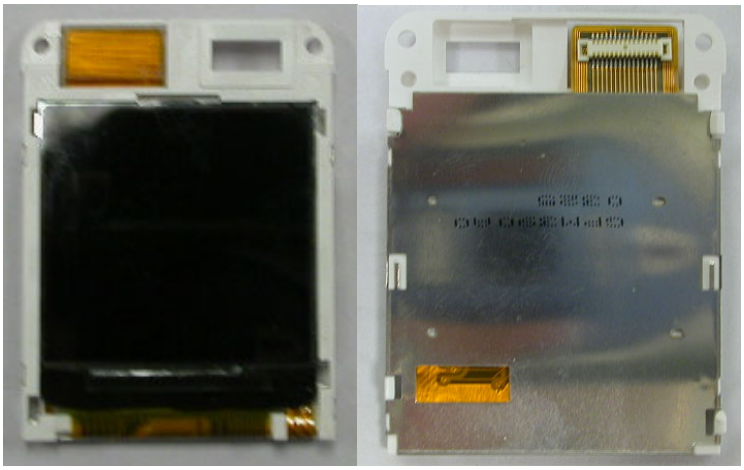
3.6.1 Connector between PCBA and LCDM



LCDM_HW_ID (ADIN1) voltage allocation vs LCDM vendor : (we use the ADIN1 (Iota) to detect the LCDM vendor)

```
272,        /* LCDM_Nanya       : 0.0 ~ 0.272V */
410,        /* Reserve             : 0.273 ~ 0.410V */
616,        /* Reserve             : 0.411 ~ 0.616V */
926,        /* Reserve             : 0.617 ~ 0.926V */
1390,       /* LCDM_GiantPlus   : 0.927 ~ 1.390V */
1718,       /* Reserve             : 1.391 ~ 1.718V */
```

3.6.2 LCM mechanical outline



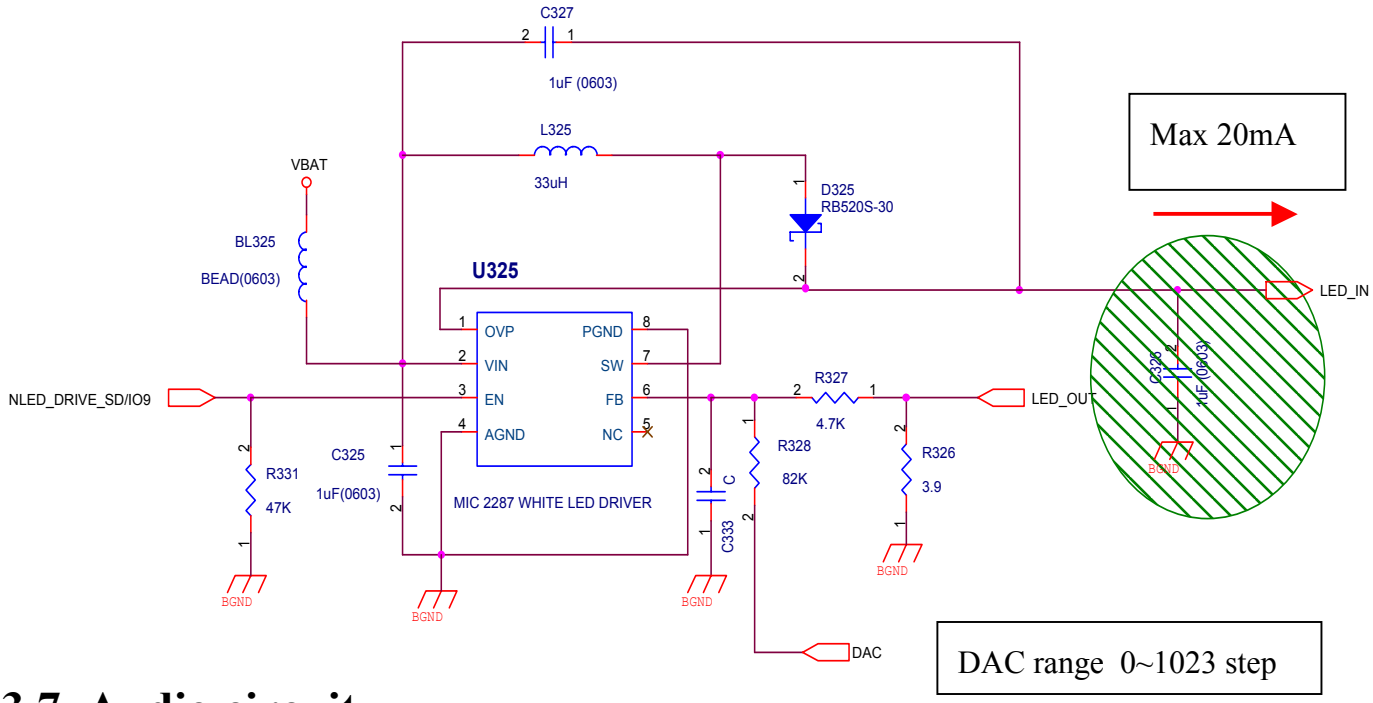
3.6.3 Description

This display module is a transmissive color STN (CSTN) Liquid crystal display (LCD) module of glass construction with a black background. The display has an internal transflector. The display consists of 128 (xRGB Stripe) x 128 pixel with 65K colors. bar connections to a flex foil accommodating components to drivers and the backlighting system. The backlighting system will consist of one light guide illumination both cells with a white backlight. Interconnection to the main board will be by a board to board connector.

This display module consists of:

- CSTN Cell with polarizers, COG
- Enhancement films (DBEF + 2*BREF)
- Mechanical support/carrier system with Magnesium frame
- One illumination system with 2 White LED's.
- Flexfoil with SMD component (include board to board connector for connection to the main part of the phone and between the module)

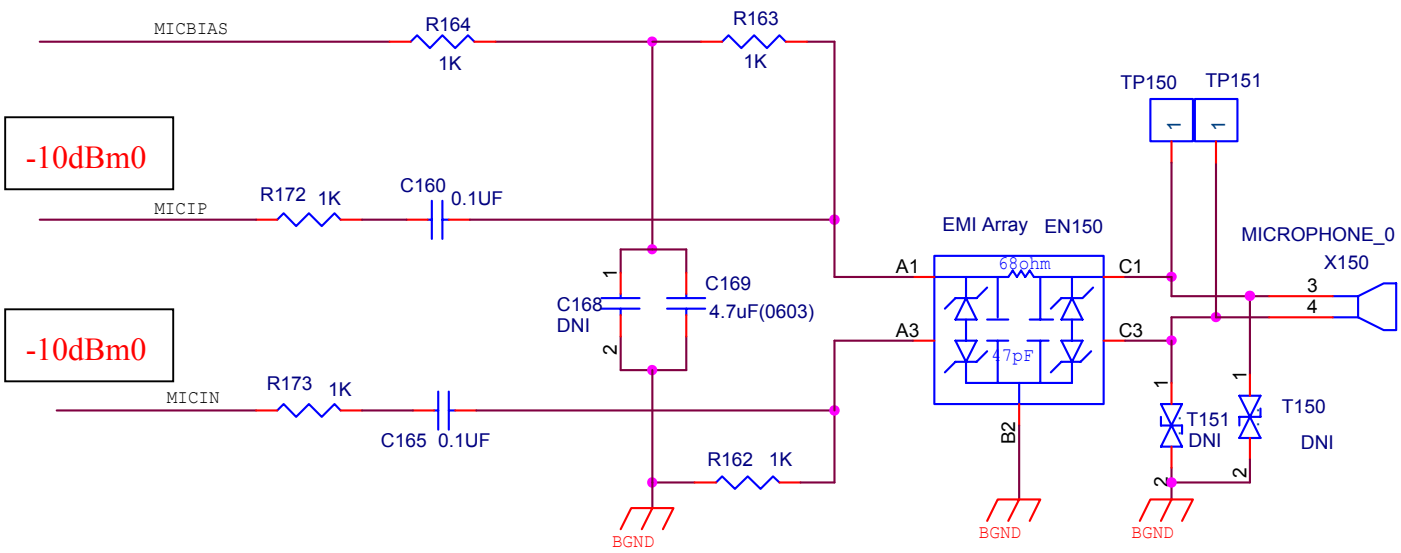
3.6.4 White LED driver schematic



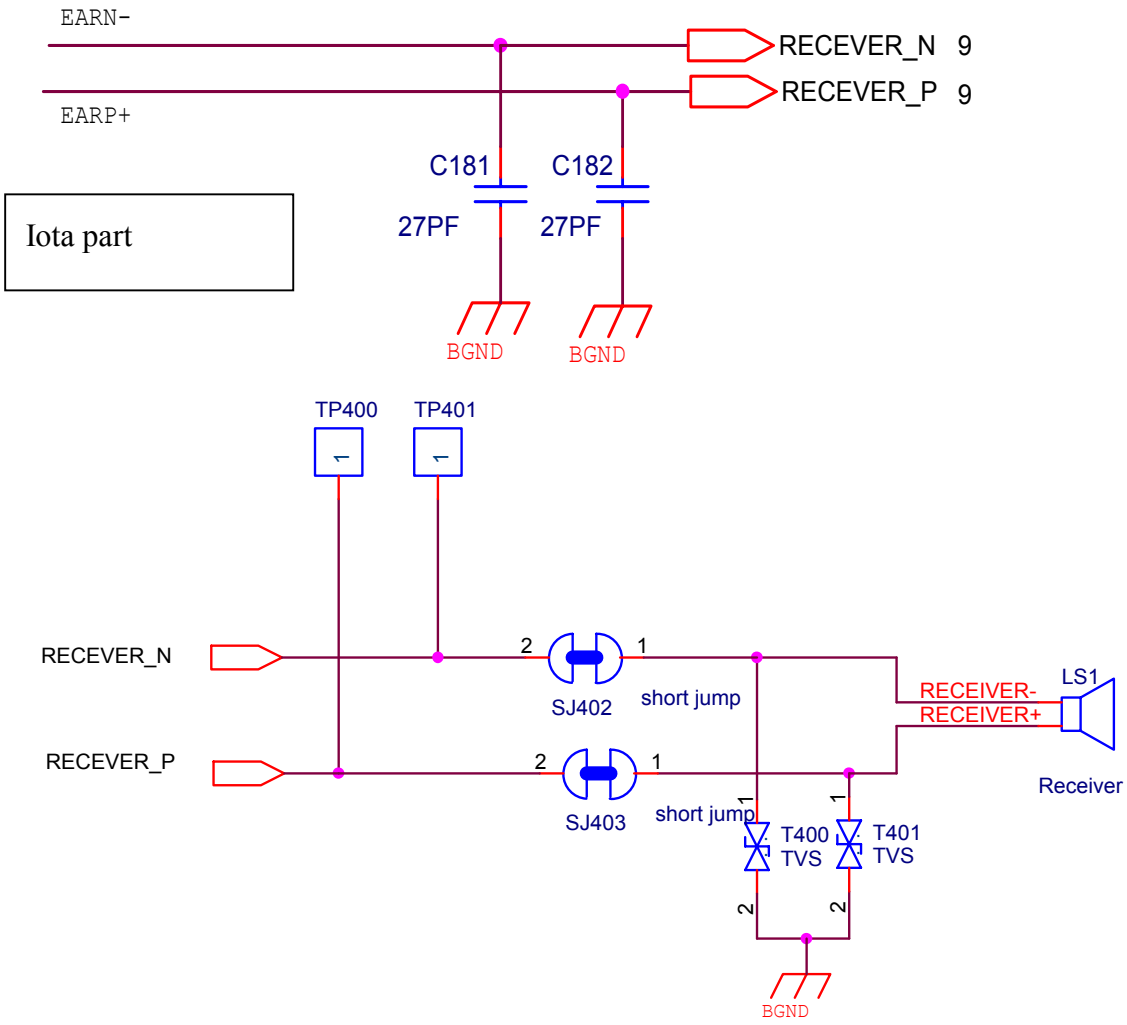
3.7 Audio circuit

3.7.1 Uplink path

2.0V



3.7.2 Downlink path



3.7.3 Description

The audio circuit is divided into two parts, uplink and downlink path.

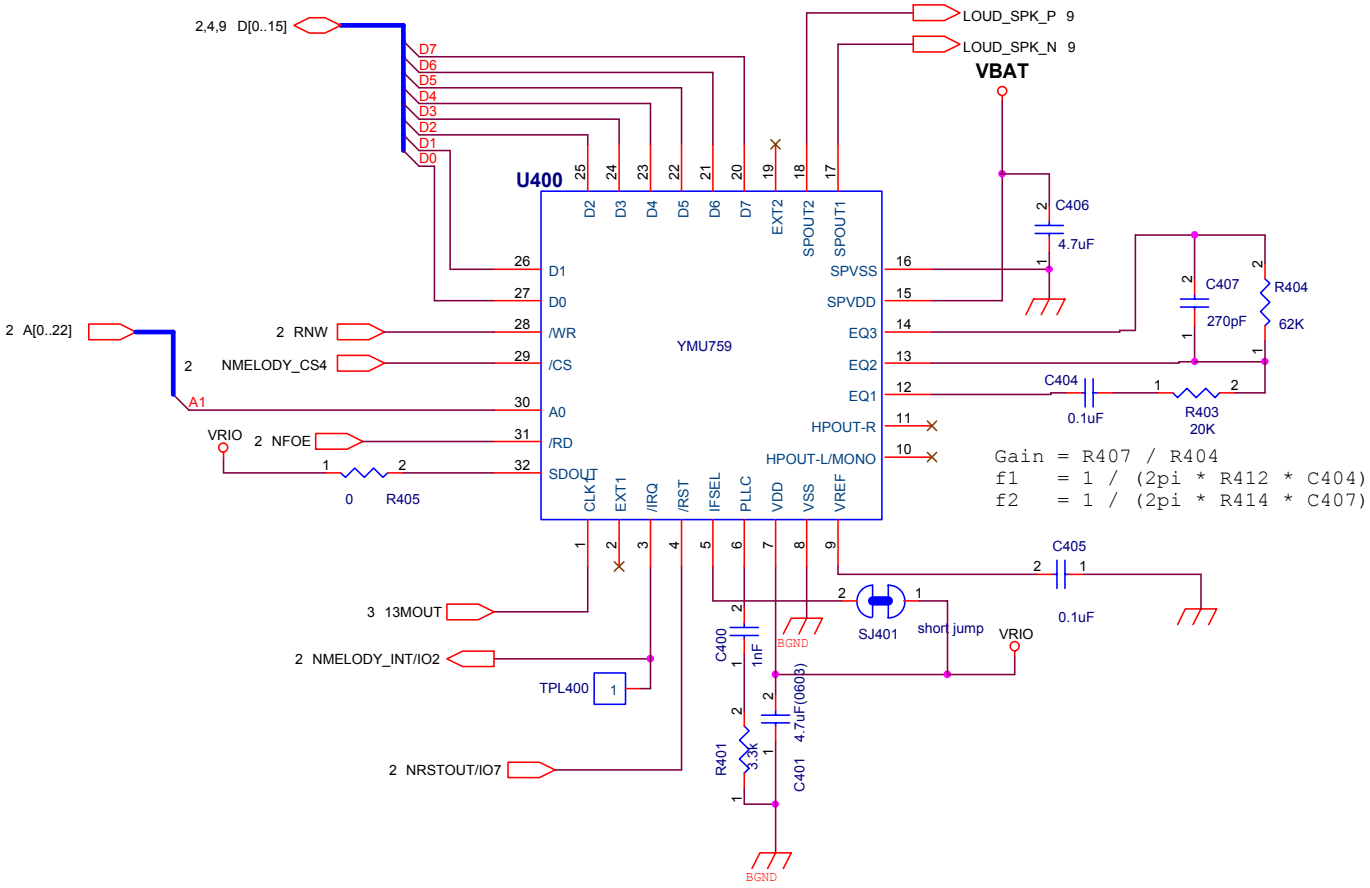
For uplink path, the analog voice signals are fed into IOTA from the microphone differential input and then transmitted to G2 DSP via the voice-band series port (VSP). After being modulated, the signals go through the uplink I/Q path to the RF transceiver and transmitted from the antenna.

The microphone circuit is biased from MICBIAS of IOTA. The bias circuit, R163, R164, R162 mainly provides the optimal operation point for the microphone signals, MICP and MICN. For downlink path, the signals received from the antenna are down-converted to I/Q signals and then transmitted to G2 DSP. After being demodulated, the signals are fed to IOTA via voice-band interface and then amplified to drive the receiver in the EARP and EARN .

3.8 Melody IC

3.8.1 Schematic

Yamaha 16 tone melody IC



3.8.2 Description:

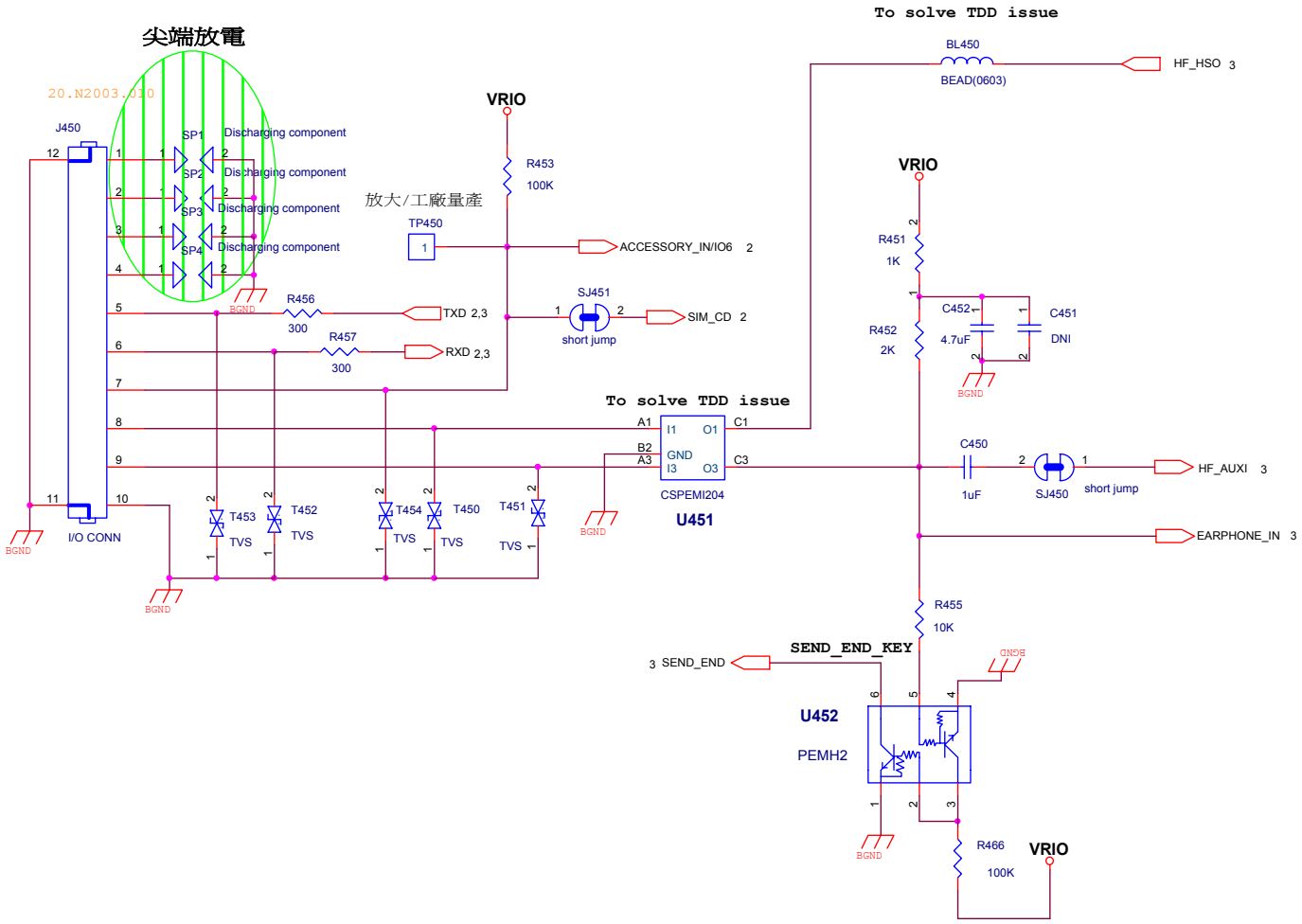
The Yamaha Melody IC (YMU759 MA2) mainly generate multi-tone for speaker. The main features are

1. Equipped with FM generator function and ADPCM playback function
2. Number of voice simultaneously generated
   When only 2-operator tone are used : up to 16 voices can be generated simultaneously
   When only 4-operator tone are used : up to 8 voices can be generated simultaneously
3. Built-in 4-bit 1ch ADPCM decoder, and supports two kinds of sampling frequency , 4kHz and 8kHz.
4. Built-in output 550mW (AVDD=3.6V) speaker amplifier
5. Built-in hardware sequencer
6. Built-in circuit for sound quality correcting equalizer
7. Supports stereophonic D/A converter
8. Provided with a stereophonic analog output terminal for headphone

9. 4 wire serial interface or 12 wire parallel interface can be selected
10. PLL is built-in to support master clock in 2MHz to 20MHz range
11. Support power down mode(Typical current: 1uA or less)
12. Power supply is divided into analog power supply for speaker amplifier and power supply for the others
    Analog power supply for speaker amplifer (SPVDD): 2.7V~4.5V (Typ 3.6V)
    Digital power supply for the others (VDD):2.7V~3.3V(Typ 3.0V)

3.9 10 Pins I/O connector

3.9.1 Schematic



Accessory type table :

0.8V < ADIN3 < 1.3V Define : Handsfree

0.45V < ADIN3 < 0.65V Define : DataCable

3.9.2 Description

The 10 Pins I/O connector circuit is used either for the headsfree or the data service. The SIM_CD will be pulled to low level when headsfree or data cable is plugged-in.

And the SEND_END_KEY function is that when handsfree work , user can send the call or end the call

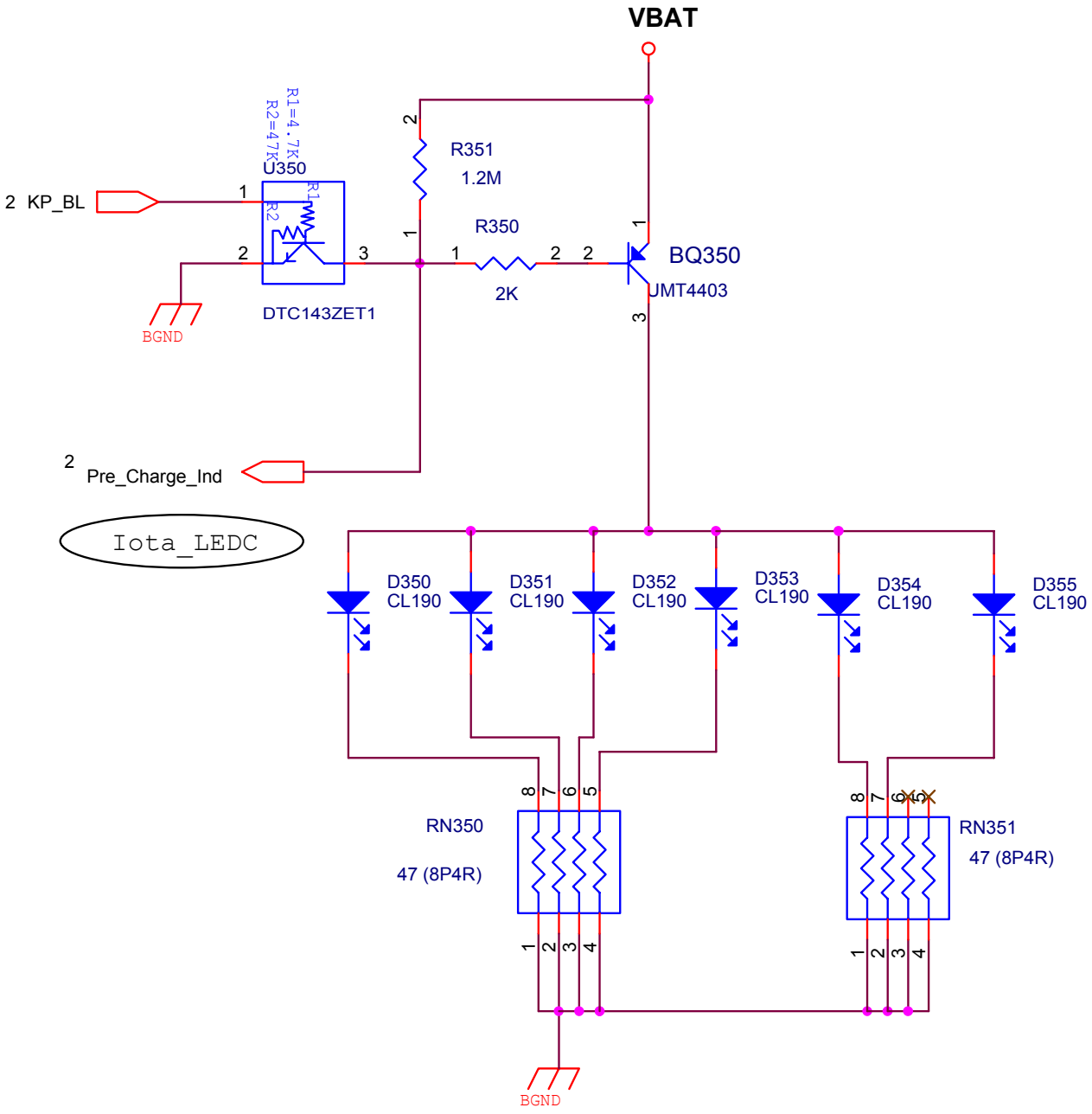
in the handsfree push bottom key. This function use the Keypad interrupt (G2-Lite) to generate the send-end function.

The HF_HSO is the handsfree speaker output and the HF_AUXI is the handsfree Micphone input for the Iota.

The EARPHONE _IN is connected to the Iota ADIN3 to judge accessory type (refer to the Accessory type table)

3.10 Keypad LED circuit

3.10.1 Schematic

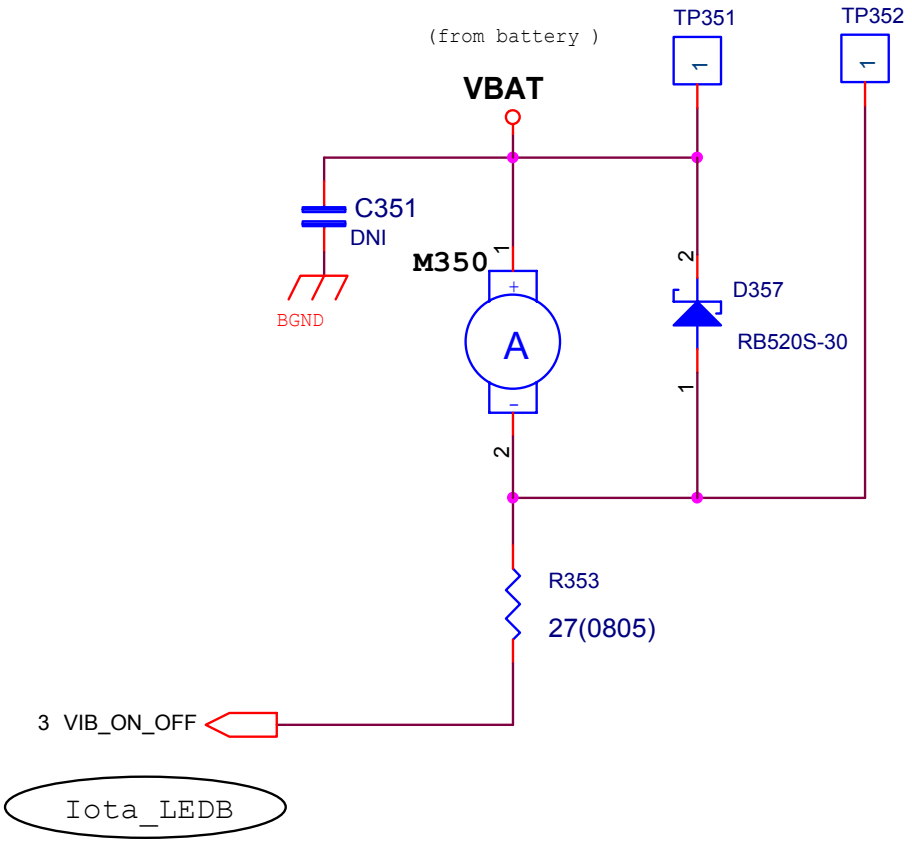


3.10.2 Description

56F52 employs six blue LEDs for keypad backlight and pre-charging indicator. The ON_OFF timing of (D350, D351, D352, D353, D354, D355) are controlled by U350 according to KP_BL = H (ON) /L (OFF). Under the default condition (VBAT=3.8V), the average current of one keypad backlight LED is about 6.25mA. So total current through LEDs is 40mA. If VBAT < 3.2V , as charger plug in handset ,Iota will do the pre-charging function and LEDC will L(ON) then these six LEDs will be turn on.

3.11 Vibrator

3.11.1 Schematic

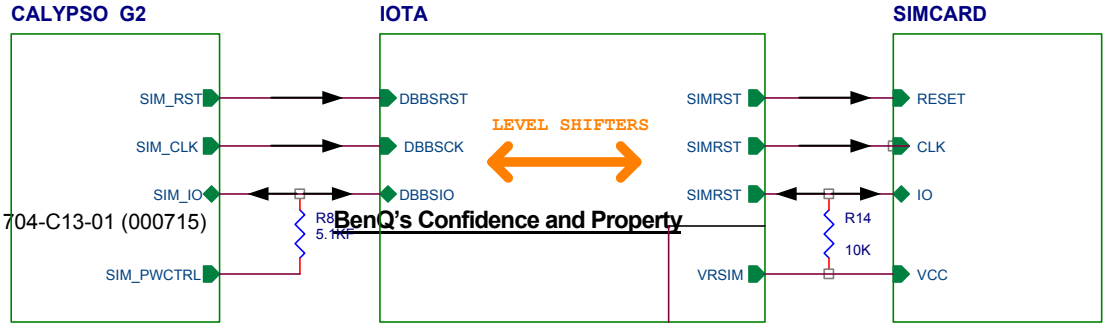


3.11.2 Description

Vibrator is enabled by LEDB control logic in IOTA. When the logic is set to ‘H’, the motor will activate. R353 are used to control operating current and D1 is used to reduce EMF. Under the condition of VBAT = 3.8V, the average drain current is around 66.5mA.

3.12 SIM Circuit

3.12.1 Schematic



BenQ's Confidence and Property

3.13.2 Description

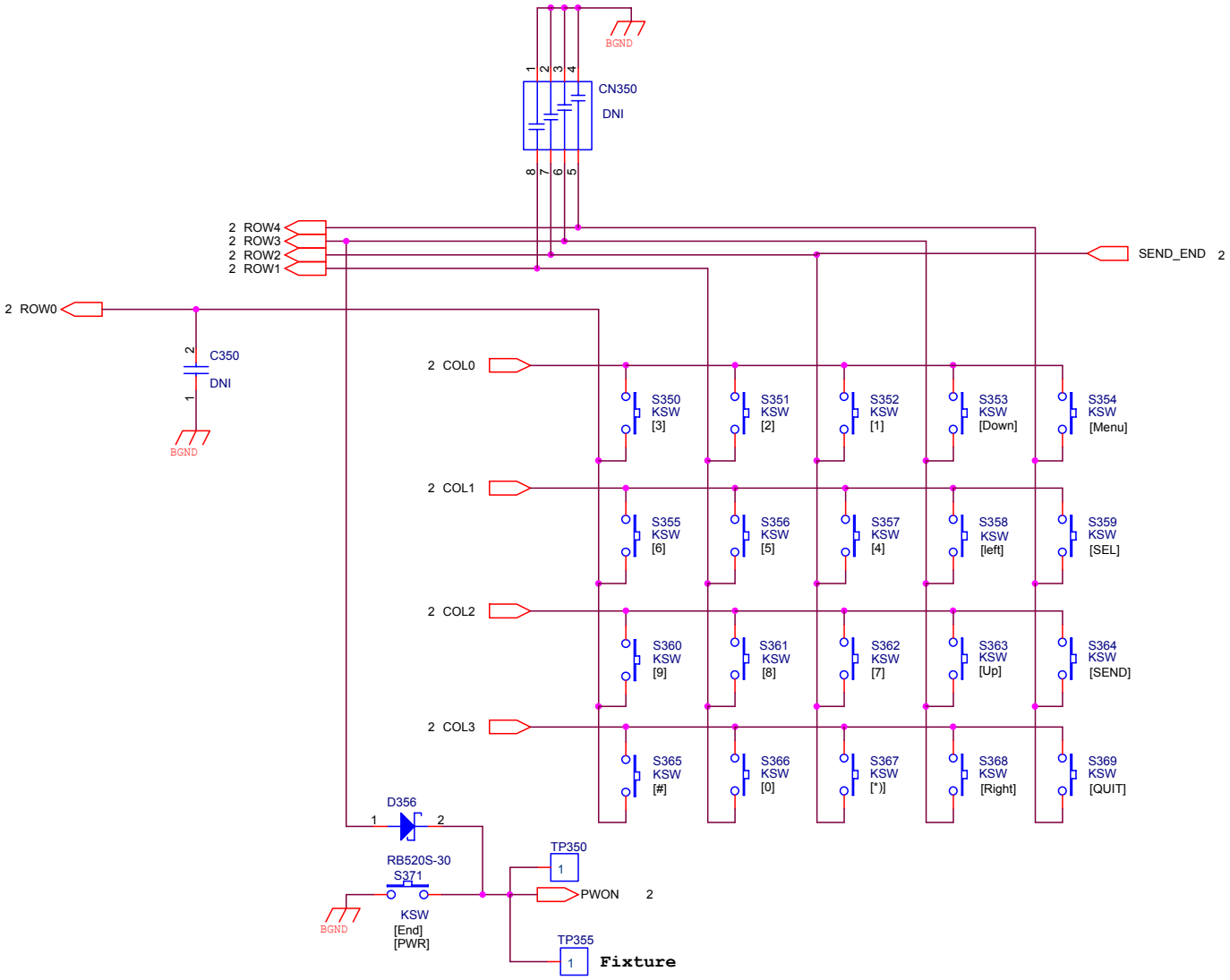
The SIM interface of IOTA is composed by a dedicated LDO and I/O level shifters. It supports 3V and 1.8V SIM cards (In 56E11 just use the 3V).

SIM_IO(I/O): Data
SIM_RST(O): Reset signal
SIM_CLK(O): Clock (1.6MHz/3.2MHz)

The SIM card digital interface insures the translation of logic levels between CALYPSO-Lite and SIM card. Selection of pull-up resistor is trade-off between the SIM IO rising time and current consumption

3.13 Keypad

3.13.1 Schematic



3.13.2 Description

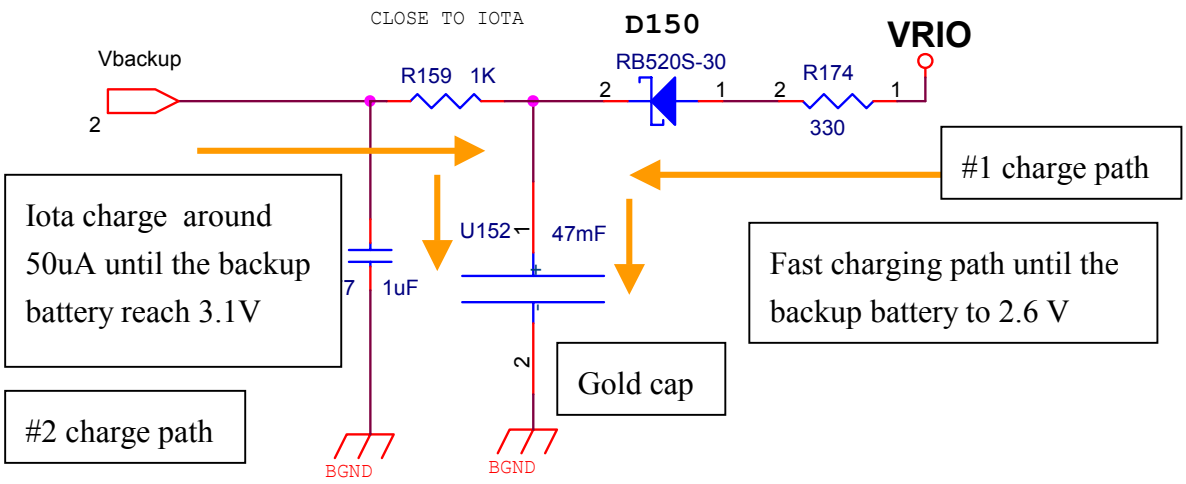
1. The keypad is made of a 5 Column x 5 Row matrixes.
2. The keypad matrix is as follows:

Function	Key	COL0	COL1	COL2	COL3	COL4	ROW0	ROW1	ROW2	ROW3	ROW4
END/PWR	S371										
3	S350	0					0				
2	S351	0						0			
1	S352	0							0		
DOWN	S353	0								0	
MENU	S354	0									0
6	S355		0				0				
5	S356		0					0			

4	S357		0						0		
LEFT	S358		0							0	
YES/Send	S359		0								0
8	S361			0				0			
7	S362			0					0		
UP	S363			0						0	
SEND	S364			0							0
9	S360			0			0				
#	S365				0		0				
0	S366				0			0			
*****	S367				0				0		
RIGHT	S368				0					0	
NO	S369				0						0

3.14 RTC Circuit

3.14.1 Schematic

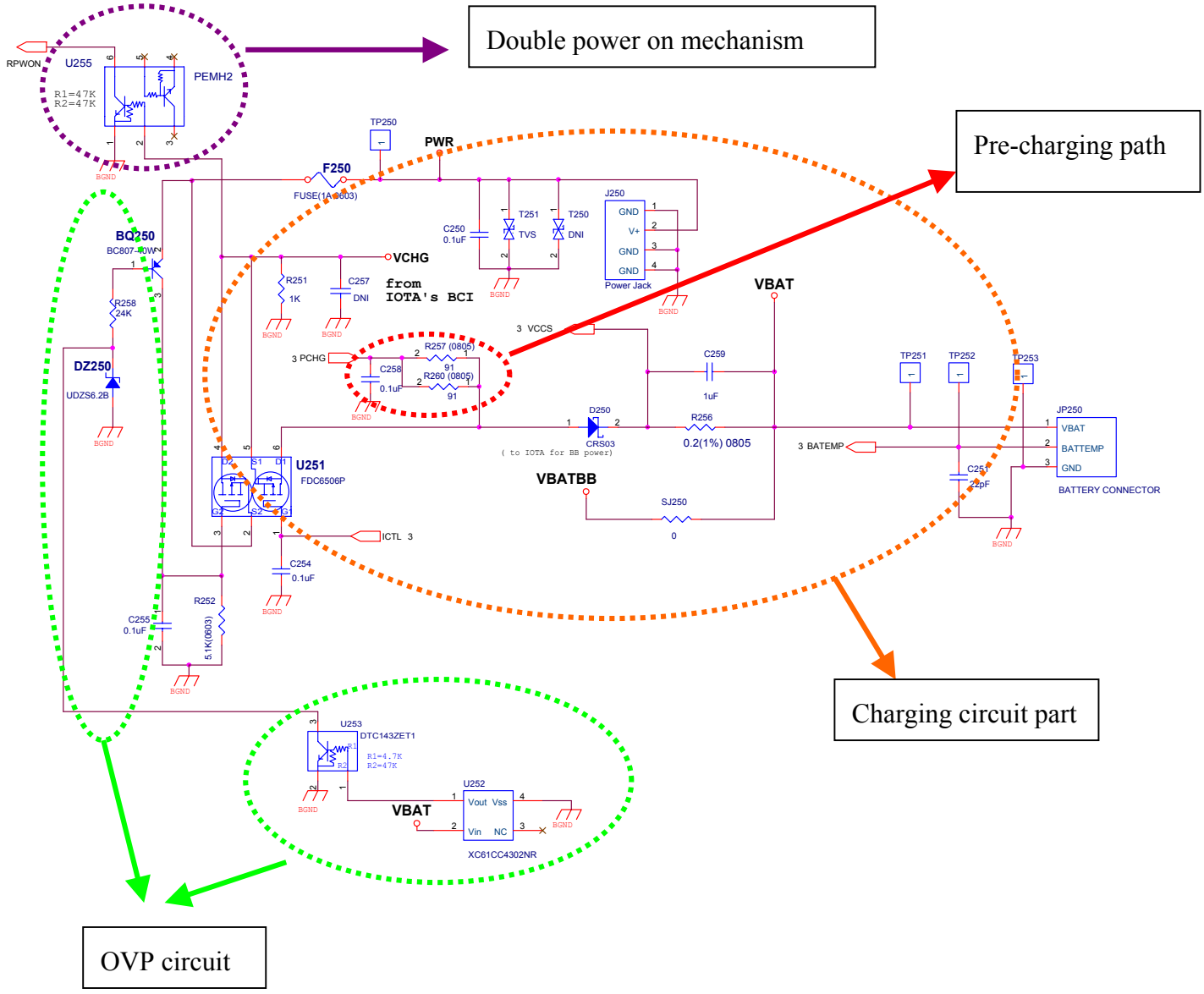


3.14.2 Description

Gold cap is employed as backup battery. When main battery is removed or battery voltage is lower than backup battery voltage, backup battery will supply real-time clock and the 32.768Hz oscillator. The supply current for backup battery is about 50uA. There are two charging paths for backup battery. The charge path #1 charge backup battery until backup battery voltage reachs around 2.6V. The charge path #2 is always on until backup battery is full-charged

3.15 Charging circuit

3.15.1 Schematic



3.15.2 Description

This circuit mainly contains OVP, Charge circuit part , and Double power on mechanism . The OVP gives system a voltage protection of over charger voltage or battery over charged. If the charger voltage is over 6.8 V and the battery is over charged to 4.4 V the OVP mechanism will work.

F250 is a 1A fuse to assure charging current under 1A limit. The group of BQ250 and DZ250 compose the charger over-charge protection circuit. The cut-off voltage is 6.8V. While the charger voltage is over 6.8V, the circuit will turn off U251 PMOS to stop charge process. The group of 253, BQ250 and U252 compose the battery over-charge protection circuit. While the battery voltage is over 4.4V, the circuit will turn on U252 to turn off U251 PMOS to stop charge process.

The normal charging operation theory (battery voltage above 3.2V) is that IOTA monitors charger voltage via VCHG pin to decide whether charger plug in or out, and control power P-MOSFET (U251.1) via ICTL pin. If phone enters into charging mode, the ICTL pin will limit the maximum charging current at 750mA(max) by sensor the R256 and control CC_H / CC_L mode. When VBAT equals to 4.2V, Iota will stop the charge function . The charging current will decrease until the charging current is lower than 30mA. In charging process, IOTA BCI always monitor the charging status. It can monitor charging current by current sense resistor (R256), VBAT and temperature by ADC pin, and charging time by internal timer. If there is any abnormal status happened while charging, IOTA BCI will turn off power P-MOSFET (U251.1) via ICTL pin to prevent any hazardous condition happening.

When VBAT<3.2V, charging state enters in “pre-charge” state. In this state, U251 is off and IOTA will supply pre-charge current from VCHG through VBAT to charge battery. We use R257 and R260 to set the pre-charge current between 35mA(VBAT=3V) to 75mA(VBAT=2V).

Double power on mechanism , this mechanism is to avoid the VCHG > Vbat power on function fail , therefore we use the Remote power on function to double turn on the power on sequence.

56E11 Li-ion 760mAH Battery Charging Algorithm

Linear Charger: 3.6V & 600mA

Definition

Full_Charge: FET is switched on, the charger is in CC mode.

T_{ON}: The period of Full_Charge and FET is switched on

T_{OFF}: The period that FET is switched off

150mA_Charge: FET is set to impose 150mA to battery

T_{ON-C}: The period of 150mA_Charge and FET is switched on

M: A positive integer, a sampling number

V_{CHARGE}: The detected average voltage of the charger when FET is off(M samples/1s)

I_{CHARGE}: The detected average current into the battery when FET is on(M samples/1s)

V_{BAT} :The detected average voltage of the battery when FET is off(M samples/1s)

V_{CELL} :The detected average voltage of the cell(M samples/1s)

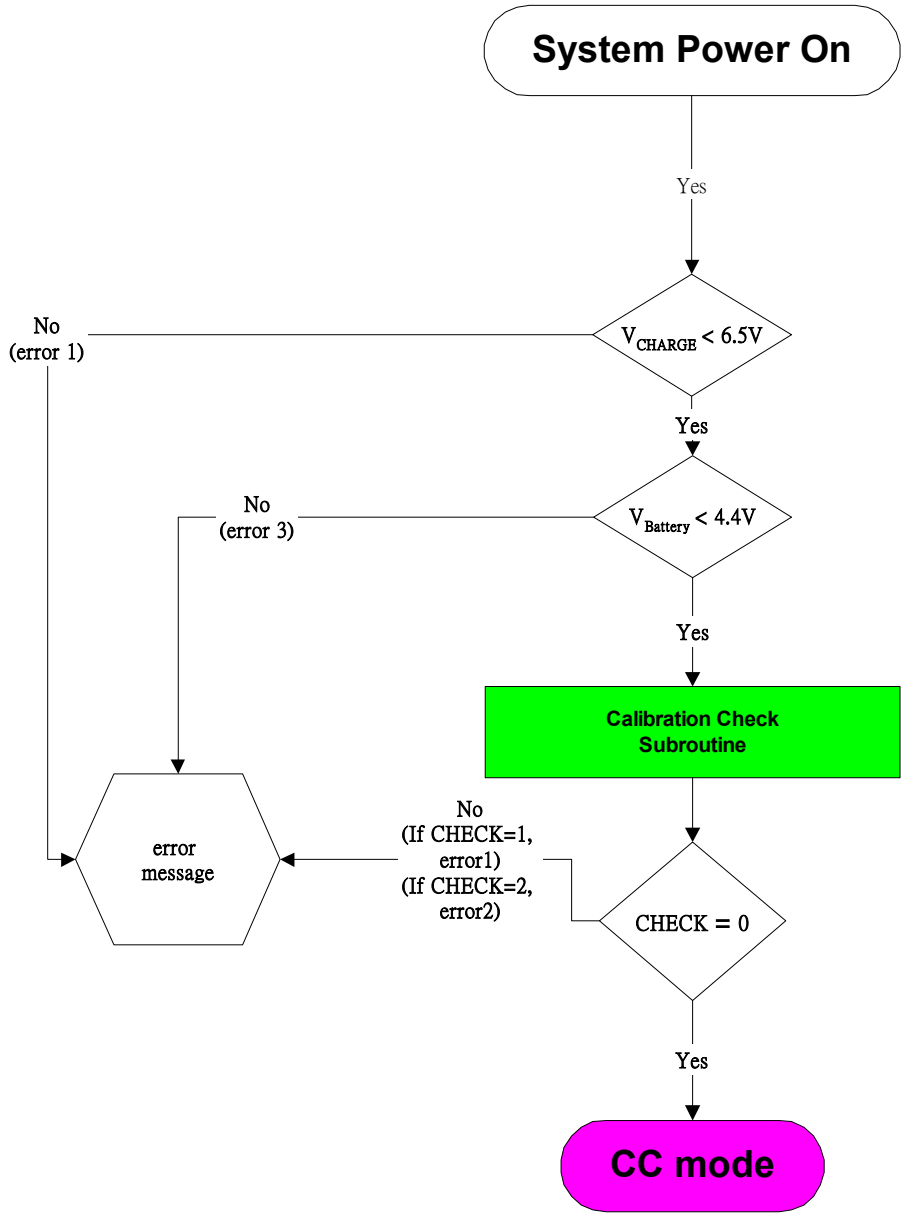
T_{SAFETY}: The defined safety timer of whole charging process

TIME: The period of single charging stage

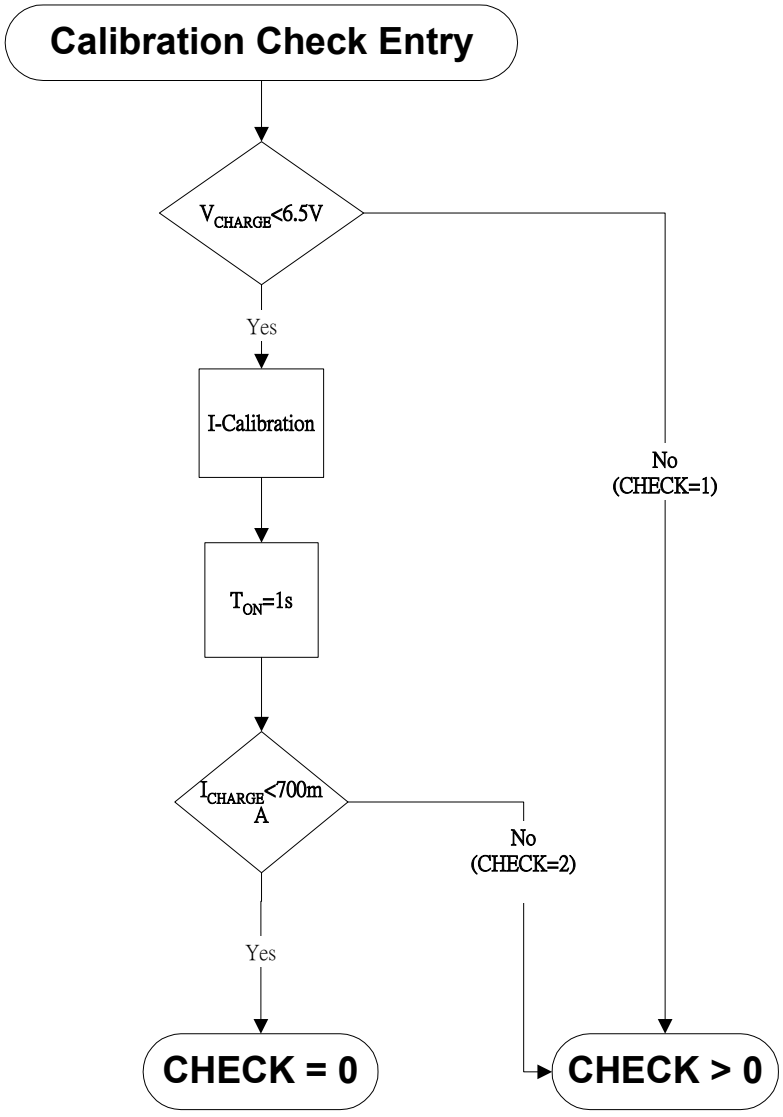
Temp: The temperature of battery(M samples/1s)

I-Calibration: System read the current offset

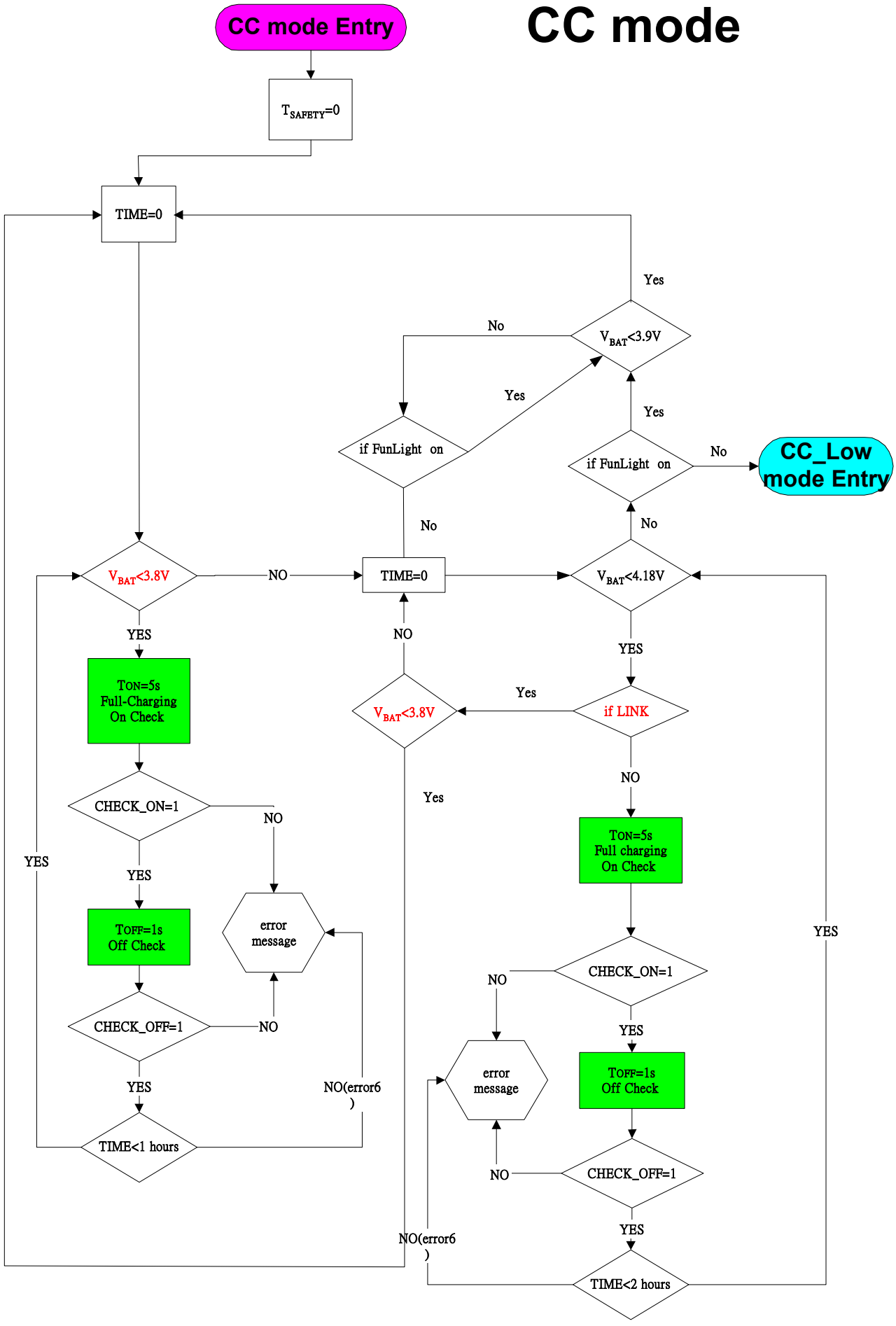
Software Charging Flow



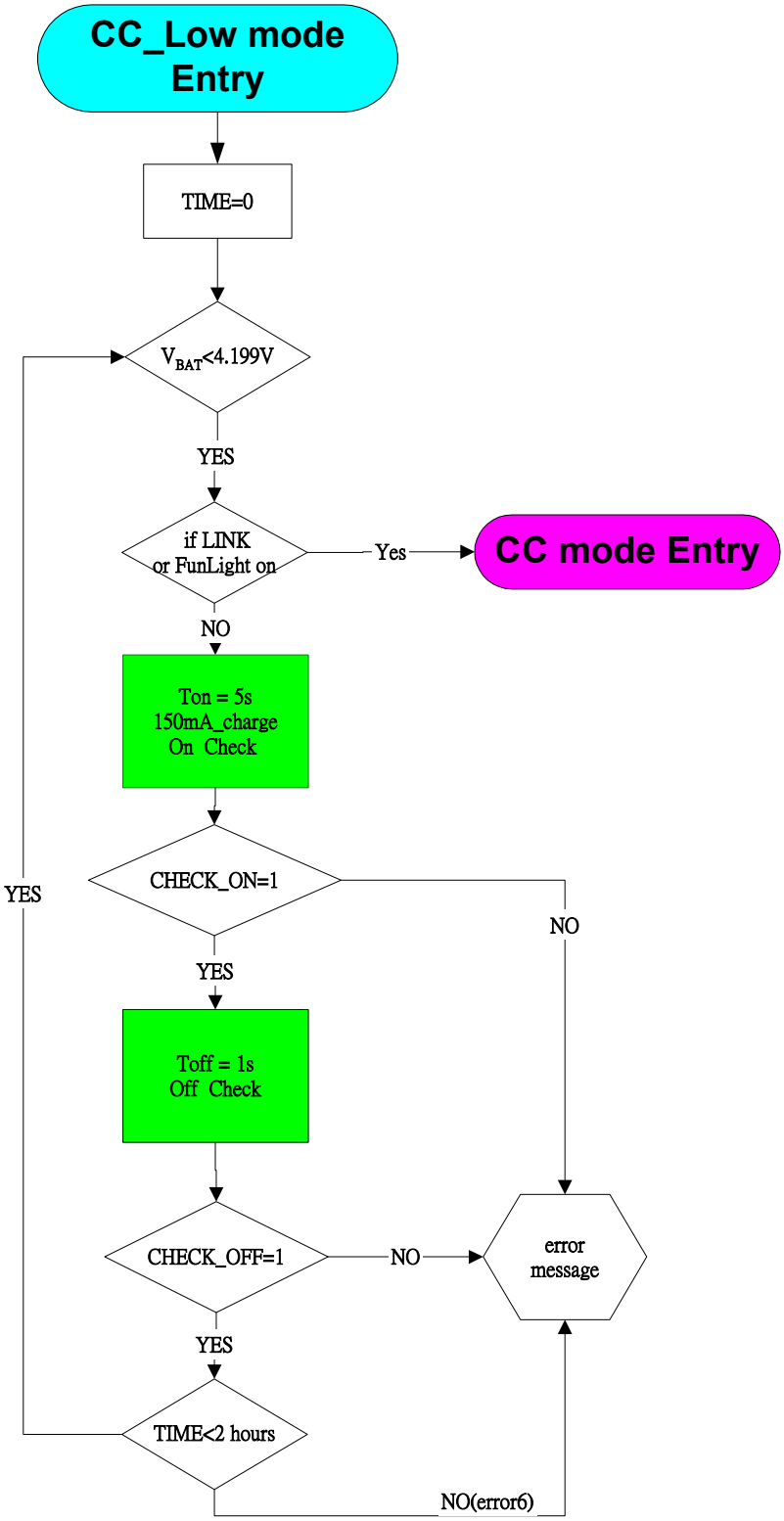
Calibration Check Subroutine



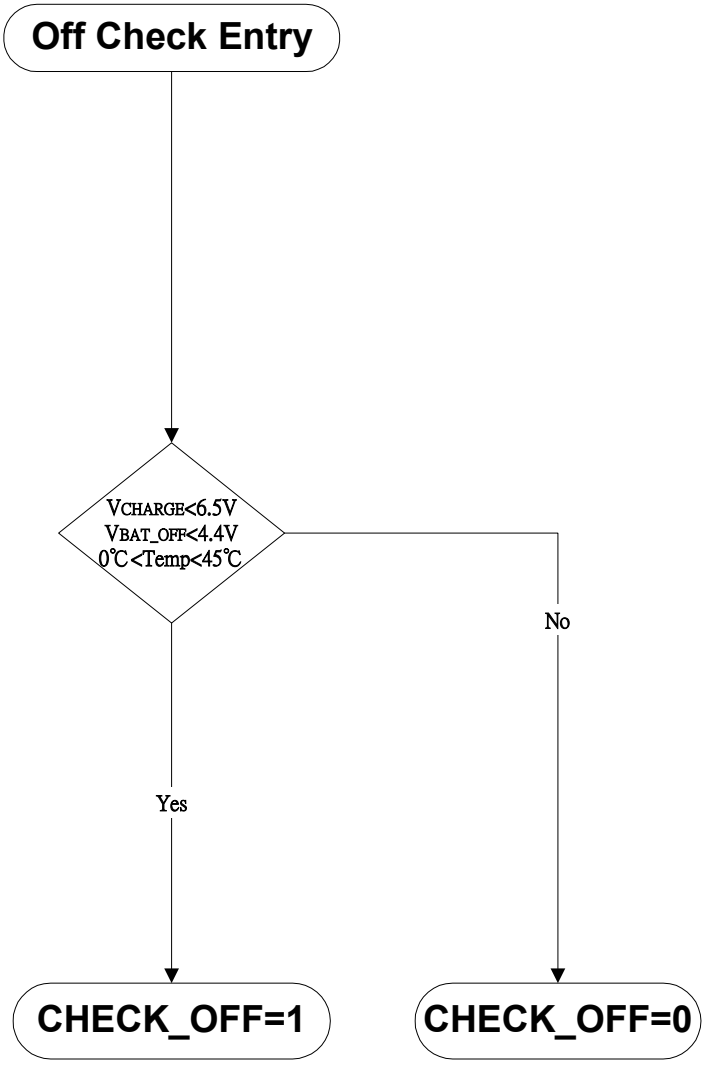
CC mode


CC mode Entry
T_{SAFETY}=0
TIME=0
V_{BAT}<3.9V
No
Yes
Yes
if FunLight on
Yes
if FunLight on
No
CC_Low mode Entry
No
No
V_{BAT}<3.8V
NO
TIME=0
V_{BAT}<4.18V
YES
NO
YES
T_{ON}=5s Full-Charging On Check
V_{BAT}<3.8V
Yes
if LINK
Yes
NO
CHECK_ON=1
NO
YES
YES
T_{ON}=5s Full charging On Check
T_{OFF}=1s Off Check
error message
YES
CHECK_ON=1
NO
YES
error message
T_{OFF}=1s Off Check
CHECK_OFF=1
NO
CHECK_OFF=1
NO
YES
YES
NO(error6)
NO(error6)
TIME<1 hours
TIME<2 hours

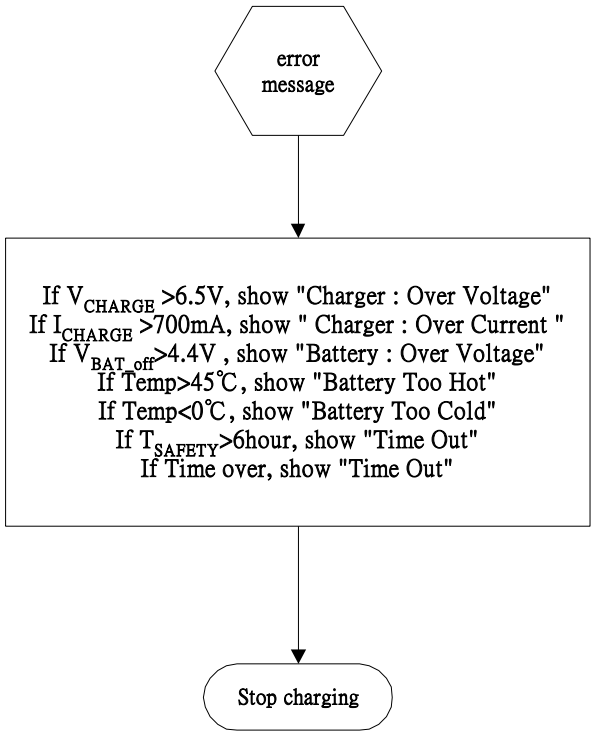
CC_Low mode


CC_Low mode Entry
TIME=0
V_{BAT}<4.199V
YES
if LINK or FunLight on
Yes
CC mode Entry
NO
Ton = 5s 150mA_charge On Check
CHECK_ON=1
YES
NO
YES
Toff = 1s Off Check
CHECK_OFF=1
NO
error message
YES
TIME<2 hours
NO(error6)

Off Check Subroutine



Error Messages



error 0 : "Illegal Battery"
error 1 : "Charger : Over Voltage"
error 2 : "Charger : Over Current "
error 3 : "Battery : Over Voltage"
error 4 : "Battery Too Hot"
error 5 : "Battery Too Cold"
error 6 : "Time Out"