Circuit Operation Theory for AWL300

Circuit Operation Theory

Basically speaking, the schematics could be separate in two parts:

1. **Analog Part**: Including HFA3983, HFA3683A, HFA3783, HFA3861B (Analog part)
2. **Digital Part**: Including HFA3861B (Digital part), AT76C503A, UT61L1024LC-12, AT25040N

1 Introduction

1.1 Scope

This document contains circuit operation theory for Wireless LAN USB AWL300.

1.2 Acronyms

AGC	AUTOMATIC GAIN-CONTROLLED-AMPLIFIER
BPF	Band-pass filter
BER	Bit-error rate
CCK	Complementary Code Keying
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DS-SS	Direct-sequence spread spectrum
DBPSK	Differential Binary Phase Shift Keying
DQPDK	differential quadrature phase shift keying
IEEE	Institute of Electrical and Electronic Engineers
IF	IF Frequency
ISM	**I**ndustrial, **S**cientific, and **M**edical
LNA	Low-noise amplifier
LO	Local oscillator
LPF	Low-pass filter
LQFP	Low Profile Quad Flat Pack
MAC	Media Access Control
mW	milliwatts(s)
P1dB	1 dB Compression Point
PA	Power amplifier
PHY	Physical layer
PLL	Phase-locked loop
PN	Pseudonoise
RF	Radio frequency
USB	Universal Serial Bus
VCO	Voltage-controlled oscillator
WEP	Wired Equivalent Privacy
WLAN	Wireless local area network

1.3 Referenced Documents

[1] Engineering Specification for AWL300

[2] Datasheet for AT76C503A

[3] Datasheet for HFA3861B

[4] Datasheet for HFA3783

[5] Datasheet for HFA3683A

[6] Datasheet for HFA3983

1.4 Record of Changes

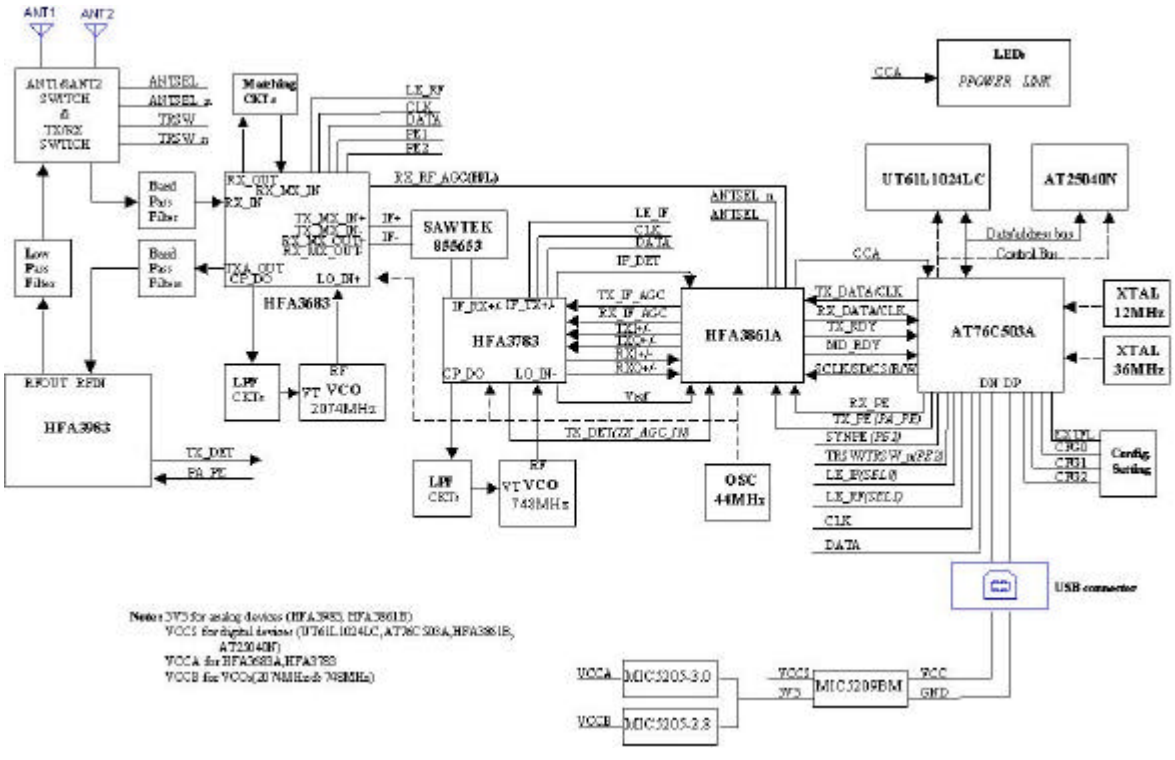
Change No.	Issue	Date	Reason of Change

2 Overview

The AcerCM ***Wireless LAN USB AWL300*** is a flexible data communications facility implemented as an extension to, or as an alternative for, a wired LAN. Using radio frequency (RF) technology, wireless LANs transmit and receive data over the air, minimizing the need for wired connections. Thus, wireless LANs combine data connectivity with user mobility.

3 Operation Theory Description

3.1 Function Block



3.2 Hardware Function description

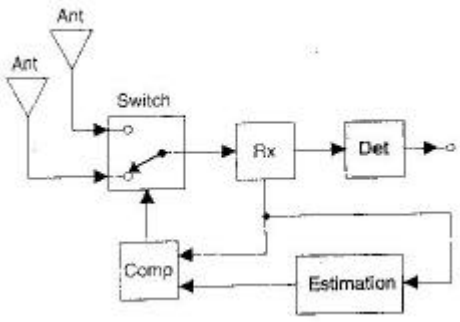
3.2.1 Overview

The BENQ AWL300 composed of six parts:

1. Antenna diversity principle
2. RF TX/RX section
3. IF signal processing section
4. Baseband signal processing section
5. MAC processor
6. Power supply section

3.2.2 Antenna diversity principle

We know that multipath Rayleigh fading severely degrades the average bit-error-rate (BER) of wireless digital radio transmission systems. In order to achieve highly reliable digital data transmission without excessively increasing both transmitter power and co-channel reuse distance. Diversity reception is one of the most effective techniques for this purpose. Since the cancellation of radio waves is geometry dependent, use of two antennas separately at least half of a wavelength can drastically mitigate this problem. On acquisition of a signal, the receiver checks each antenna and simply selects the antenna with the best signal quality.



Switching from one antenna to the other occurs when the signal level, which is the RSSI signal in AWL300 system, falls below a threshold. The threshold can be set a fixed value within a small area, but this value is not necessarily the best over the entire service area. In AWL300, when the firmware set the bit 7 of CR40 in baseband chip HFA3681B to be 1, the threshold is a absolute value. The threshold may be adjusted dynamically as the environment variations. In AWL300, when the bit 7 of CR40 is set to be 0, the threshold is relative to noise floor.

The control pins in HFA3681B are ANTSEL and ANTSEL_n, which are mutual complement for differential drive of antenna switches, are used to control RF switch U7 (UPG158TB). The operation mode follows this table.

ANTSEL	ANTSEL_n	ANT1/ANT2
High	Low	ANT2
Low	High	ANT1

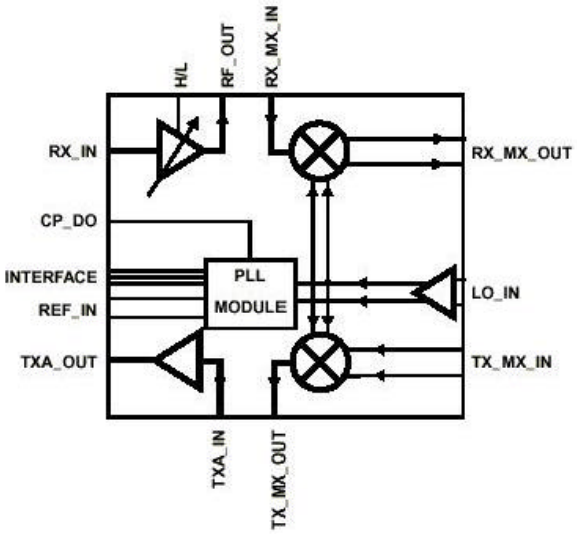
Selecting transmission and receiving branch, this system use TRSW and TRSW_n signals to control U11 (UPG158TB). The operation mode follows this table.

TRSW	TRSW_n	TX/RX
High	Low	TX
Low	High	RX

3.2.3 RF TX/RX section

In AWL300 system, we used two Intersil chips HFA3683A and HFA3983 to build up RF transceiver part.

The HFA3683A is a monolithic SiGe half-duplex RF/IF transceiver designed to operate in the 2.4GHz ISM band. **The receive chain** features a low noise, gain selectable amplifier ***(LNA)*** followed by a down-converter mixer. An up-converter mixer and a high performance preamplifier compose **the transmit chain**. The remaining circuitry comprises a high frequency Phase Locked Loop ***(PLL)*** synthesizer with a three wire programmable interface for local oscillator applications. A reduced filter count is realized by multiplexing the receive and transmit IF paths and by sharing a common differential Matching network. Furthermore, both transmit and receive RF amplifiers can be directly connected to mixers. The inherent image rejection of both the transmit and receive functions allow this economic advantage.



Simplified Block Diagram for HFA3683A

In receive mode, we use a multi-layered dielectric band pass filter ***(BPF)*** FL2 to reject interferers outside the 2.4GHz ISM band and providing image rejection. Next, the signal enters the HFA3683A, first passing through the integrated LNA section and then going off-chip to a matching circuit, which composed of L10 and C73.The signal then enters the downconverter section of the HFA3683A.Local oscillator injection is used to mix down to the single intermediate frequency ***(IF)***, 374MHz. A discrete LC matching is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 200Ù-

balanced environment.

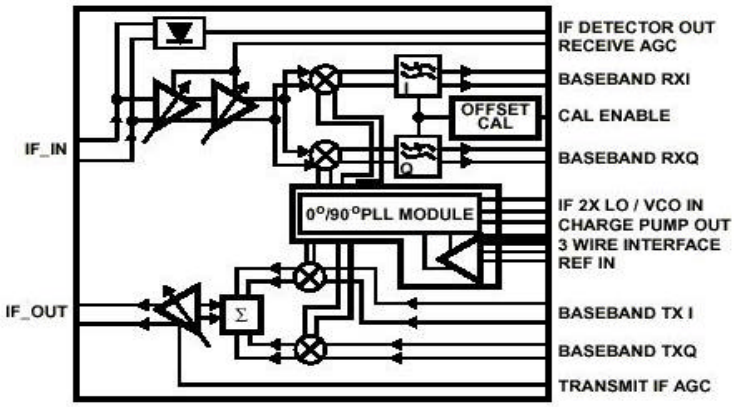
On the transmit side, the IF signal from IF SAW filter FL1 goes to the high impedance input of the HFA3683A uncovering mixer for conversion to the 2.4GHz – 2.5GHz band. The mixer output is directly coupled to the integrated pre-amplifier which amplifiers the selected sideband, easing the requirement for HFA3983 RFPA gain.

Two multi-layered dielectric band pass filters ***(BPF)***, FL3 and FL5, are used to suppress both transmit LO leakage and the undesired sideband. The HFA3983 RFPA amplifies the transmit signal. The HFA3983 is a 2.4GHz monolithic SiGe Power Amplifier designed to operate in the ISM Band. It features two low voltage single supply stages Cascaded, they deliver a 18dBm (Typ.) of an output power for the typical DSSS signal (ACPR, 1st Side Lobe < -30dBc, 2nd Side Lobe < -50dBc). In addition, the device includes a 2.4GHz detector which is accurate over a 15dB of dynamic range with (±)1dB. Therefore, an accurate ALC function can be implemented. The LPF FL4 rejects interferers outside above the 2.4GHz ISM band and provides image rejection.

3.2.4 IF signal processing section

IF-signal processing section locates between RF and baseband section. It consists of two major components: SAW filter and HFA3783.

The HFA3783 is a highly integrated and fully differential SiGe Baseband converter for half duplex wireless applications. It features all the necessary blocks for quadrature modulation and demodulation of “I” and “Q” Baseband signals. It has an integrated AGC receive IF amplifier with frequency response to 600MHz. The AGC has 70dB of voltage gain and better than 70dB of gain control range. The transmit output also features gain control with 70dB of range. The receive and transmit IF paths can share a common differential matching network to reduce the filter component count required for single IF half duplex transceivers. A pair of 2nd order anti-aliasing filters with an integrated DC offset cancellation architecture is included in the receive chain for baseband operation down to DC. In addition, an IF level detector is included in the AGC chain for threshold comparison. Up and down conversion are performed by doubly balanced mixers for “I” and “Q” IF processing. These converters are driven by a broadband quadrature LO generator (U4) with frequency of operation phase locked by an internal 3-wire interface synthesizer and PLL.



Simplified Block Diagram for HFA3783

The majority of frequency synthesis is derived from the PLL. Figure 1 demonstrates all of the vital circuits that make up a common single loop PLL synthesizer. A 44MHz crystal oscillator feeds a reference frequency into the R divide, which decreases the reference frequency to equal the desired frequency out of the N adjustable frequency divider. The reference frequency out of the R divider is then inserted into the phase comparator, which compares the phase of the R divider to that of the N adjustable frequency divider. The adjustable N frequency divider receives its own input frequency from the VCO' s (U4) output, dropping it down to a lower frequency that must be equal to the R divider' s output. As the phase comparator is comparing the two frequencies at its input from the N and R dividers to see if they are of the same phase, it will produce a rectified DC correction voltage at its output into the low-pass PLL loop filter if these two frequencies differ. This filter eliminates any AC variations and noise products, placing the now pure DC directly into the VCO' s frequency control input. The all-important loop filter is required to filter powerful phase comparator constitutes at the comparison frequency and its harmonics, since if these responses actually got through to the VCO they would adversely modify its stability. The varactor diode' s bias within the VCO is affected by this DC control voltage, which immediately forces the VCO back on frequency if it has drifted off. These actions permit a frequency source to be adjustable over many discrete frequencies, but with the stability of the crystal oscillator reference.

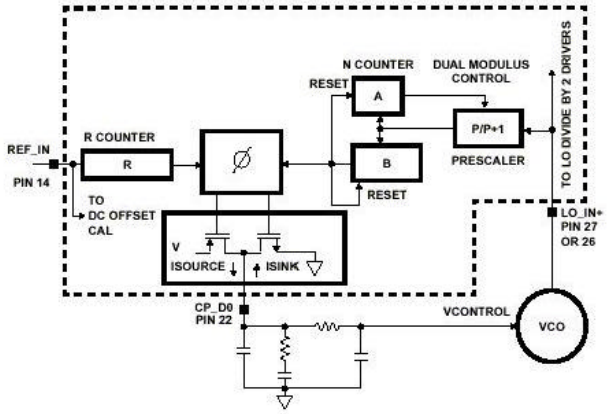


Figure 1. PLL SIMPLIFIED BLOCK DIAGRAM

SAW filters are indispensable in applications calling for steep skirts, linear phase, and low amplitude ripple. The basic SAW transducer is a bi-directional radiator. That is, half of the power is directed toward the output transducer while the other half is radiated toward the end of the crystal and is lost. By reciprocity, only half of the intercepted acoustic energy at the output is reconverted to electrical energy; hence, the inherent 6 dB loss associated with this structure. (Refer to Figure 2.). Since a SAW device consists of metal electrodes separated by a dielectric material, the return loss appears quite capacitive on the Smith chart

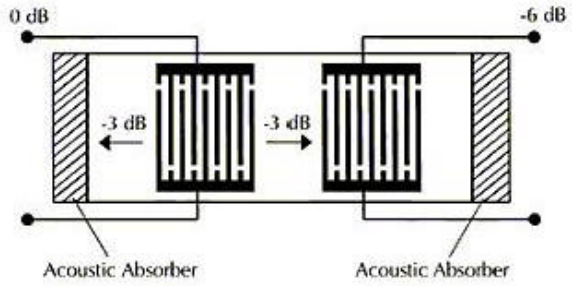
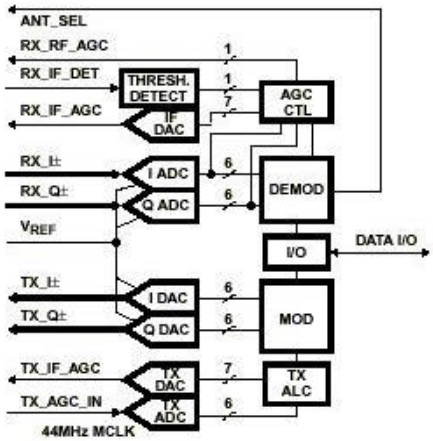


Figure 2. Simple transversal SAW filter configuration

In AWL300, the IF receive filter FL1, is a SAW device used for channel selection within the band. The SAW output is reactively matched to the IF input of the HFA3783 I/Q Modulator/ Demodulator and Synthesizer

3.2.5 Baseband signal processing section

The HFA3861B has on-board A/D' s and D/A for analog I and Q inputs and outputs, for which the HFA3783 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with Complementary Code Keying to provide a variety of data rates. Built-in flexibility allows the HFA3861B to be configured through a general-purpose control bus, for a range of applications. Both Receive and Transmit AGC functions with 7-bit AGC control obtain maximum performance in the analog portions of the transceiver



Simplified Block Diagram for HFA3861B

On the transmit side, the transmit data port accepts the data that needs to be transmitted serially from an MAC processor The data is modulated and transmitted as soon as it is received from the MAC processor. The serial data is input to the HFA3861B through TXD using the next rising edge of TXCLK to clock it in the HFA3861B. TXCLK is an output from the HFA3861B. The MAC processor initiates the transmit sequence by asserting TX_PE. TX_PE envelopes the transmit data packet on TXD. The HFA3861B internally generates the preamble and header information from information supplied via the control registers. The MAC processor needs to provide only the data portion of the packet and set the control registers. Assertion of TX_PE will initialize the generation of the preamble and header. TX_RDY,

which is an output from the HFA3861B, is used (if needed) to indicate to the MAC processor that the preamble has been generated and the device is ready to receive the data packet ***(MPDU)*** to be transmitted from the MAC processor. The transmit port is completely independent from the operation of the other interface ports including the RX port, therefore supporting a full duplex mode.

The HFA3861B transmitter is designed as a DSSS modulator. It can handle data rates of up to 11Mbps. The various modes of the modulator are DBPSK for 1Mbps, DQPSK for 2Mbps, and CCK for 5.5Mbps and 11Mbps. These implement data rates as shown in Table 1.

DATA MODULATION	A/D SAMPLE CLOCK (MHz)	TX SETUP CR 5 BITS 1, 0	RX SIGNAL CR 63 BITS 7, 6	DATA RATE (Mbps)	SYMBOL RATE (MSPS)
DBPSK	22	00	00	1	1
DQPSK	22	01	01	2	1
CCK	22	10	10	5.5	1.375
CCK	22	11	11	11	1.375

Table 1.BIT RATE TABLE EXAMPLES FOR MCLK = 44MHz

The signal from IF section is mixed down to baseband with the quadrature baseband demodulator into the I and Q components. The baseband circuit samples the waveform with 6-bit ADCs and demodulates the received data. The receive data port serially outputs the demodulated data from RXD. The data is output as soon as it is demodulated by the HFA3861B. RX_PE must be at its active state throughout the receive operation. When RX_PE is inactive the device's receive functions, including acquisition, will be in a stand by mode. RXCLK is an output from the HFA3861B and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the HFA3861B and it may be set to go active after the SFD or CRC fields. Note that RXCLK becomes active after the Start Frame Delimiter (SFD) to clock out the Signal, Service, and Length fields, then goes inactive during the header CRC field. RXCLK becomes active again for the data. MD_RDY returns to its inactive state after RX_PE is deactivated by the MAC controller, or if a header error is detected. A header error is either a failure of the CRC check, or the failure of the received signal field to match one of the 4 programmed signal fields. For either type of header error, the HFA3861B will reset itself after reception of the CRC field. If MD_RDY had been set to go active after CRC, it will remain low. MD_RDY and RXCLK can be configured through

CR 1, bits 1 and 0 to be active low, or active high. The receive port is completely independent from the operation of the other interface ports including the TX port, supporting therefore a full duplex mode.

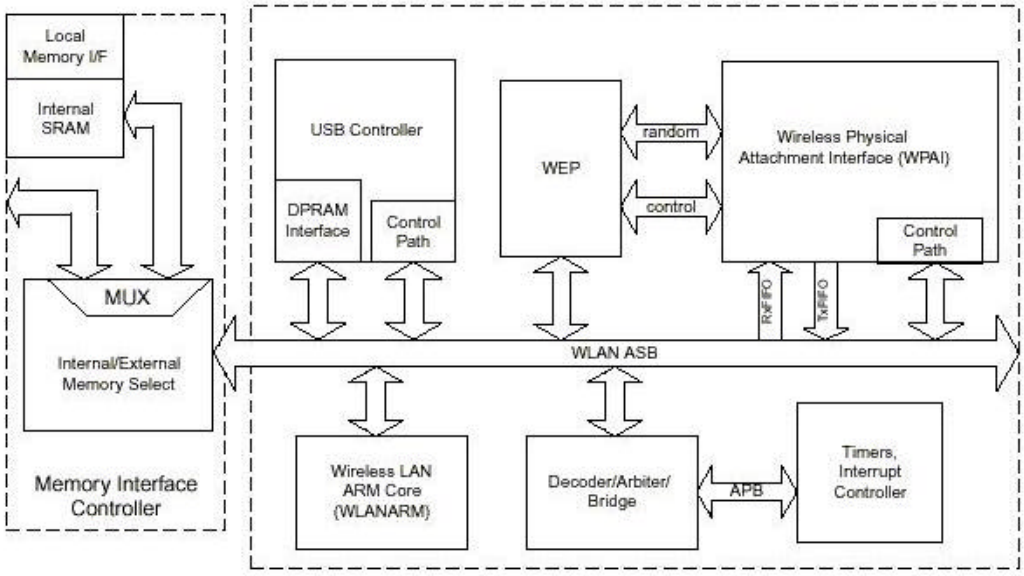
The clear channel assessment (CCA) circuit implements the carrier sense portion of a carrier sense multiple access (CSMA) networking scheme. The Clear Channel Assessment (CCA) monitors the environment to determine when it is feasible to transmit.. We used this signal to light ***Link*** LED.

3.2.6 MAC processor

We adopt Atmel chip AT76C503A as the MAC processor in the AWL300 system. AT76C503A is a single-chip controller that provides all processing and functionality needed for the MAC protocol of wireless LANs (focusing on, but not limited to the IEEE 802.11b standard). AT76C503A provides a glueless interface conforming to 12-Mbit universal serial bus specifications and can control a variety of wireless physical interfaces.

The AT76C503A chip contains a USB interface, a MAC control unit, and a physical attachment interface (PAI). The PAI supports the new 5.5- and 11-Mbit WLAN physical interfaces and IEEE 802.11(1 or 2 Mbps) direct-sequence spread spectrum.

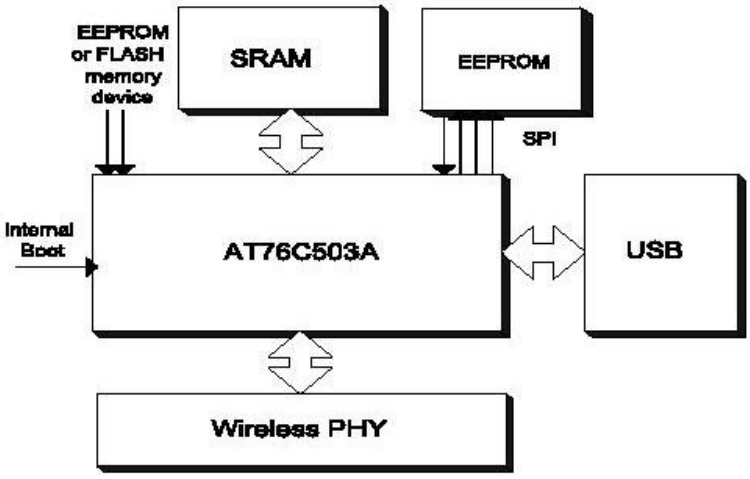
The ARM7TDMI core supports two alternative instruction sets. Powerful 32-bit code can be executed by the processor in ARM@ operating mode, however, a 16-bit instruction subset is also available in THUMB@ mode. THUMB@ mode can be selected to exploit full processor power with limited external memory resources. Note that ARM7TDMI operating mode can be changed at run time with negligible overhead.



Simplified Block Diagram for AT76C503A

The External Memory Interface (EMI) is used by AT76C503A to gain access to Flash and SRAM memory that accompanies a complete AT76C503A-based design. Flash memory contains the AT76C503A firmware, while SRAM memory accommodates the ARM core stack, AT76C503A firmware status variables, structures supporting host/firmware interface and network data buffers. In AWL300, the SRAM size is 1M. When the host driver software

passes network data to AT76C503A through the USB interface unit, the data is automatically re-routed to the external memory interface in order to reach SRAM In AWL300, parallel flash is omitted and firmware is downloaded into internal memory through DFU. The series EEPROM (U13, memory size is 512 byte) contain some control register values used by MAC processor, like CR31, CR58, VID, PID, MAC address.



Configuration for AT76C503A (no parallel flash)

3.2.7 Power supply section

System power supply configuration is as following table:

Net name	Voltage	Components associated with this power
VCC	5V	Main power from PC via USB connector
3V3	3.3V	HFA3983, HFA3861B
VCCS	3.3V	UT61L1024LC, AT76C503A, HFA3861B, AT25040N
VCCA	3.0V	HFA3683A, HFA3783
VCCB	2.8V	VCOs(2074MHz & 748MHz)

Technical Description fro AWL300

Product Internal Engineering Specification –AWL300

1. Introduction

1.1 Distribution

1.2 Product Objective

The Wireless LAN USB Adapter AWL300 is a flexible data communications facility implemented as an extension to, or as an alternative for, a wired LAN. Using radio frequency (RF) technology, wireless LANs transmit and receive data over the air, minimizing the need for wired connections. Thus, wireless LANs combine data connectivity with user mobility.

1.3 Functions

AWL300 provides a notebook PC with USB interface the wireless-communication capability that is IEEE 802.11b compliant for data, video and audio transportation of up to 11Mbit/s rate with other PCs, servers which are also equipped with the same facility. AWL300 performs station functions under either infrastructure or ad-hoc mode. The AWL300 connects with notebook PC via USB type II interface.

2. Applicable Documents

2.1 ACM Documents

N/A

2.2 Other Documents

IEEE802.11 Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications

3. Requirement

3.1 Hardware Requirement

Standard Compliance：

- IEEE 802.11b

Frequency Range：

- 2.412 ~ 2.484 GHz (Subject to local requirements)

Spreading：

- Direct Sequence Spread Spectrum (DSSS)

Operating Channel numbers：

- N. America/FCC: 2.412~2.462 GHz (11 channels)
- Europe CE/ETSI: 2.412~2.472 GHz (13 channels)
- Japan: 2.412~2.484 GHz (14 channels)
- France: 2.457~2.472 GHz (4 channels)
- Spain: 2.457~2.462 GHz (2 channels)

3.1.1 Transmit Spectrum Mask

The transmitted spectral products shall be less than –30dBr (dB relative to the SINx/x peak) for

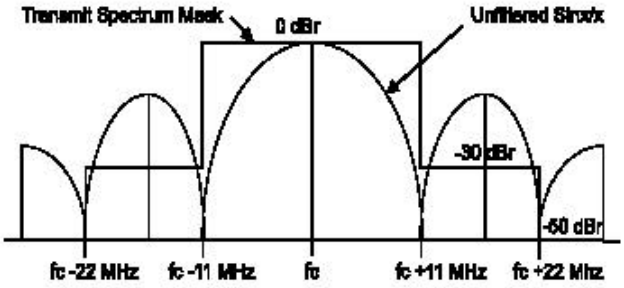
fc-22MHz< f <fc-11MHz; and fc+22MHz< f <fc+11MHz

And shall be less than –50dBr for

f<fc-22MHz and f>fc+22MHz

Where fc is the channel center frequency as shown in following table.

The transmit-spectral mask is shown in figure 1. The spectrum analyzer is set to 100kHz resolution bandwidth and 100kHz video bandwidth. The data rate is set to 11Mbps.



Item	Channel	Frequency (fc)	First Side Lobe	Second Side Lobe	Output Power
1	1	2412MHz	>30dBc	>50dBc	12dBm<Power<20dBm
2	2	2417MHz	>30dBc	>50dBc	12dBm<Power<20dBm
3	3	2422MHz	>30dBc	>50dBc	12dBm<Power<20dBm
4	4	2427MHz	>30dBc	>50dBc	12dBm<Power<20dBm
5	5	2422MHz	>30dBc	>50dBc	12dBm<Power<20dBm
6	6	2437MHz	>30dBc	>50dBc	12dBm<Power<20dBm
7	7	2442MHz	>30dBc	>50dBc	12dBm<Power<20dBm
8	8	2447MHz	>30dBc	>50dBc	12dBm<Power<20dBm
9	9	2452MHz	>30dBc	>50dBc	12dBm<Power<20dBm
10	10	2457MHz	>30dBc	>50dBc	12dBm<Power<20dBm
11	11	2462MHz	>30dBc	>50dBc	12dBm<Power<20dBm
12	12	2467MHz	>30dBc	>50dBc	12dBm<Power<20dBm
13	13	2472MHz	>30dBc	>50dBc	12dBm<Power<20dBm
14	14	2484MHz	>30dBc	>50dBc	12dBm<Power<20dBm

3.1.2 Wideband Spur Sweep

None of signal (except the carrier) with frequency between 100MHz to 7500MHz is higher than –45dBm. The data rate is set to 11Mbps.

Item	Channel	Specification
1	1	<-45dBm
2	2	<-45dBm
3	3	<-45dBm
4	4	<-45dBm
5	5	<-45dBm
6	6	<-45dBm
7	7	<-45dBm
8	8	<-45dBm
9	9	<-45dBm
10	10	<-45dBm
11	11	<-45dBm
12	12	<-45dBm
13	13	<-45dBm
14	14	<-45dBm

3.1.3 Carrier Frequency Accuracy

The tolerance of the transmitted central frequency shall be less than ± 25ppm (60 KHz). The data rate is set to 11Mbps.

Item	Channel	Frequency	Deviation	Range
1	1	2412MHz	<60KHz	2411.940~2412.060MHz
2	2	2417MHz	<60KHz	2416.940~2417.060MHz
3	3	2422MHz	<60KHz	2421.940~2422.060MHz
4	4	2427MHz	<60KHz	2426.940~2427.060MHz
5	5	2432MHz	<60KHz	2431.940~2432.060MHz
6	6	2437MHz	<60KHz	2436.940~2437.060MHz
7	7	2442MHz	<60KHz	2441.940~2442.060MHz
8	8	2447MHz	<60KHz	2446.940~2447.060MHz
9	9	2452MHz	<60KHz	2451.940~2452.060MHz
10	10	2457MHz	<60KHz	2456.940~2457.060MHz
11	11	2462MHz	<60KHz	2461.940~2462.060MHz
12	12	2467MHz	<60KHz	2466.940~2467.060MHz
13	13	2472MHz	<60KHz	2471.940~2472.060MHz
14	14	2484MHz	<60KHz	2483.940~2484.060MHz

3.1.4 Transmitter PER

PER <8% at receiver end when transmitter O/P power is -40dBm. The measurement is conducted with data rate of 11 Mbps.

Item	Channel	Frequency	Transmit PER
1	1	2412MHz	<8%
2	2	2417MHz	<8%
3	3	2422MHz	<8%
4	4	2427MHz	<8%
5	5	2422MHz	<8%
6	6	2437MHz	<8%
7	7	2442MHz	<8%
8	8	2447MHz	<8%
9	9	2452MHz	<8%
10	10	2457MHz	<8%
11	11	2462MHz	<8%
12	12	2467MHz	<8%
13	13	2472MHz	<8%
14	14	2484MHz	<8%

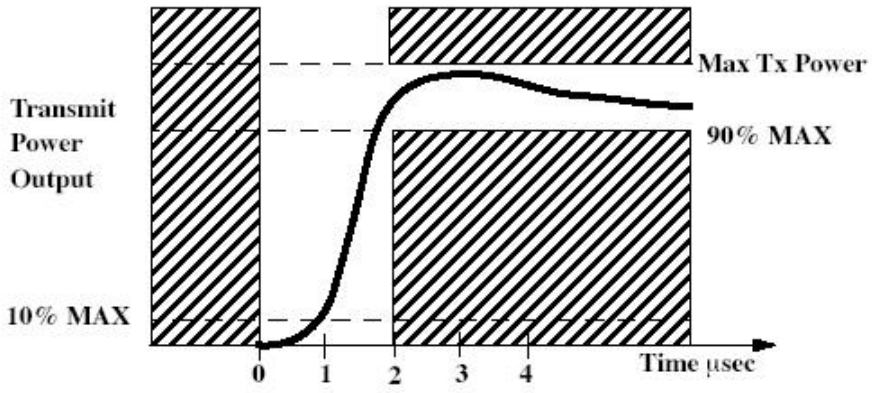
3.1.5 Carrier Suppression

The carrier suppression measured at the channel center frequency, shall be at least 15 dB below the peak power spectrum. The data rate is set to 11Mbps.

Item	Channel	Frequency	Deviation
1	1	2412MHz	>15dB
2	2	2417MHz	>15dB
3	3	2422MHz	>15dB
4	4	2427MHz	>15dB
5	5	2422MHz	>15dB
6	6	2437MHz	>15dB
7	7	2442MHz	>15dB
8	8	2447MHz	>15dB
9	9	2452MHz	>15dB
10	10	2457MHz	>15dB
11	11	2462MHz	>15dB
12	12	2467MHz	>15dB
13	13	2472MHz	>15dB
14	14	2484MHz	>15dB

3.1.6 Transmit power-on ramp

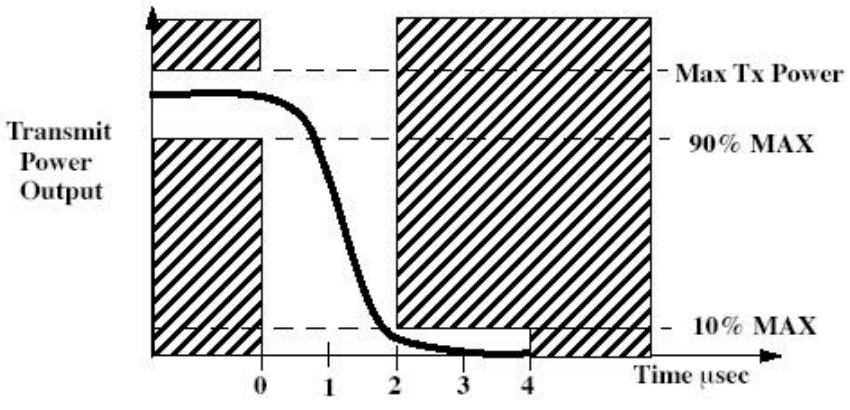
The time for transmit power-on ramp from 10% to 90% of maximum power shall be no greater than 2 μs. The data rate is set to 11Mbps.



Item	Channel	Frequency	Power-on ramp
1	1	2412MHz	<2us
2	2	2417MHz	<2us
3	3	2422MHz	<2us
4	4	2427MHz	<2us
5	5	2422MHz	<2us
6	6	2437MHz	<2us
7	7	2442MHz	<2us
8	8	2447MHz	<2us
9	9	2452MHz	<2us
10	10	2457MHz	<2us
11	11	2462MHz	<2us
12	12	2467MHz	<2us
13	13	2472MHz	<2us
14	14	2484MHz	<2us

3.1.7 Transmit power-down ramp

The time for transmit power-down ramp from 90% to 10% maximum power shall be no greater than 2 μs. The data rate is set to 11Mbps.



Item	Channel	Frequency	Power-down ramp
1	1	2412MHz	<2us
2	2	2417MHz	<2us
3	3	2422MHz	<2us
4	4	2427MHz	<2us
5	5	2422MHz	<2us
6	6	2437MHz	<2us
7	7	2442MHz	<2us
8	8	2447MHz	<2us
9	9	2452MHz	<2us
10	10	2457MHz	<2us
11	11	2462MHz	<2us
12	12	2467MHz	<2us
13	13	2472MHz	<2us
14	14	2484MHz	<2us

3.1.8 Power Consumption：

The current value is measured at channel 1, 6, 11 at data rate of 11Mbps.

Item	Action Mode	Power consumption (current)
1	Transmit	<380mA
2	Receive	<280mA

3.1.9 CW jammer adjacent channel rejection

When –50dBm signal is applied to the receiver that the data rate is ser to 11Mbps with PSDU length of 1024 octets, the PER of receiver can not exceed 8% under condition that a CW jammer with at most –15dBm level is also applied at adjacent channel with 25MHz offset.

Item	Channel	Frequency	Frequency +25MHz	Frequency –25MHz
1	1	2412MHz	>35dB	>35dB
2	2	2417MHz	>35dB	>35dB
3	3	2422MHz	>35dB	>35dB
4	4	2427MHz	>35dB	>35dB
5	5	2422MHz	>35dB	>35dB
6	6	2437MHz	>35dB	>35dB
7	7	2442MHz	>35dB	>35dB
8	8	2447MHz	>35dB	>35dB
9	9	2452MHz	>35dB	>35dB
10	10	2457MHz	>35dB	>35dB
11	11	2462MHz	>35dB	>35dB
12	12	2467MHz	>35dB	>35dB
13	13	2472MHz	>35dB	>35dB
14	14	2484MHz	>35dB	>35dB

3.1.10 Image rejection

When –76dBm signal is applied to the receiver that the data rate is ser to 11Mbps with PSDU length of 1024 octets, the PER of receiver cannot exceed 8% under condition that an image with at most –30dBm level is also applied at adjacent channel with -748MHz offset.

Item	Channel	Frequency	Image Frequency	Image Level
1	1	2412MHz	1664MHz	46dB
2	2	2417MHz	1669MHz	46dB
3	3	2422MHz	1674MHz	46dB
4	4	2427MHz	1679MHz	46dB
5	5	2422MHz	1684MHz	46dB
6	6	2437MHz	1689MHz	46dB
7	7	2442MHz	1694MHz	46dB
8	8	2447MHz	1699MHz	46dB
9	9	2452MHz	1704MHz	46dB
10	10	2457MHz	1709MHz	46dB
11	11	2462MHz	1714MHz	46dB
12	12	2467MHz	1719MHz	46dB
13	13	2472MHz	1724MHz	46dB
14	14	2484MHz	1734MHz	46dB

3.1.11 Sensitivity：

For an input signal level no less than –76dBm, the PER shall be less than 8% at a PSDU length of 1024 octets at respective channel and data rate.

Item	Channel	1Mbps	2Mbps	5.5Mbps	11Mbps
1	1	-80dBm	-80dBm	-76dBm	-76dBm
2	2	-80dBm	-80dBm	-76dBm	-76dBm
3	3	-80dBm	-80dBm	-76dBm	-76dBm
4	4	-80dBm	-80dBm	-76dBm	-76dBm
5	5	-80dBm	-80dBm	-76dBm	-76dBm
6	6	-80dBm	-80dBm	-76dBm	-76dBm
7	7	-80dBm	-80dBm	-76dBm	-76dBm
8	8	-80dBm	-80dBm	-76dBm	-76dBm
9	9	-80dBm	-80dBm	-76dBm	-76dBm
10	10	-80dBm	-80dBm	-76dBm	-76dBm
11	11	-80dBm	-80dBm	-76dBm	-76dBm
12	12	-80dBm	-80dBm	-76dBm	-76dBm
13	13	-80dBm	-80dBm	-76dBm	-76dBm
14	14	-80dBm	-80dBm	-76dBm	-76dBm

Modulation：

- 11Mbps (CCK) / 5.5 Mbps (CCK) / 2 Mbps (DQPSK) / 1 Mbps (DBPSK)

Antenna：

- Internal, with diversity function

Range Coverage：

- Open space: 100m – 300m
- Indoor space: 30m –100m

Data Security：

- 64/128-bit WEP (Wired Equivalent Privacy) Encryption

Host Interface：

- USB

Voltage Requirements：

- DC 5V

3.2 Software Requirement

Software Drivers Supported：

Windows: 98/98second edition/2000/ME (support NDIS5)/Win XP

Software Utility：

Software tools for diagnostics and management

Customization capability for tool and installation (option)

Network Architecture：

Supports Ad-Hoc Mode (Peer-to-Peer without Access Point) or Infrastructure Mode (Communications to wired networks via Access Points)

3.3 Mechanical Requirement

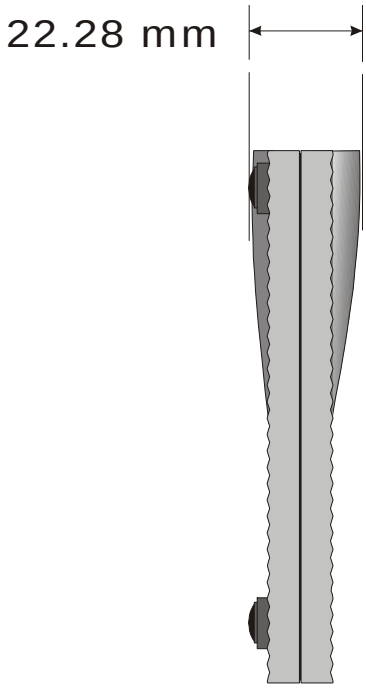
The physical dimension for AWL300 is:

Height: 31.7 mm

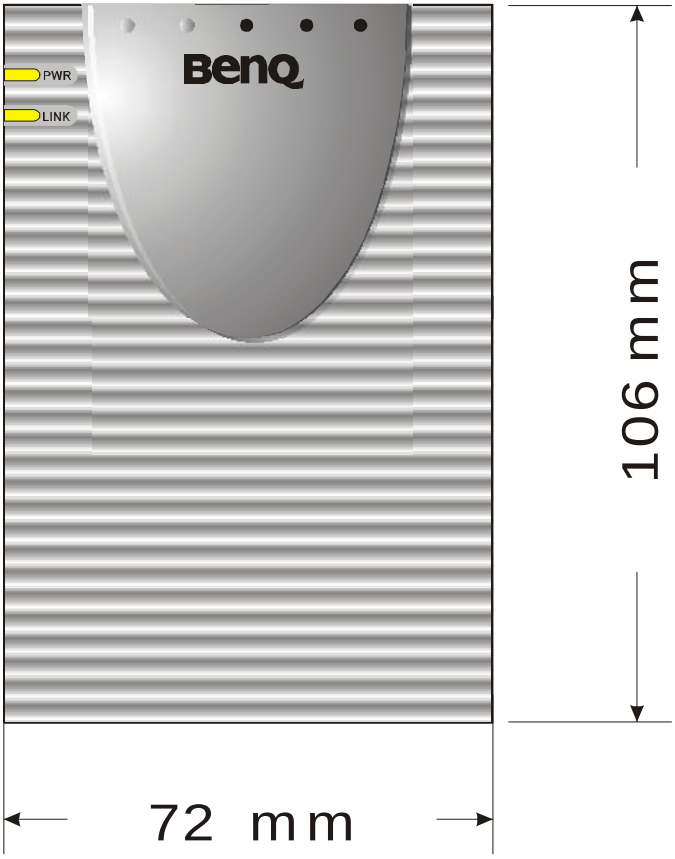
Width: 162 mm

Length: 103.5 mm

The USB interfaces is located on the rear-end panel. The rear panel is shown in the figure below. Two LEDs for indication of RF link and power are located on the top panel as shown below.



The AWL300 Side View



AWL300 Rear View

4. Document & Change

First Release

5. Regulatory

5.1 ESD Immunity

EN61000-4-2 criteria B:

5.2 EMI

FCC Part 15 (CFR 47) Class B

- FCC Part 15, Subpart B, Part 68
- UL 1950

6. Reliability, Maintainability & Quality

6.1 Reliability

MTBF: 4 years.

6.2 Maintainability

N/A

6.3 Quality

The product quality must satisfy conditions set forth in Acer factory's quality control manuals ED-024, ED-025, ED-608, ED-610, ED-614.

7. Environmental Requirements

7.1 Operating Environment:

Temperature : 5℃ to 40℃

Humidity: 10% to 90%, non-condensing

7.2 Storage Environment:

Temperature: -20℃ to 70℃

Humidity: 10% to 95%, non-condensing

8. Simulated Life Test Requirement

8.1 Operation Environment Criteria

8.1.1 High operation Temperature

55℃ with power on for 96 hours

8.1.2 Low operation Temperature

5℃ with power on for 96 hours

8.1.3 Normal Operation Temperature

25℃ with power on for 96 hours

8.2 Storage Environment Criteria

- 35℃ ~ 75℃ with power off in two cycle (1 cycle/day)

8.3 Thermal Shock Criteria

- 40℃ ~ 85℃ with power off for two days

8.4 Humidity Criteria

65℃ with power off , 90% RH for 48 hours

8.5 ESD Immunity Criteria

DUT shall comply with EN61000-4-2 criteria B:

Air: 8KV

Contact: 4KV

8.6 EMI regulation

DUT shall comply with FCC Part 15 (CFR 47) Class B

8.7 Card pull-out/plug-in Test

DUT shall function normally in-between 10000 times of plug-in/pull-out test.

8.8 Drop Test

Drop DUT two times in three mutually exclusive axes from a height of 75 cm onto a non-cushioning vinyl-tile surface.

8.9 Vibration Test

Apply 3G peak amplitude on DUT at 10~2000 Hz frequency with 12 cycles per axis and 36 cycles for three axes

9. Online Reliability Test

Perform all environment tests on 6 DUT per month.

10 Compatibility

WiFi for multi-vendor interoperability and IEEE 802.11 backward compatible. (optional)