# 5. WLAN Circuit Operation Theory

## 5.1 System Operation Theory

Figure 65 shows a block diagram of the system. The TNETW1100B supports glueless connection to CardBus, PCI, PCMCIA/CF+/Generic Slave, and USB host interface buses. The P50 design implements the 12-bit Generic Slave interface. The PDA host communicates to the 802.11b subsystem via the TNETW1100B host interface. Data transmitted by the Bulverde is stored within the TNETW1100B on-chip memory before being converted into baseband analog 802.11 signals. The baseband signals from the TNETW1100B are presented to a 2.4GHz radio for modulation and transmission over the air. The 802.11b signals received by the radio are converted to baseband and presented to the TNETW1100B's baseband processor where they are converted into digital signals for protocol processing by the MAC and storage within TNETW1100B on-chip memory for access by the host. The TNETW1100B system can supports two antennas for transmit and receive diversity but we don’t use this feature as for our P50 system.

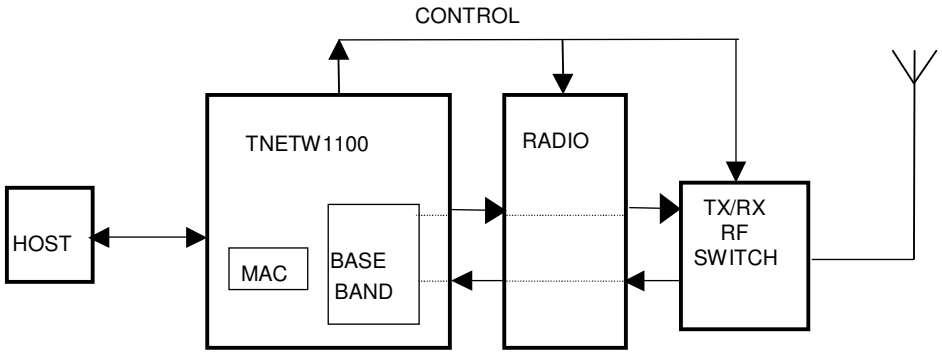


**Fig. 65 P50 WLAN system block diagram**

### 5.1.1 MAC and Baseband Functions

Figure 66 shows the blocks within the TNETW1100B that implement the MAC and Baseband functions.

**MAC**

The MAC hardware implements real-time functions such as access protocol management, encryption, decryption and data frame DMA. There is an ARM7 core embedded within the TNETW1100B hat provides the flexibility to adapt to improvements in the 802.11x standard. In a P50 application, firmware for the ARM7 core is automatically loaded by the OS NDIS drivers that run on the host PDA. The ARM7 orchestrates the 802.11 scan and join operations, manages the WEP key tables and maintains transmit and receive queues within on-chip SRAM.

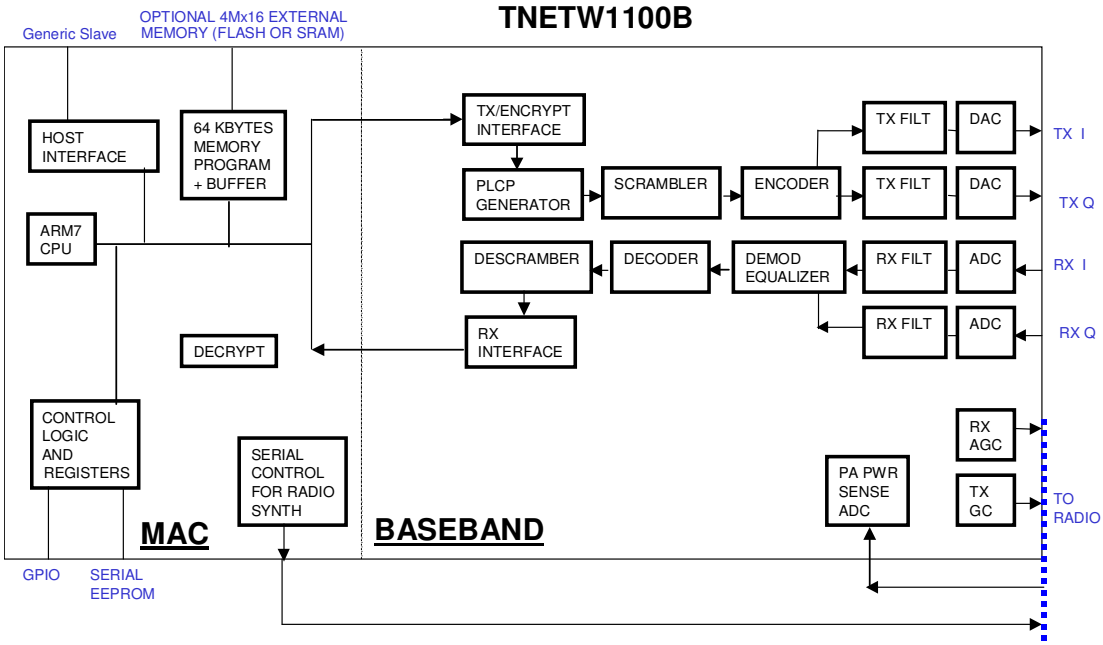


**Fig. 66 Detail block diagram of TNETW1100B**

## Baseband

The baseband logic is responsible for transmitting and receiving modulated signals. In the transmit direction the baseband logic reads a frame from TNETW1100B on-chip SRAM, performs physical layer encapsulation according to the 802.11b physical layer convergence protocol (PLCP). The PLCP frame is then scrambled before presentation to the encoder. The encoder supports Barker, CCK and PBCC algorithms. The encoded data is then converted to analog I and Q signals for modulation of the radio carrier. The receive channel in the baseband block reverses this process. In the receive direction, I and Q channel ADCs present a data stream to a demodulator/equalizer. The resulting data is decoded, descrambled and then stored in TNETW1100B on-chip SRAM for processing by the MAC.

## 5.1.2 Radio

Figure 67 shows the TNETW1100B based subsystem block diagram with a more detailed view of the radio.

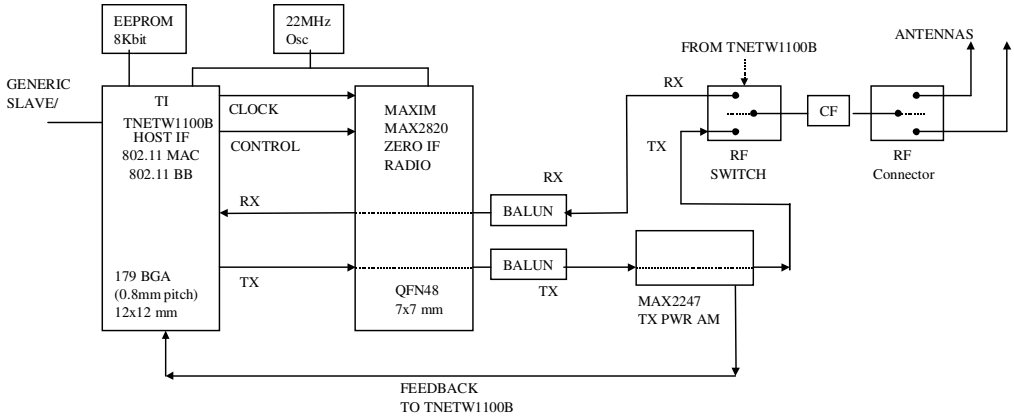


**Fig. 67 Block diagram showing MAXIM Radio**

### 5.1.2.1 Radio Hardware

The radio centers on the MAX2820, which is a highly integrated Zero IF transceiver. The MAX2820 includes transceiver, VCO, frequency synthesis and baseband interface functions. The input for the MAX2820 synthesizer is a 22 MHz clock generated by the crystal oscillator. The TNETW1100B uses a serial control channel to program the MAX2820.

### 5.1.2.2 Radio Transmit Path

Figure 68 shows the radio transmit path. Analog baseband data from the TNETW1100B is applied to the MAX2820 spread spectrum transceiver. The MAX2820 transceiver modulates a carrier in the 2.4GHz band that is generated by the synthesizer within the Max2820. The resulting modulated carrier is presented as a differential signal at the pins of the MAX2820. The differential signal is converted to single ended form by a BALUN transformer. The single ended signal is fed to a MAX2247 (2.4 GHz Linear Power amplifier), which supports a maximum linear output power of +24 dBm.

The output transmit signal from the power amplifier is presented to the antenna switch. The switch selects transmit or receive path. In this case, it is set for transmit. There is an additional ceramic filter to filter out of band spurious.

A transmit level feedback path from the MAX2242 to the TNETW1100B allows the TNETW1100B to measure the actual transmitted RF power and adjust the transmit gain in the MAX2820 transceiver accordingly. The TNETW1100B enables/disables the MAX2247 power amplifier, which is configured for a fixed gain.

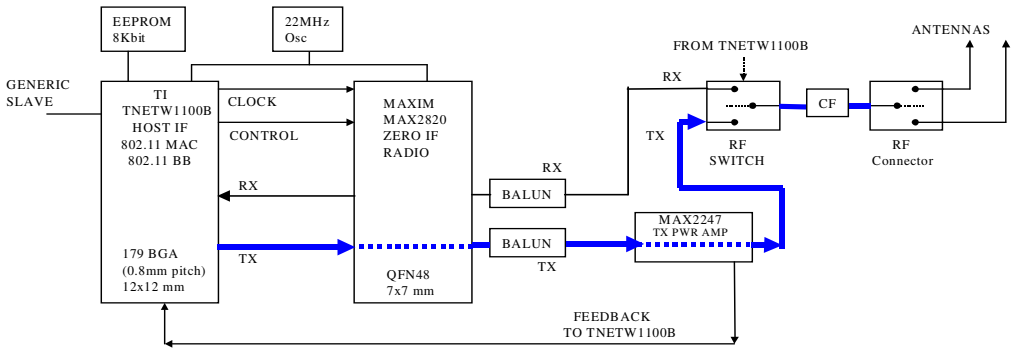


**Fig. 68 Radio transmission path**

## 5.1.2.3 Radio Receive Path

Figure 69 shows the radio receive path. RF signals arrive at the radio via an antenna. The RF signal passes through the switch that selects between transmit and receive paths. The receive signal then passes through a BALUN transformer which converts it from single ended to differential form. The differential receive signal is then applied to the MAX2820 transceiver. Within the MAX2820 the received signal is amplified and mixed with a local oscillator so that the desired baseband signal can be derived. The frequency of the local oscillator synthesized by the MAX2820 varies depending on the 802.11b channel selected.

The resulting baseband signal is then fed from the MAX2820 to the TNETW1100B. The TNETW1100B controls the receive path gain in the MAX2820 to eliminate clipping of the received signal at the TNETW1100B baseband analog to digital conversion stage, which expects a signal with a maximum peak-to-peak amplitude of 200 mV.

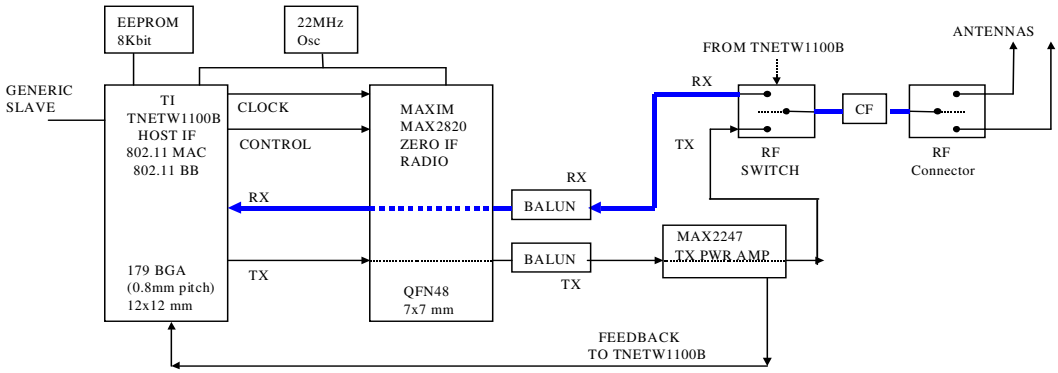


**Fig. 69 Radio receiving path**

## 5.1.3 TNETW1100B Firmware Download and Initialization

This section presents the procedures for initializing the TNETW1100B during system power up or reset.

### 5.1.3.1 Sense-On-Reset Pins

Upon power up or reset, the TNETW1100B reads the values on the MDATA[9:2, 0] pins to determine the external memory configuration, the firmware code image location, and the host interface mode. Table 1.1 provides descriptions of the sense-on-reset functionality for these pins. The values on these pins are loaded into a set of TNETW1100B registers. Because there are no internal resistors on these pins, external pull-up or pull-down resistors are implemented as shown on P50 circuit (logical 1 requires a pull-up resistor, logical 0 requires a pull-down resistor).

Besides the Sense-on-reset pins MDATA[6:5], the CFPLUS pin of the TNETW1100B further determines host Interface modes. If this pin is pulled high, the chip works in PCMCIA/CF+ mode. If this pin is pulled low, the chip works in Generic Slave mode. For our design, the CFPLUS pin is pulled low.

**Table 1.1 Sense-on-reset pins setting for P50 WLAN**

| Pin | Description | Settings For P50 |
|---|---|---|
| MDATA9 | 0 = 8-bit Flash device attached<br>1 = 16-bit Flash device attached | Don't care<br>(set to 0) |
| MDATA[8:7] | 00 = Flash on MCS0<br>01 = Flash on MCS1<br>10 = Flash on MCS2<br>11 = no Flash | 11 |
| MDATA[6:5] | Host Interface Mode:<br>00 = CardBus<br>01 = PCI<br>10 = Generic Slave/PCMCIA/CF+/USB<br>11 = PCI Control Point | 10 |
| MDATA4 | 0 = Host interface pads in CardBus/Generic Slave/PCMCIA/CF+/USB modes<br>1 = Host interface pads in PCI/PCI Control Point modes | 0 |
| MDATA3 | 0 = eCPU in little endian mode<br>1 = eCPU in big endian mode | 0 |
| MDATA2 | 0 = Download firmware from host and boot from internal zero- wait-state RAM<br>1 = Load firmware from Flash | 0 |
| MDATA0 | 0 = Disable auto-read from EEPROM upon reset<br>1 = Enable auto-read from EEPROM upon reset | 1 |

## 5.1.3.2 Boot-up sequence

This section describes the boot procedure for the TNETW1100B in a P50 WLAN application. During the boot process the TNETW1100B loads configuration data from the serial EEPROM and the host PDA downloads firmware to the embedded ARM processor within the TNETW1100B. The sequence of events is as follows:

The host supplies the TNETW1100B by setting the WLAN_EN to high. The reset signal for TNETW1100B is generated from a simple RC circuit upon powering on the U702 LDO.

Upon reset, the TNETW1100B reads the configuration resistors on the MDATA bus and starts a burst read of configuration data from the EEPROM. The configuration

data includes the Card Information Structure (CIS). In embedded system, we disregarde this information since we don't need it.

The TNETW1100B starts to load the associated driver.

The PDA host starts to execute the TNETW1100B Windows NDIS driver for the enumerated TNETW1100B P50 module. The driver initialization process involves issuing a soft reset to the TNETW1100B and uploading a firmware binary file from the PDA into the TNETW1100B on-chip RAM.

After uploading the firmware file to the TNETW1100B the PDA host driver performs a checksum calculation on the firmware to verify its integrity and then the PDA host activates the TNETW1100B ARM processor and the TNETW1100B begins to execute the firmware.

The TNETW1100B firmware reactivates the TNETW1100B EEPROM hardware state machine and initiates a follow-on burst read of the EEPROM to load additional configuration data. One of the configuration parameters loaded during this burst read is a pointer to the location within the EEPROM of additional configuration data tables.

The TNETW1100B firmware then assumes control of the EEPROM interface and manually reads final configuration information from the data tables in the EEPROM.

This concludes the boot process and the systems enters its steady state operating mode.

## 5.1.4 Power Management

TNETW1100B supports Enhance Low Power (ELP) mode that includes two power saving states, the Doze state and the Deep Sleep state.

### 5.1.4.1 Doze State

The Doze state is equivalent to the 802.11 infrastructure power saving mode defined in the 802.11 standard. The STA enters and exits Doze state when instructed by the AP it is associated with. In the Doze state, the TNETW1100B turns off power to the majority of the chip. A clock and timer remain active to maintain timing for wake up interval. The STA wakes up periodically on a set (beacon) interval to check beacon from the AP. The sleep clock is provided using an external 32 KHz crystal oscillator.

The TNETW1100B saves additional power in the Doze state by turning off power

to external and internal components that are not used. In each case, the voltage regulator for the component is turned off via a TNETW1100B GPIO pin connected to the Enable pin of the regulator. That is, GPIO10 controls the Enable pin of the regulator for V_SYN and XOSC_EN_N for Analog 1.8V.

Table 1.2 shows some of the various power supplies for the TNETW1100B and other on board devices and their status in the Doze state.

A STA enters or exits the Doze mode by the instructions from an AP. Before entering Doze state, The Firmware powers down power supplies to the components that are not needed. When exiting, these power supplies are turned back on.