Theory of Operation

Gyration, Inc. Millennium Series GyroRemote
Model GP241-001

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The Millennium Series Gyro Remote consists of a 40 or 49 MHz (depending on country code) electrical assembly (including gyro) mounted in a compact ABS plastic remote control housing. A battery compartment (with slide-off cover) containing four AAA-sized alkaline cells is located in the underside of the handle portion of the housing. The top of the housing contains a number of illuminated translucent buttons with custom printed legends allowing for customized applications. Screen printed control buttons on either side of the top portion of the remote are not illuminated but still allow for further customization of operating functions per individual OEM requirements.

The pc board in the Gyro Remote consists of an 8-bit CPU (U2) with internal masked ROM memory and an external EEPROM (U6) surrounded by associated power supply and switch matrix scanning circuitry, plus an FSK RF transmitter. Information concerning motion originates with the gyro assembly (U5). The output from the gyro is processed by a custom ASIC (U3) and relayed via serial peripheral interface to the CPU. The RF transmitter consists of a dual PLL synthesizer (U1) and a 40/49 MHz VCO (Voltage Controlled Oscillator) (Q1, Q2) plus an RF output amplifier/filter section. The output from this transmitter is connected to a short end-loaded monopole antenna located at the top (away from user) end of the pc board.

The VCO consists of a varactor (D1) tuned Colpitts oscillator (Q1, L2, C3, C10) plus a buffer stage (Q2). Both Q1 and Q2 operate in the emitter follower configuration. The PLL synthesizer operates with a reference frequency determined by 10.24 MHz crystal Y1. The 10.24 MHz reference oscillator is frequency modulated by pulling the crystal frequency downward with a parallel capacitance (C14) switched in and out of circuit with a bipolar transistor (Q4). Q4 is in turn switched on and off at a rate corresponding to 4800 bits per second (bps) by the tx data output from the CPU. The RF signal generated by the VCO thus becomes modulated to a level of 2.4 KHz deviation, representing a minimum shift keying (MSK) condition for 4800 bps binary FSK signaling (BT = 0.5).

The 40/49 MHz VCO output at the emitter of Q2 branches off into two separate directions. The first branch (via C16) is sent back to the PLL in order to provide an output reference for frequency/phase comparison. The second branch (via C5) is sent onward to the RF output stage (Q3) and then on to the antenna via a matching network. The antenna matching network (consisting of L5, C20, C26, C17, C18 and C19) also functions as a transmitting filter to reduce the radiated harmonic output levels in order to meet emission limits imposed by government regulations.

The power supply section consists of a 4-cell (6 VDC) alkaline battery pack, a reverse polarity protection diode (D3), a fixed 4.0 VDC linear low-dropout regulator U4 (supply for CPU -- always on) and a fixed 3.3 VDC linear low-dropout regulator with external on/off control (U7). The 3.3V supply is used to power the VCO and PLL sections only and is shut off when the transmitter is not turned on. Low voltage detector U9 resets the CPU during conditions of insufficient pack voltage (about 1 V per cell), thus eliminating the possibility of out-of-spec transmitter operation at low battery voltages.