3 FUNCTIONAL DESCRIPTION

This section presents a functional description of the MDR-8000 series radios. The descriptive information covers the main functions of the radio, followed by a description of the modules. Module descriptions are to the functional block level to meet maintenance philosophy requirements. Engineering drawings referenced throughout the text are located in the Diagrams section of this manual. Prior to describing the radio itself, information about a typical MDR network is described.

3.1 MICROWAVE DIGITAL RADIO NETWORK DESCRIPTION

See Figure 3-1. Communication between microwave radio sites is by microwave links. These links are called hops and numbered sequentially. The link between the first and second site would be identified as Hop 1. The link between the second and third site would be identified as Hop 2, and so on. The following description deals with three sites identified as sites. The third site, site C, is also a terminal radio site comprised of one MDR.

At site A, the MDR comprises one transmitter (XMTR) and one receiver (RCVR). Site A can communicate with site B via a common RF XMT and RCV antenna in two directions commonly identified as eastbound and westbound traffic (arbitrary directions chosen to distinguish between two different but not necessarily opposite directions of transmission or reception of radio signals). The RF communication path between site A and site B is Hop 1.

At site B, there are two MDRs each comprising one XMTR and one RCVR. These radios can be located in the same rack on separate shelves or in separate racks. The radios communicate with each other, internal to the site, over connecting cable rather than by RF antenna. This configuration is called a repeater. In a repeater configuration, one MDR communicates with site A and the other MDR communicates with site C by means of RF XMT and RCV antennas. Again, the directions of communication are identified as eastbound and westbound traffic. The RF communication path between site B and site C is Hop 2.

At site C, the MDR comprises one transmitter (XMTR) and one receiver (RCVR). Site C can communicate with site B over a common RF XMT and RCV antenna in both eastbound and westbound traffic directions.

It should be noted that input and output to and from site B can also be Drop and/or Insert traffic via customer furnished equipment (CFE) in addition to the normal eastbound/westbound payload traffic. Drop is the process and/or point at which transmitted information is removed or diverted from the normal channel path by CFE prior to reaching the terminal site. Insert: is the process and/or point at which desired information is inserted by CFE as opposed to the normal XMT or RCV modules for transmission to the next site.

F1, F2, F3, and F4 represent the frequencies transmitted and received by the specific radio transmitters and receivers.

3.2 MDR-8000 MAIN FUNCTIONS

See Figure 3-2 through Figure 3-12.

3.2.1 Transmit

In the transmit direction, the MDR-8000 uses a modulation structure where the I and Q baseband signals modulate the in-phase and quadrature phase components of the transmitter.

3.2.1.1 Simplex Non-standby Transmitter Signal Flow

The simplex non-standby configuration consists of one unprotected transmitter connected to a single antenna through a standard XMT filter. The basic signal path for DS1/E1 and DS3 radios is from the LBO to the I/O Interface to the XMTR to the XMT Filter and out the Transmit/Receive Antenna. The digital signal input (DS1/E1 or DS3) from the customer cross-connect equipment, or a wayside source, is fed to the radio LBO. The LBO, comprised of resistors, inductors, and capacitors, electrically simulates a transmission line length and achieves impedance matching between the cross-connect equipment and the radio. The digital signals are split into two equal inputs and are transformer coupled to the radio input/output interface (I/O interface). The I/O interface converts these digital input signals to I and Q quadrature signals.

In the OC3 radio, optical input signals from the customer cross-connect equipment go directly to the OC3 I/O interface. This interface converts the optical signals into electrical baseband I and Q signals.

The I and Q signals of all configurations go to the XMTR module for digital to analog conversion and frequency multiplication. The final output is an RF signal of the desired transmit frequency. The RF signal goes either to an optional power amplifier or directly to the transmitter filter. From the filter, the RF goes to the antenna or in a split package radio, to the outdoor unit for further frequency multiplying and then to the antenna for over the air transmission.

3.2.2 Receive

In the receive direction, the MDR-8000 uses a demodulation conversion structure. The received TCM or QAM RF signal is fed into a filter followed by a receiver module. The receiver module directly converts the RF signal to I and Q baseband signals and provides all of the acquisition loops. The receiver also provides countermeasures to dynamic path distortions. Clock and digital data are extracted from the analog channels and passed on to the I/O interface. The digital data is processed by the I/O interface module and converted to a DS1/E1 or DS3 format.

3.2.2.1 Simplex Non-standby Receiver Signal Flow

This configuration consists of one unprotected receiver connected to a single antenna through a standard RCVR filter. The received RF signal from the antenna is sent to the receiver filter (in the split package configuration, to the ODU for frequency down-conversion and then to the receive filter) and on to the receiver module. In the receiver module the RF signal is frequency down-converted, de-multiplexed into quadrature I and Q baseband signals, and sent to the I/O interface for conversion into DS1/E1 or DS3 signals. The customer's cross connect equipment or to DS1 wayside equipment.

3.2.3 Signal Paths In Other Than Simplex Radios

When dealing with hot-standby, frequency diversity, space-diversity, etc. configurations, the basic signal flow throughout the radio components is the same. The difference is in the on/off conditions of the specific transmitter/receiver channels. See descriptions of the different configurations in the following paragraphs of this section.

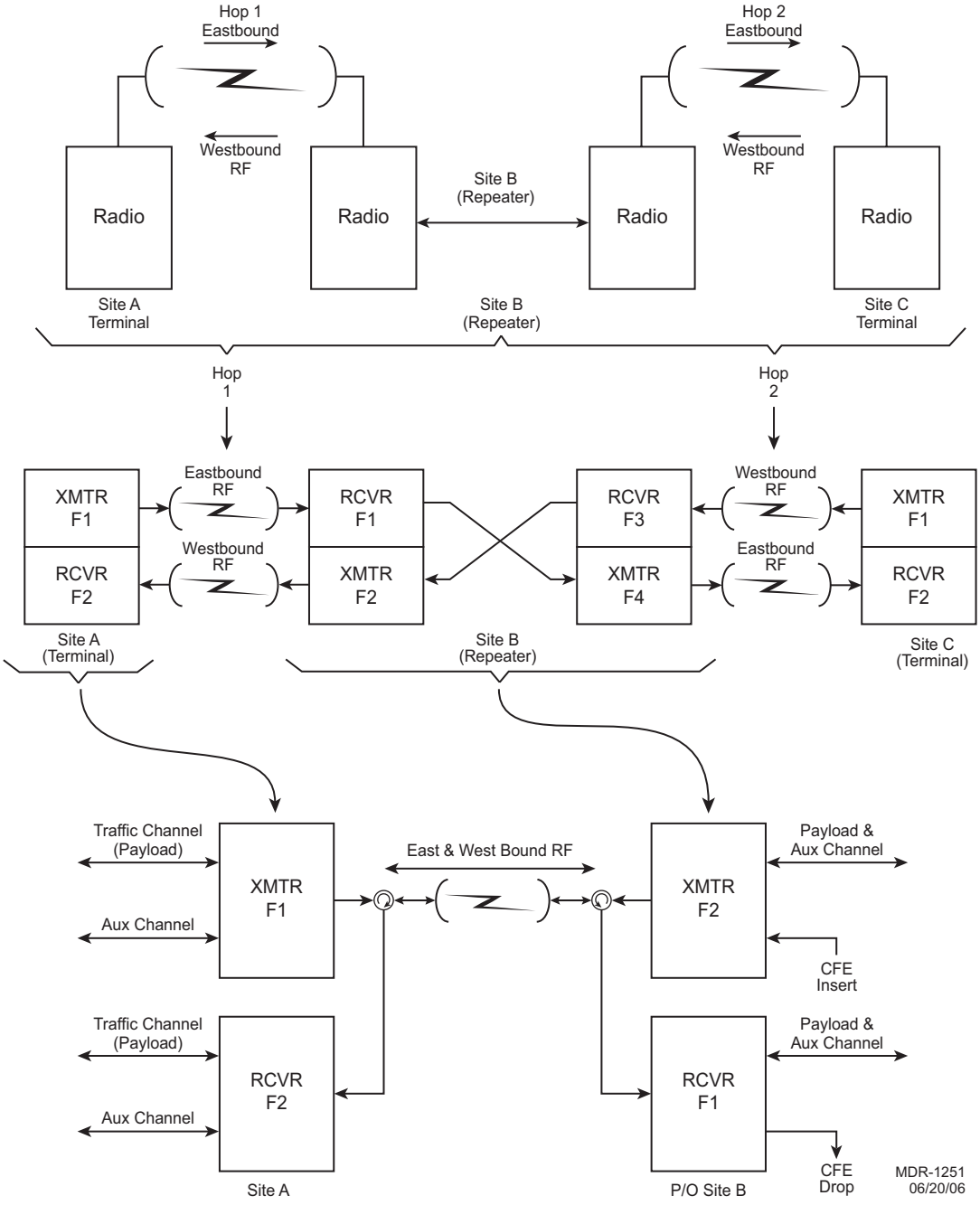


Figure 3-1 MDR Network Description

3.3 MDR-8000 MAIN FUNCTIONS

See Figure 3-2 through Figure 3-8. In the transmit direction, the MDR-8000 uses a modulation structure where the I and Q baseband signals modulate the in-phase and quadrature phase components of the transmitter.

The DS1/E1 I/O interface converts the format of the incoming DS1/E1 data streams to I, Q, data, and clock. The DS1/E1 I/O interface module uses the DS1/E1 signals to generate 32 or 128 trellis code amplitude modulated (TCM) baseband signals The transmitter processes the TCM baseband signals to generate the modulated TCM RF signal. The RF signal is then amplified and applied directly to the antenna branching or further amplified by a solid-state amplifier (optional) and applied to the antenna branching.

The DS3 I/O interface converts the format of the incoming DS3 and Wayside (WS) DS1 data streams to I, Q, data, and clock. The I/O interface module uses the DS3 signals to generate 64 Quadrature Amplitude Modulated (QAM) baseband signals. The transmitter processes the QAM baseband signals to generate the modulated QAM RF signal. The RF signal is then amplified and applied directly to the antenna branching or further amplified by a solid-state amplifier (optional) and applied to the antenna branching.

In the receive direction, the MDR-8000 uses a demodulation conversion structure. The received TCM or QAM RF signal is fed into a filter followed by a receiver module. The receiver module directly converts the RF signal to I and Q baseband signals and provides all of the acquisition loops. The receiver also provides countermeasures to dynamic path distortions. Clock and digital data are extracted from the analog channels and passed on to the I/O interface. The digital data is processed by the I/O interface module and converted to a DS1/E1 or DS3 format.

The MDR-8000 consists of I/O, transmit, receive, control and monitor, and power distribution subsystems. An overview of these functions followed by detailed functional descriptions of the modules that comprise each subsystem follows.

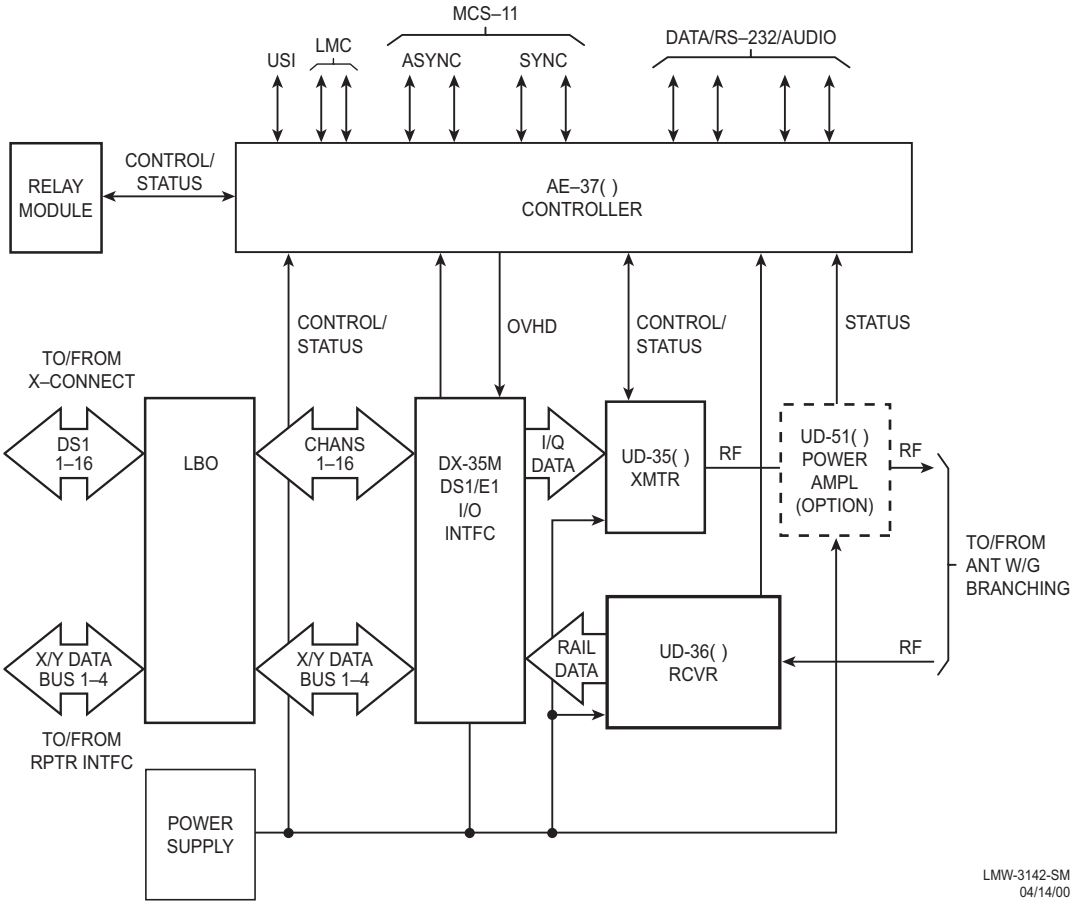


Figure 3-2 Typical DS1/E1 Non-Standby Radio Functional Block Diagram

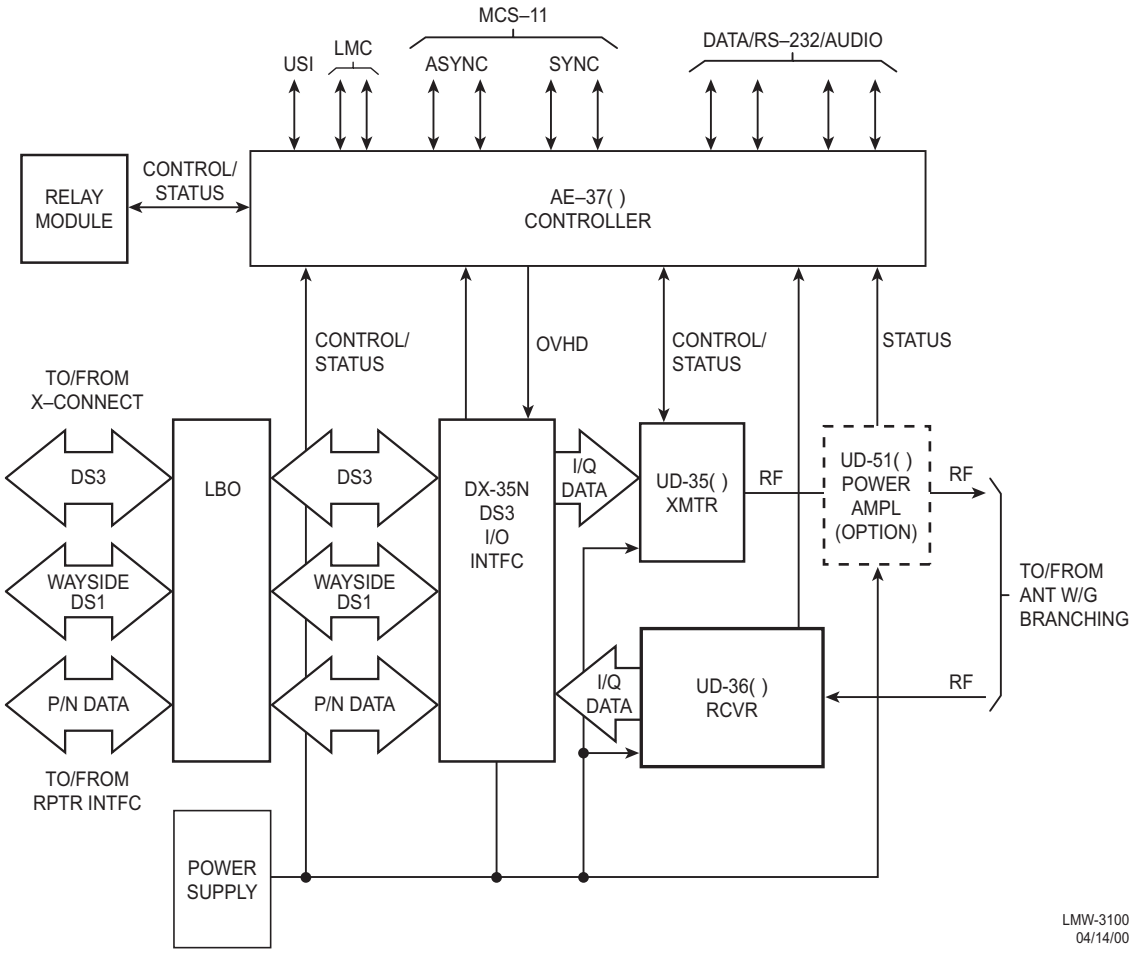


Figure 3-3 Typical DS3 Non-Standby Radio Functional Block Diagram

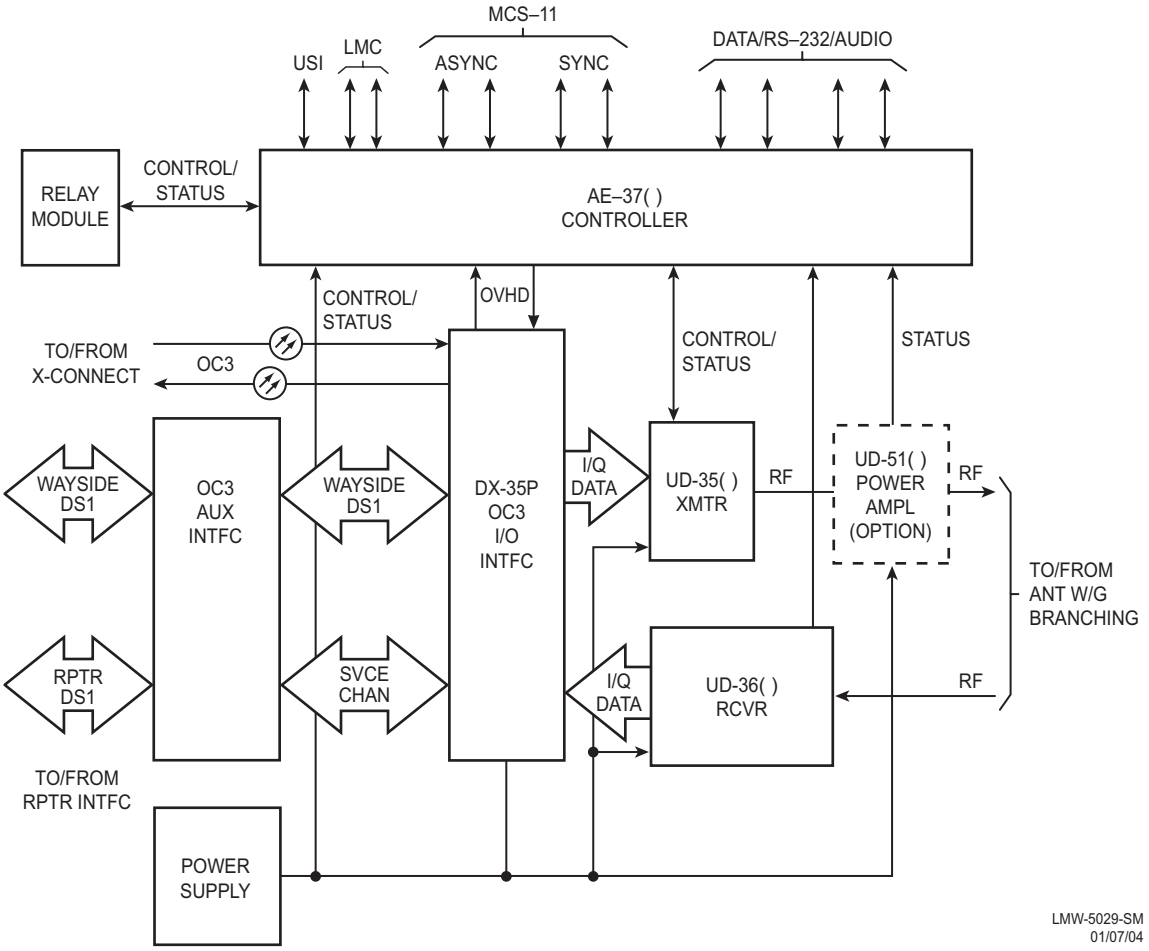
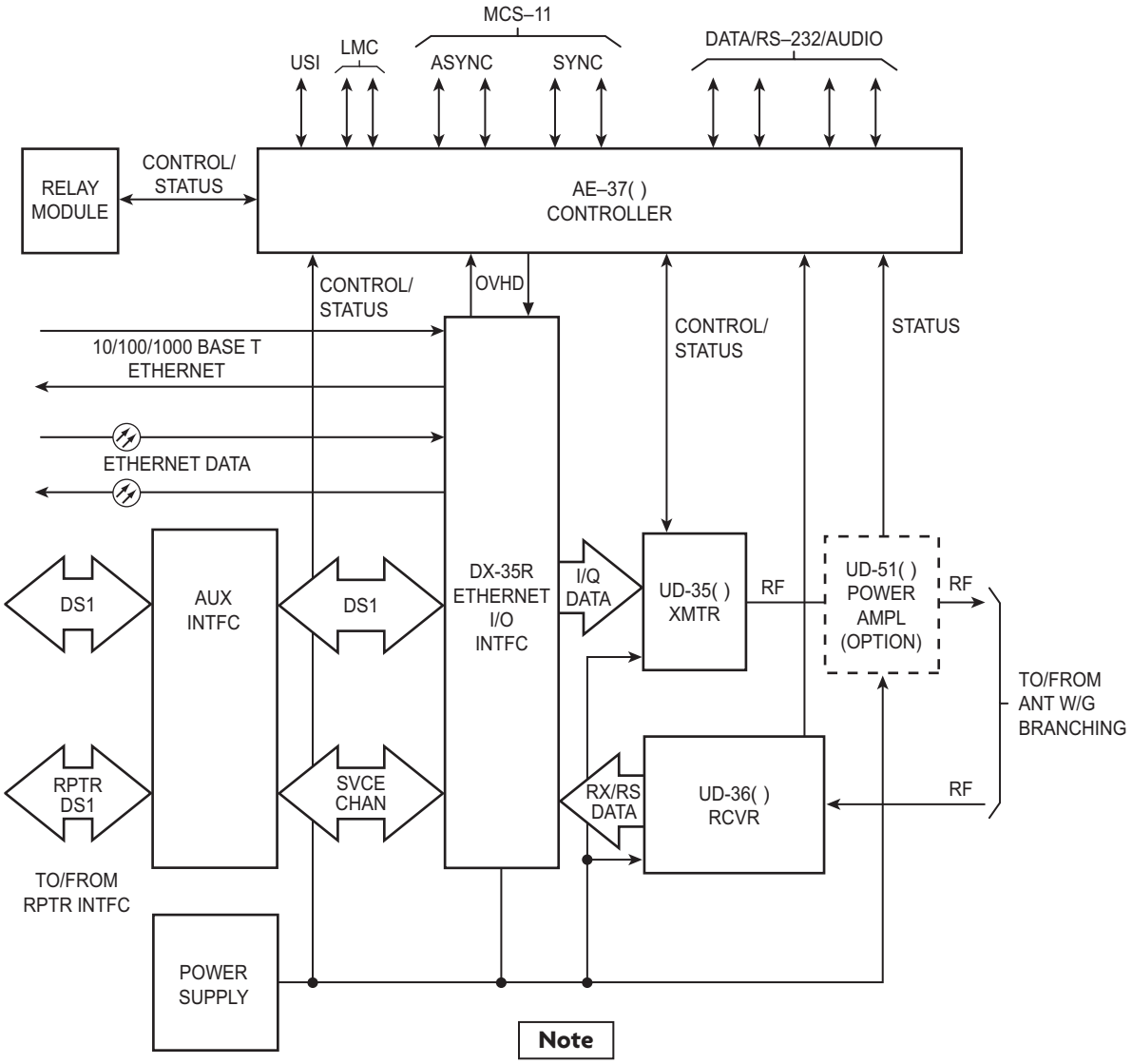


Figure 3-4 Typical OC3/STM-1 Non-Standby Radio Functional Block Diagram



Ethernet interface can be electrical or optical.

Figure 3-5 Typical Ethernet Non-Standby Radio Functional Block Diagram

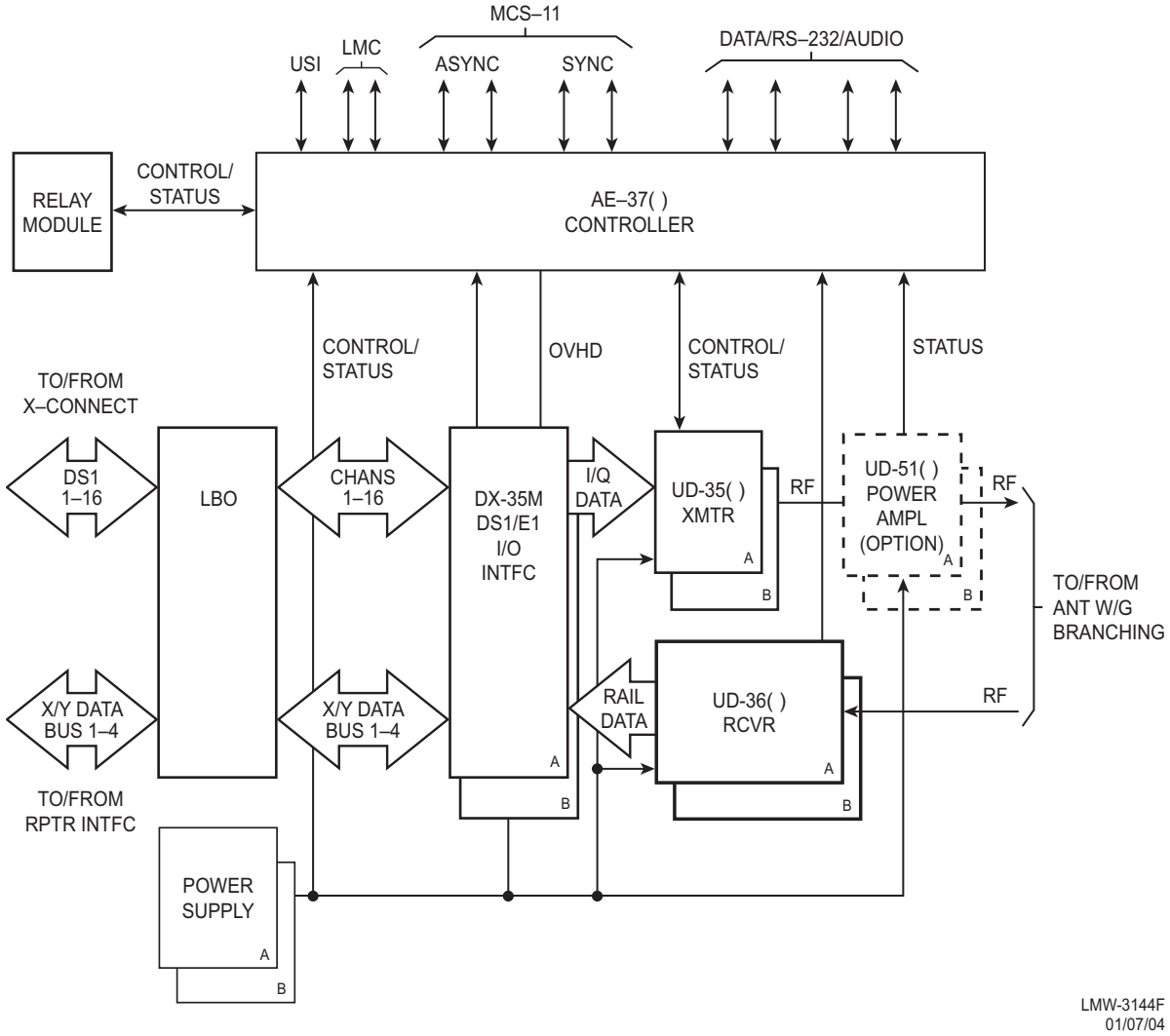


Figure 3-6 Typical DS1/E1 Hot-Standby Radio Functional Block Diagram

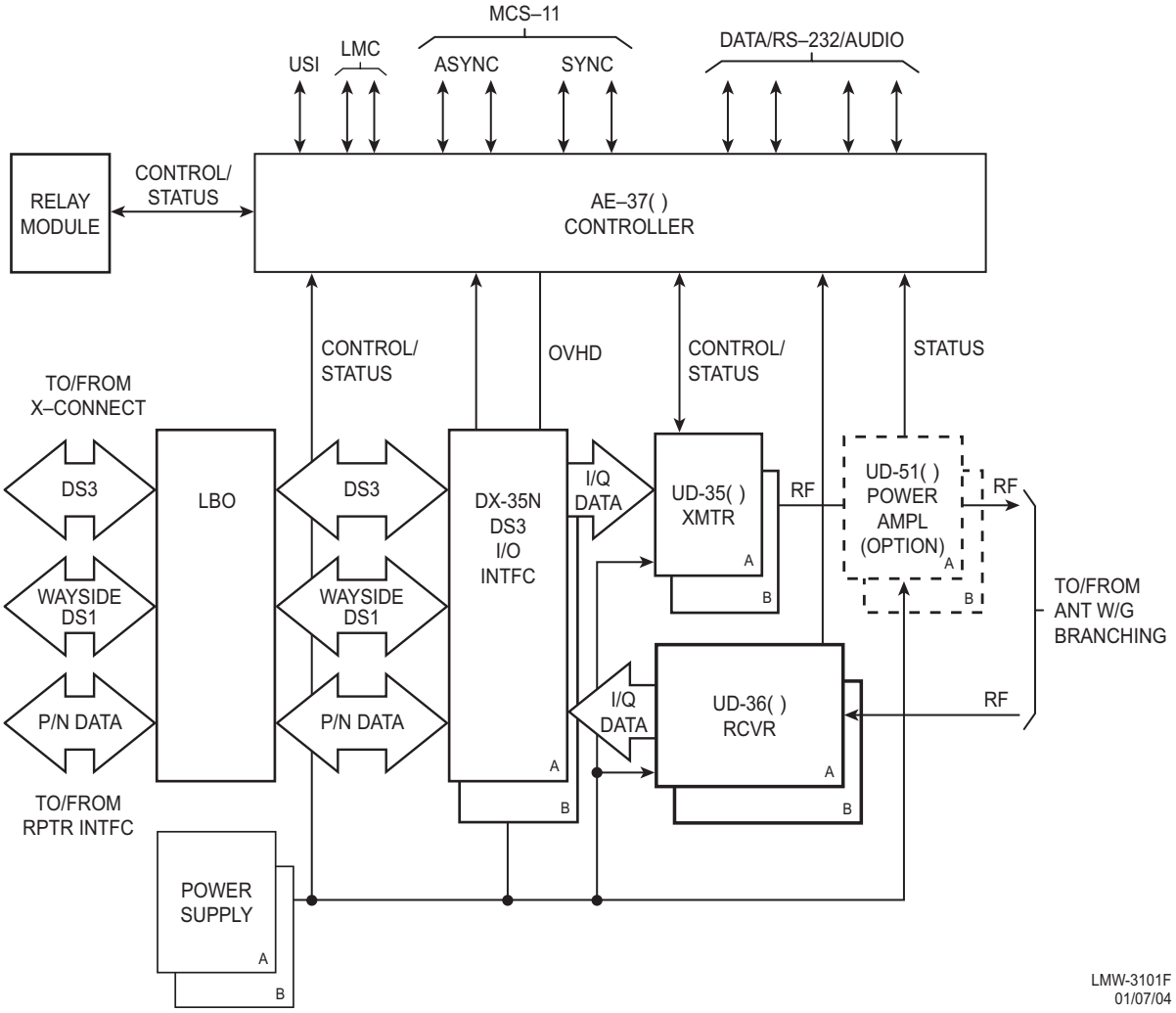


Figure 3-7 Typical DS3 Hot-Standby Radio Functional Block Diagram

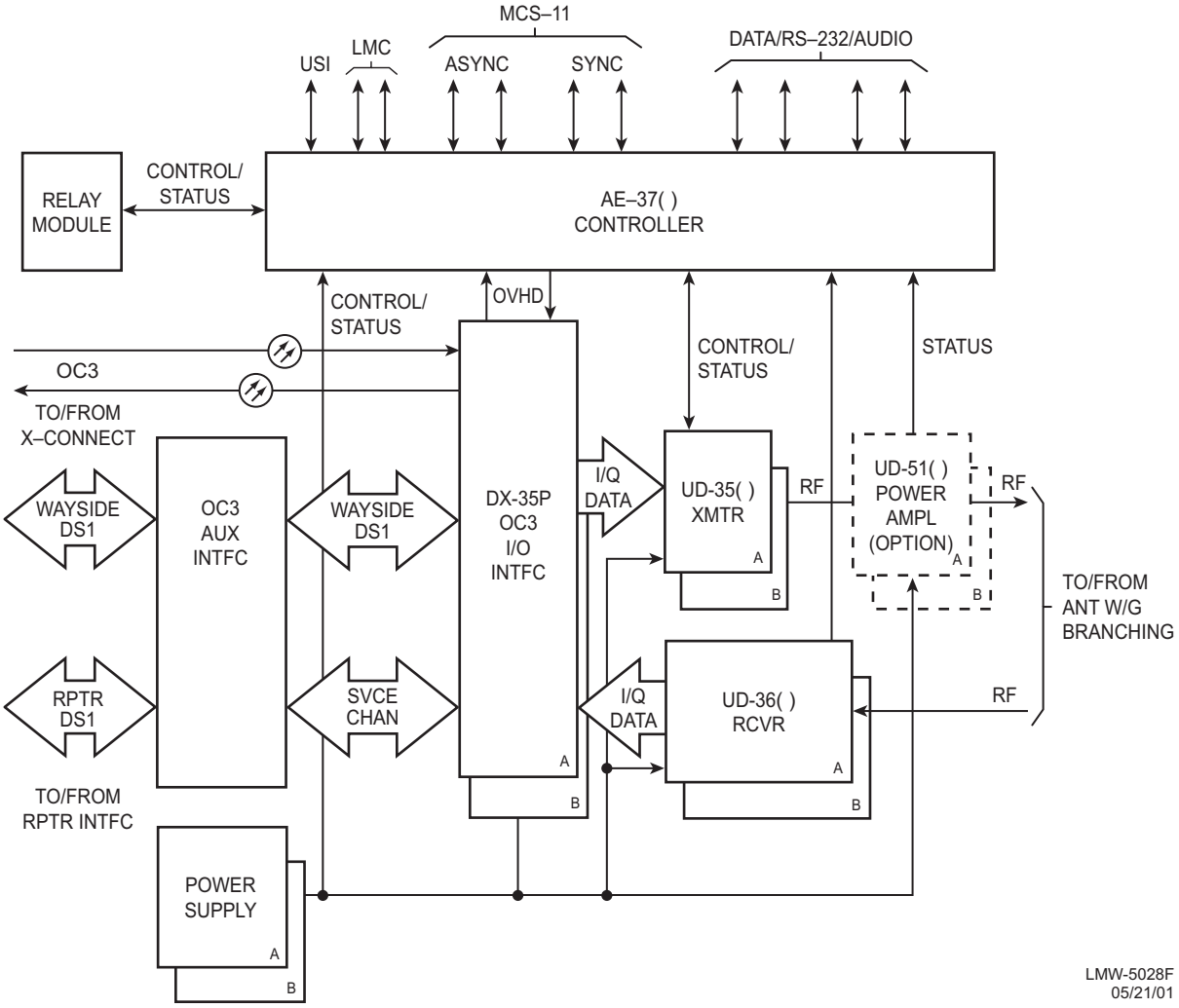


Figure 3-8 Typical OC3/STM-1 Hot-Standby Radio Functional Block Diagram

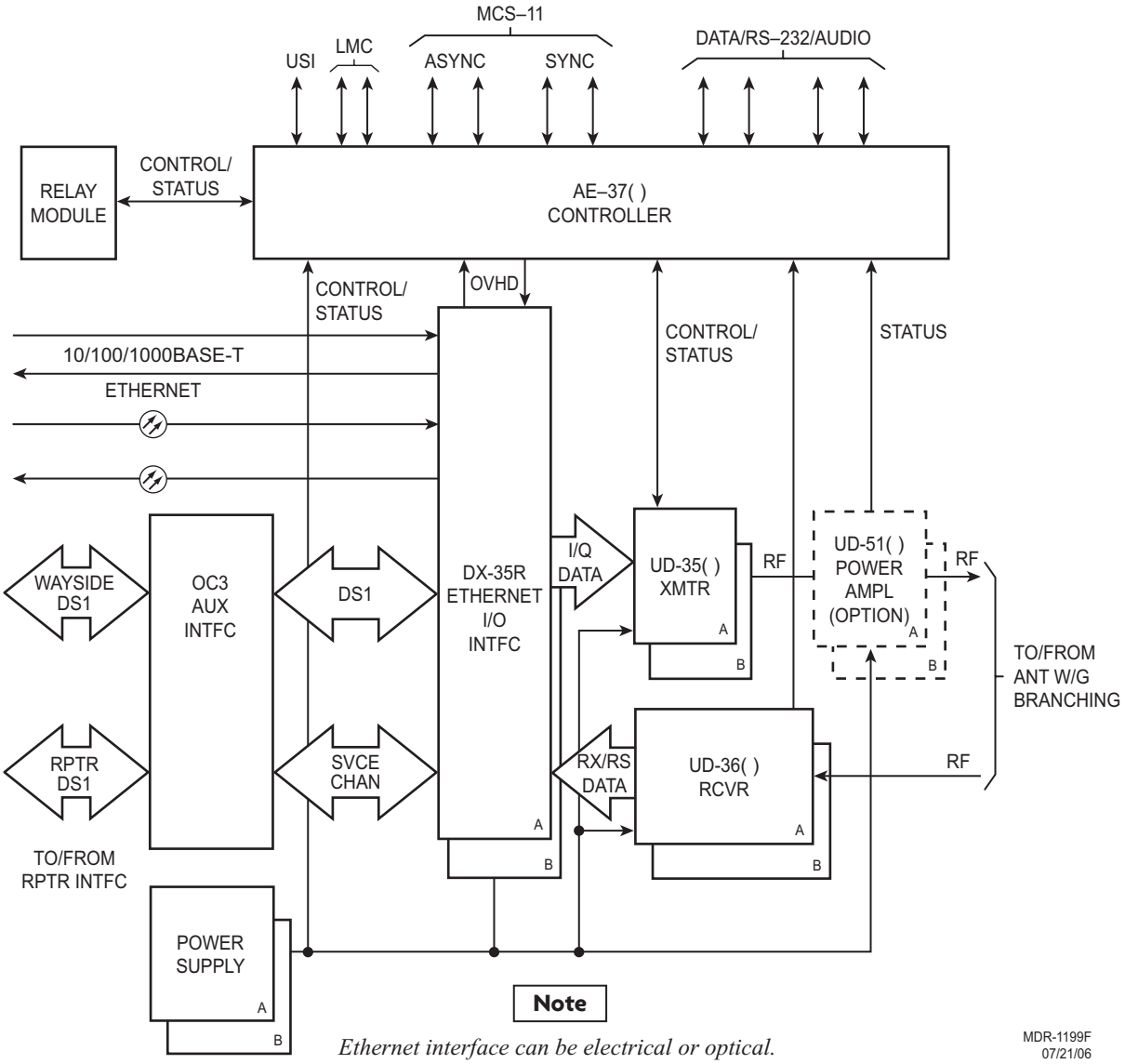


Figure 3-9 Typical Ethernet Hot-Standby Radio Functional Block Diagram

3.4 I/O SUBSYSTEM FUNCTIONAL DESCRIPTION

See Figure 3-10, Figure 3-11, Figure 3-12 and Figure 3-13. The DS1/E1 and DS3 I/O subsystem consists of the DS1/E1 and DS3 LBO and I/O interface modules. The OC3/STM-1 I/O subsystem consists of the OC3/STM-1 AUX interface board and I/O interface modules. The I/O subsystem interfaces the XMT and RCV and monitor and control subsystems. The DS1, E1, and DS3 I/O subsystem converts digital signals into a data stream and multiplexes this data with overhead data. The OC3/STM-1 I/O subsystem converts OC3/STM-1 optical signals to digital signals and multiplexes this data with overhead data. Multiplexed data is demultiplexed to separate the overhead data from the data stream.

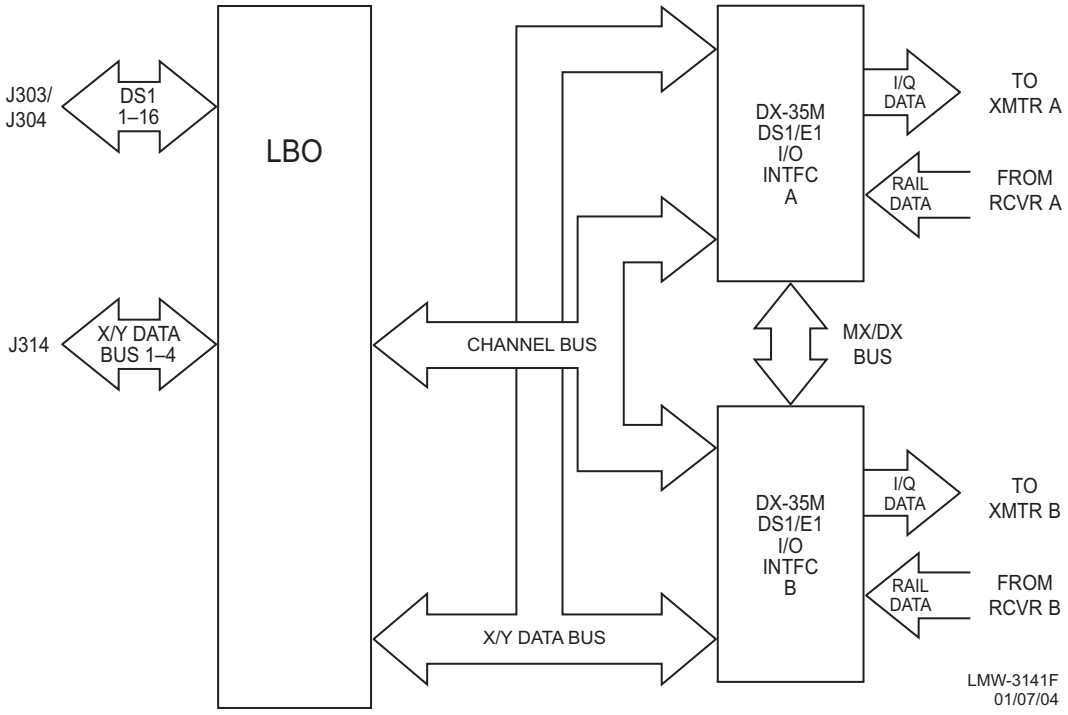


Figure 3-10 DS1/E1 I/O Function Block Diagram

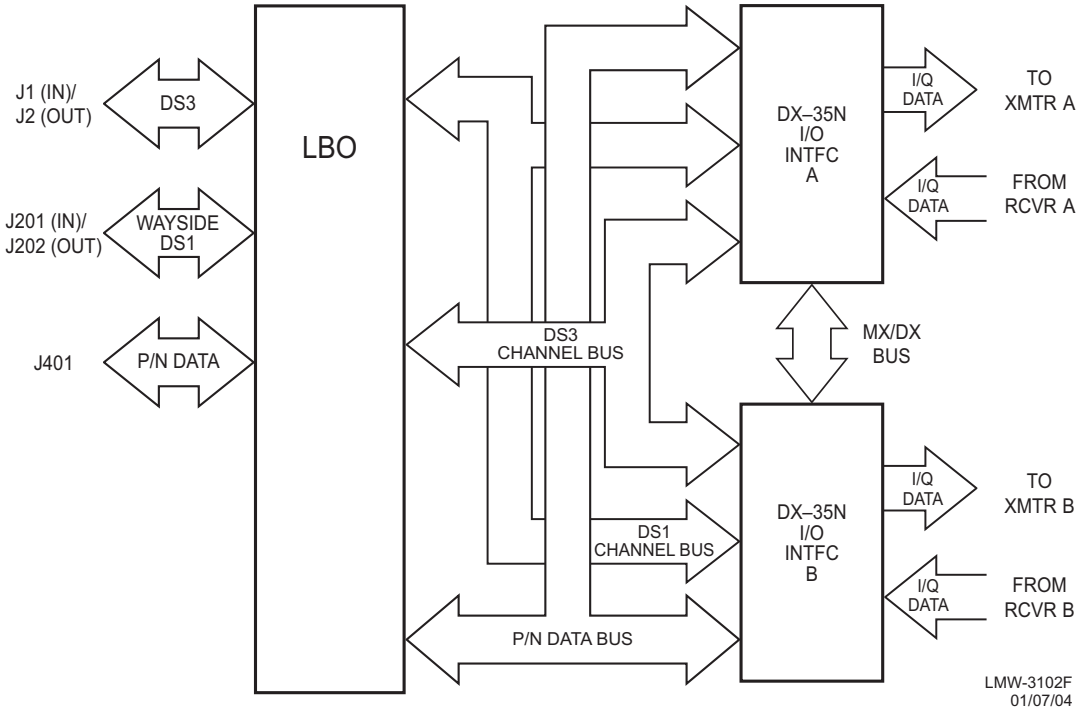


Figure 3-11 DS3 I/O Functional Block Diagram

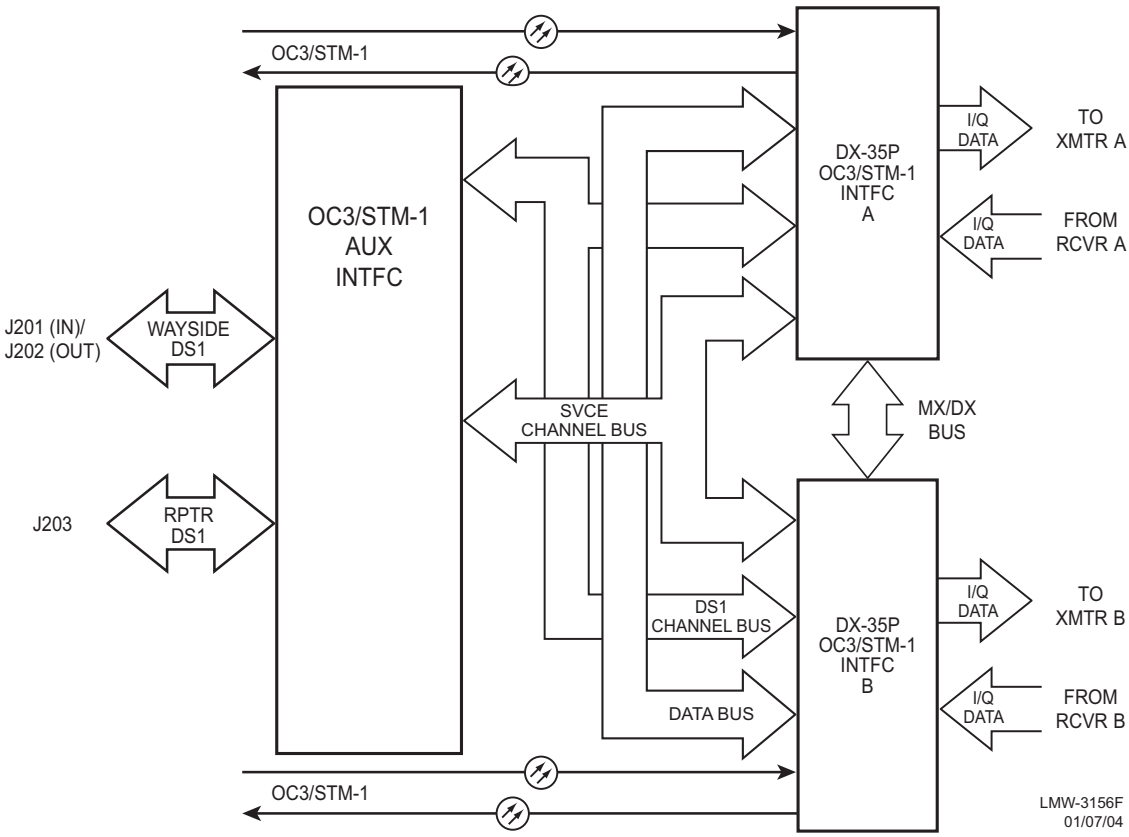


Figure 3-12 OC3/STM-1 I/O Functional Block Diagram

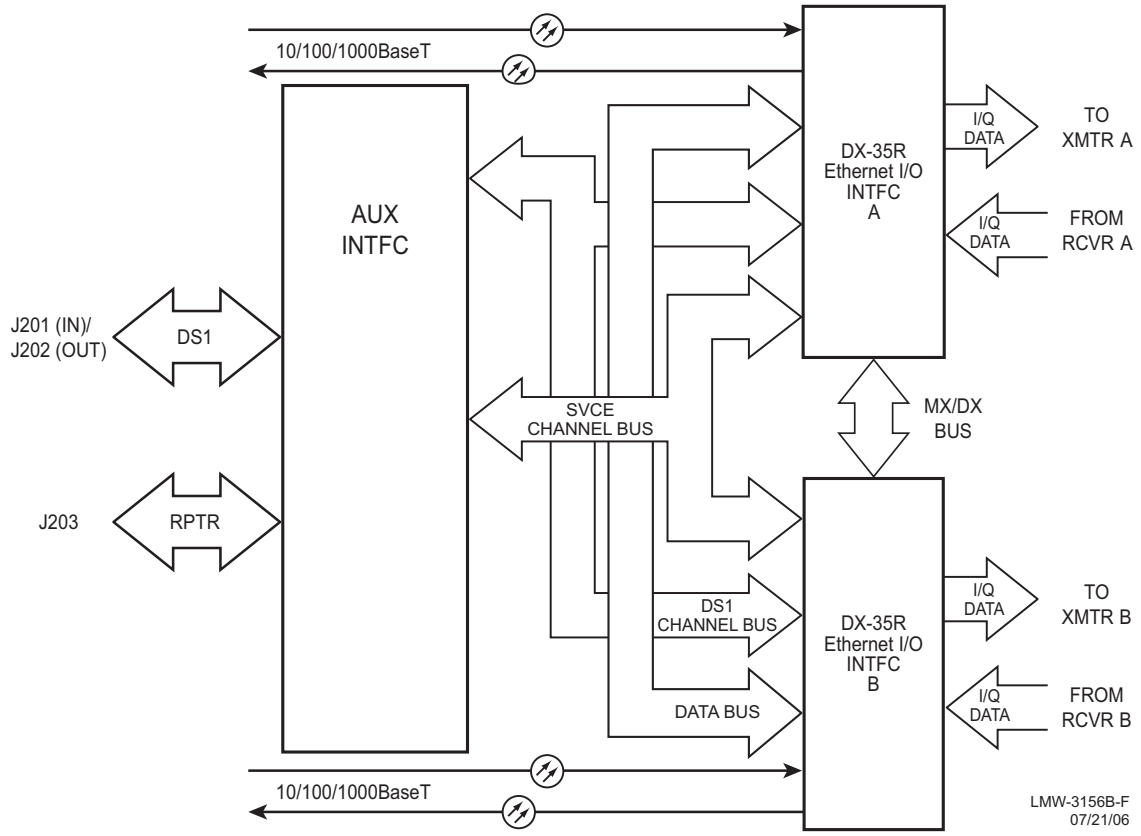


Figure 3-13 Ethernet I/O Functional Block Diagram

3.4.1 I/O Transmit Signal Flow

3.4.1.1 DS1/E1 Radio

Digital signals are routed from the DS1 cross-connect/E1 interface to the LBO. The incoming DS1/E1 signals are transformer coupled to a splitter/termination. The splitter terminates the balanced signals and converts them to unbalanced P and N signals. These signals are connected to the A and B I/O Interface cards. The I/O interface cards multiplex up to 16 DS1/E1 input signals with overhead into a data stream. If the radio is being used as a repeater (repeater cable is connected to J314), data on the X/Y data bus is also multiplexed into the data stream. This data stream is converted into XY rail data and then multiplexed into I/Q data rails (digital baseband).

3.4.1.2 DS3 Radio

Digital signals are routed from the DS3 cross-connect to the LBO. The incoming DS3 signals are transformer coupled to a splitter/termination. The splitter terminates the balanced signals and converts them to unbalanced P and N signals. These signals are connected to the A and B I/O Interface cards. If wayside DS1 is desired, digital signals are routed from the DS1 cross-connect to the LBO. The incoming wayside DS1 signals are transformer coupled to a

DS1 splitter/termination. The DS1 splitter terminates the balanced signals and converts them to unbalanced P and N signals that are connected to the A and B I/O Interface cards. The I/O interface cards multiplex one or three DS3 and WS DS1 signals with overhead into a data stream. If the radio is being used as a repeater (repeater cable is connected to J401), data on the X/Y data bus is also multiplexed into the data stream. This data stream is converted into XY rail data and then multiplexed into I/Q data rails (digital baseband).

3.4.1.3 OC3/STM-1 Radio

Optical signals are routed from the fiber optic interface to the A and B I/O Interface cards. If wayside DS1 is desired, digital signals are routed from the DS1 cross-connect to the aux board. The wayside DS1 signals are connected to the A and B I/O Interface cards. The I/O interface cards convert the optical signal to digital signal and multiplex the digital signal and WS DS1 signals with overhead into a data stream. If the radio is being used as a repeater (repeater cable is connected to J401), data on the X/Y data bus is also multiplexed into the data stream. This data stream is converted into XY rail data and then multiplexed into I/Q data rails (digital baseband).

3.4.1.4 Ethernet Radio

The Ethernet radio I/O subsystem is populated with the OC3 AUX Interface board and one or two DX-35R-1 or -2 ETH I/O Interface modules for Ethernet software releases prior to R2.0 and the line interface card and one or two DX-35S-1 ETH/T1 I/O modules for release following R2.0. The following paragraphs describe both versions of I/O subsystems.

3.4.1.4.1 I/O Prior to R2.0

The DX-35R-1 I/O interface module accepts electrical 10/100/1000 Base-T ETH signals. The DX-35R-2 I/O Interface module accepts optical or electrical 10/100/1000 Base-T ETH signals. Optical ETH signals are converted to ETH electrical signals using an SFP (Small Form-factor Pluggable), a compact optical XCVR connected to the fiber optic cable.

In the ETH RCV/Radio XMT direction, the I/O interface module processes and multiplexes the incoming ETH signals with up to four (4) DS1 and service channel signals to provide an I/Q baseband data output to the XMTR module(s). The XMTR module(s) convert the digital baseband signal to a modulated TCM RF signal that can be further amplified by the Power Amplifier module(s) (if equipped) or applied directly to the antenna.

3.4.1.4.2 I/O After R2.0

The DX-35S-1 ETH/T1 I/O module accepts optical and electrical 10/100/1000 Base-T ETH signals. Optical ETH signals are converted to ETH electrical signals using an SFP (Small Form-factor Pluggable), a compact optical XCVR connected to the fiber optic cable.

In the ETH RCV/Radio XMT direction, the ETH/T1 I/O module processes and multiplexes the incoming ETH signals with up to 32 T1 and service channel signals to provide an I/Q baseband data output to the XMTR module(s). The XMTR module(s) convert the digital baseband signal to a modulated TCM RF signal that can be further amplified by the Power Amplifier module(s) (if equipped) or applied directly to the antenna.

3.4.1.5 Overhead

The transmitted overhead data consists of three 64 kb/s service channels and one 64 kb/s extended link monitor channel (ELMC). Each service channel contains multiplexed telephone, ELMC, MCS-11/TBOS alarm and control data, RS-232 serial data, and audio signals.

3.4.2 I/O Receive Signal Flow

3.4.2.1 DS1/E1 Radio

In the I/O interface, the digital rails received from the RCVR are demultiplexed to separate the overhead data from the traffic. The I/Q rails are demultiplexed to produce an XY rail data stream that is converted and demultiplexed to provide overhead and up to 16 DS1/E1 outputs.

3.4.2.2 DS3 Radio

In the I/O interface, the digital rails received from the RCVR are demultiplexed to separate the overhead data from the traffic. The I/Q rails are demultiplexed to produce an XY rail data stream that is converted and demultiplexed to provide overhead, up to three DS3 outputs and up to three wayside DS1 outputs.

3.4.2.3 OC3/STM-1 Radio

In the I/O interface, the digital rails received from the RCVR are demultiplexed to separate the overhead data from the traffic. The I/Q rails are demultiplexed to produce an XY rail data stream that is converted and demultiplexed to provide overhead, OC3/STM-1 optical output, and up to three wayside DS1 outputs.

3.4.2.4 Ethernet Radio

The Ethernet radio I/O subsystem is populated with the OC3 AUX interface board and one or two DX-35R-1 or -2 ETH I/O interface modules for Ethernet software releases prior to R2.0 and the ETH/T1 Line interface card and one or two DX-35S-1 ETH/T1 I/O modules for releases following R2.0. The following paragraphs describe both versions of I/O subsystems.

3.4.2.4.1 I/O Prior to R2.0

In the Radio RCV/ETH XMT direction, the TCM RF signal from the antenna is converted to demodulated R and S baseband data in the RCVR module(s) and applied to the I/O interface module(s). The I/O interface module(s) process and demultiplex the baseband to provide electrical ETH, DS1, and service channel outputs to the OC3 AUX interface board.

3.4.2.4.2 I/O After R2.0

In the Radio RCV/ETH XMT direction, the TCM RF signal from the antenna is converted to demodulated R and S baseband data in the RCVR module(s) and applied to the ETH/T1 I/O module(s). The ETH/T1 I/O module(s) process and demultiplex the baseband to provide electrical ETH, T1, and service channel outputs to the line interface card.

3.4.2.5 Overhead

The overhead data stream is demultiplexed to provide three 64 kb/s service channels and one 64 kb/s ELMC channel. Each service channel is demultiplexed to provide telephone, ELMC, MCS-11/TBOS alarm and control data, RS-232 serial data, and audio signals.

3.5 I/O SUBSYSTEM MODULES

Modules are described to the functional block diagram level in the following paragraphs. Modules are described in transmit signal flow order.

3.5.1 DS1/E1 LBO

Refer to Table 3-1 for LBO options. The MDR-8000/i/s can be equipped with an XMT LBO to interface DS1 or E1 data rates. The LBO compensates for the distance to the cross-connect for DS1 requirements or compensates for 12 dB cable loss (maximum allowed) between the radio and customer connection point to meet E1 requirements. See Figure 3-14 for application information.

Table 3-1 LBO Options

MODULE/DESCRIPTION	PART NUMBER	APPLICATIONS
LBO (domestic) 0-330 ft. (near)	3DH 03144 AA	Linear/Ring
LBO (domestic) 330-650 ft. (far)	3DH 03144 AB	Linear/Ring
LBO (international) (near)	3DH 03144 AC	Linear/Ring

3.5.1.1 XMT Circuit (DS1/E1 Line RCVR)

See Figure 3-15 for functional block diagram. The transformer couples the DS1/E1 Multiplex Tip/Ring (DS1/E1 MX T/R) signals at J303 to DX-35( ) I/O Interface A (via connector A3D), and B (via connector B3D) if the system is hot-standby.

3.5.1.2 RCV Circuit (DS1/E1 Line Driver)

The demultiplexed signals from the DX-35( ) I/O Interface module(s) are transformer coupled to the LBO circuit. The LBO circuit simulates lengths of twisted-pair cable to meet cross-connect requirements. The LBO conditions up to 16 DS1/E1 lines. The balanced output is applied to the DS1 cross-connect or E1 interface via connector J304.

3.5.1.3 Repeater Signal Distribution

The DS1/E1 LBO distributes repeater data (XMT and RCV X/Y DATA T/F 1-4) between RPTR connector J314 and the A and B I/O interface modules.

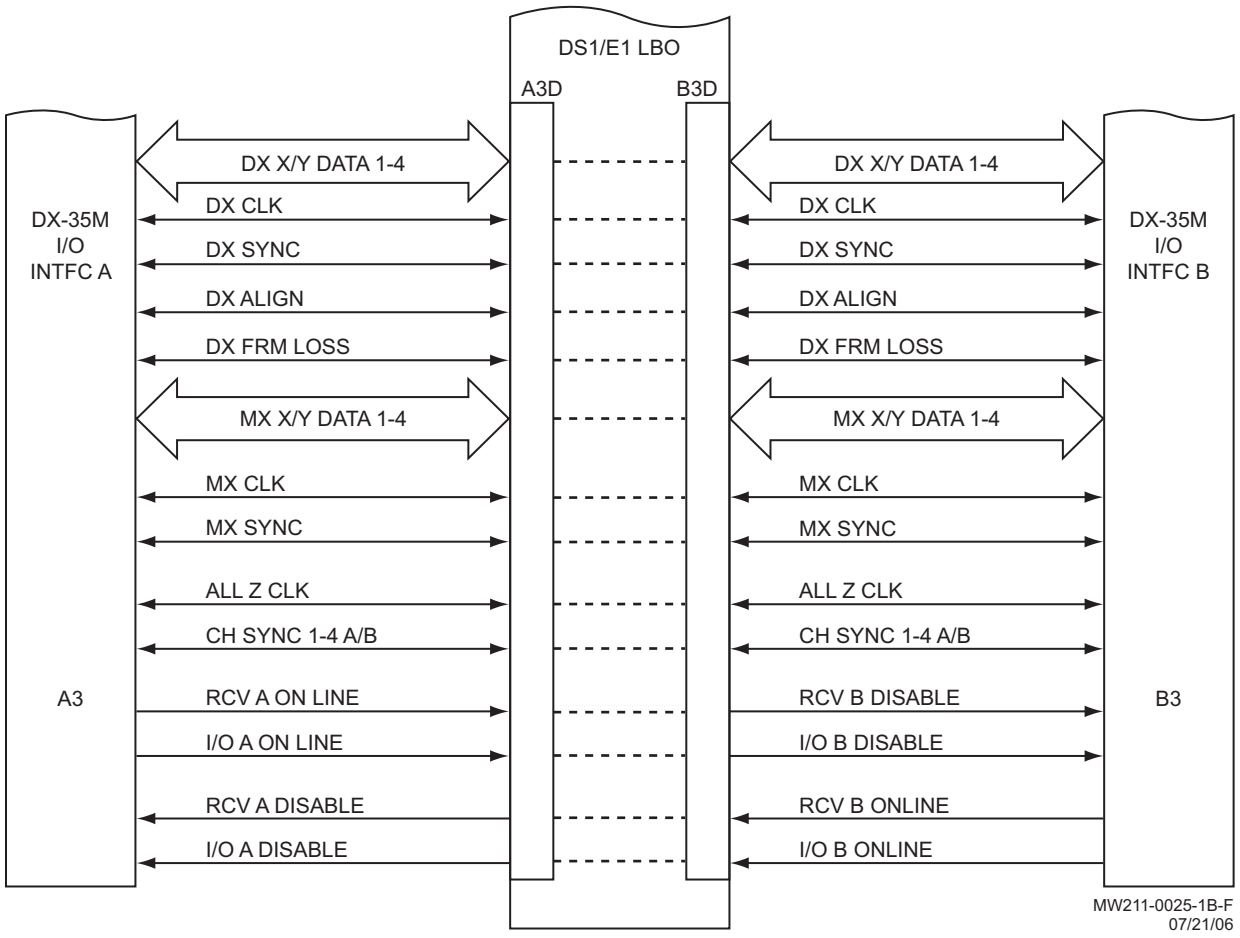


Figure 3-14 DS1/E1 LBO Interconnect Diagram (Sheet 1 of 2)

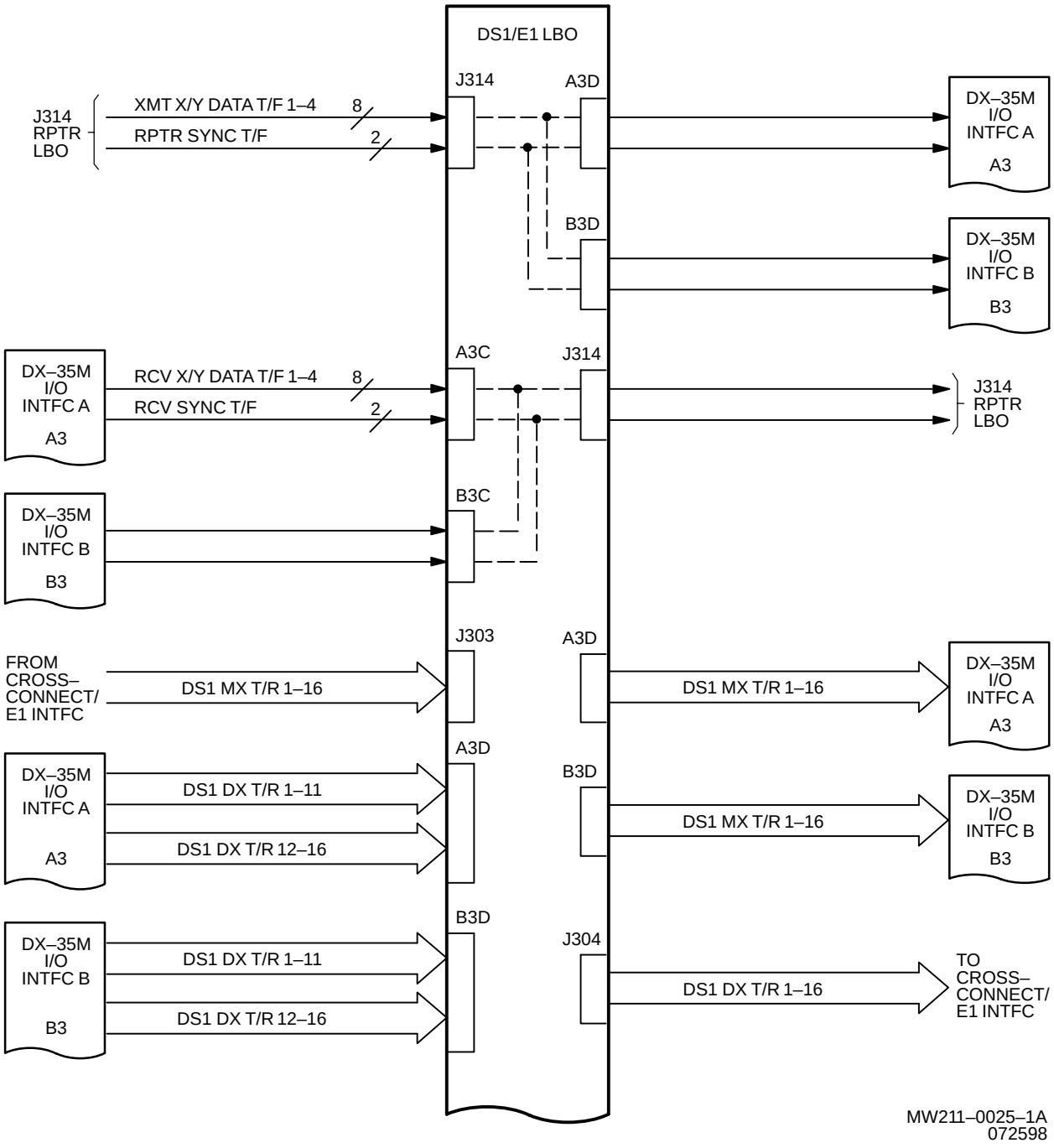


Figure 3-14 DS1/E1 LBO Interconnect Diagram (Sheet 2 of 2)

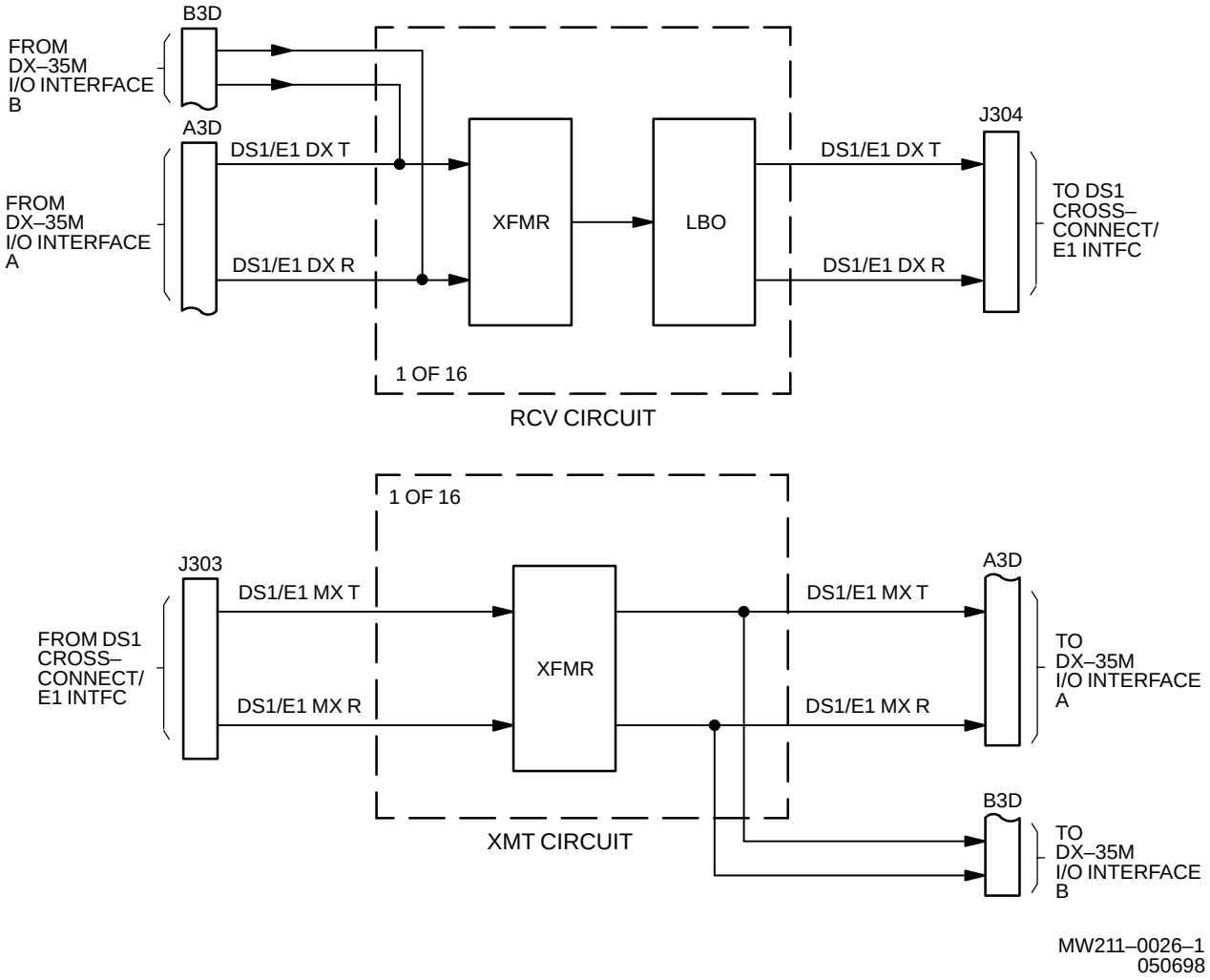


Figure 3-15 DS1/E1 LBO Functional Block Diagram

3.5.2 DS3 LBO

The MDR-8000 is equipped with an XMT LBO to interface DS3 data rates and wayside DS1 data rates. The LBO compensates for the distance to the cross-connect for DS3 requirements. See Figure 3-17 for to/from signal information and application information.

The DS3 LBO functions in non-standby and hot-standby configurations. In non-standby configurations, Only the A-side is used. Sides A and B are used for hot-standby. One side is on-line. The off-line side remains in standby mode until the on-line side fails.

The DS3 LBO contains three identical XMT and RCV circuits. Only one circuit (line 1) is shown and described. The functional block diagram and description for lines 2 and 3 are the same as line 1.

3.5.2.1 Strapping

FAR position straps are provided to bypass the LBO circuits and pass the signals without delay. NEAR straps are provided to delay the circuit. Straps are changed manually and are not software controlled.

3.5.2.2 DS3 XMT Circuit

See Figure 3-16 for functional block diagram. The transformer couples the DS3 Multiplex Tip/Ring (DS3 MX T/R) signals at J2 to DX-35N I/O Interface A (via connector A3C), and B (via connector B3C) if the system is hot-standby.

3.5.2.3 Wayside DS1 XMT Circuit

The transformer couples the wayside DS1 Multiplex Tip/Ring (WDS1 MX T/R) signals at J201 to DX-35N DS3 I/O Interface A (via connector A3D), and B (via connector B3D) if the system is hot-standby.

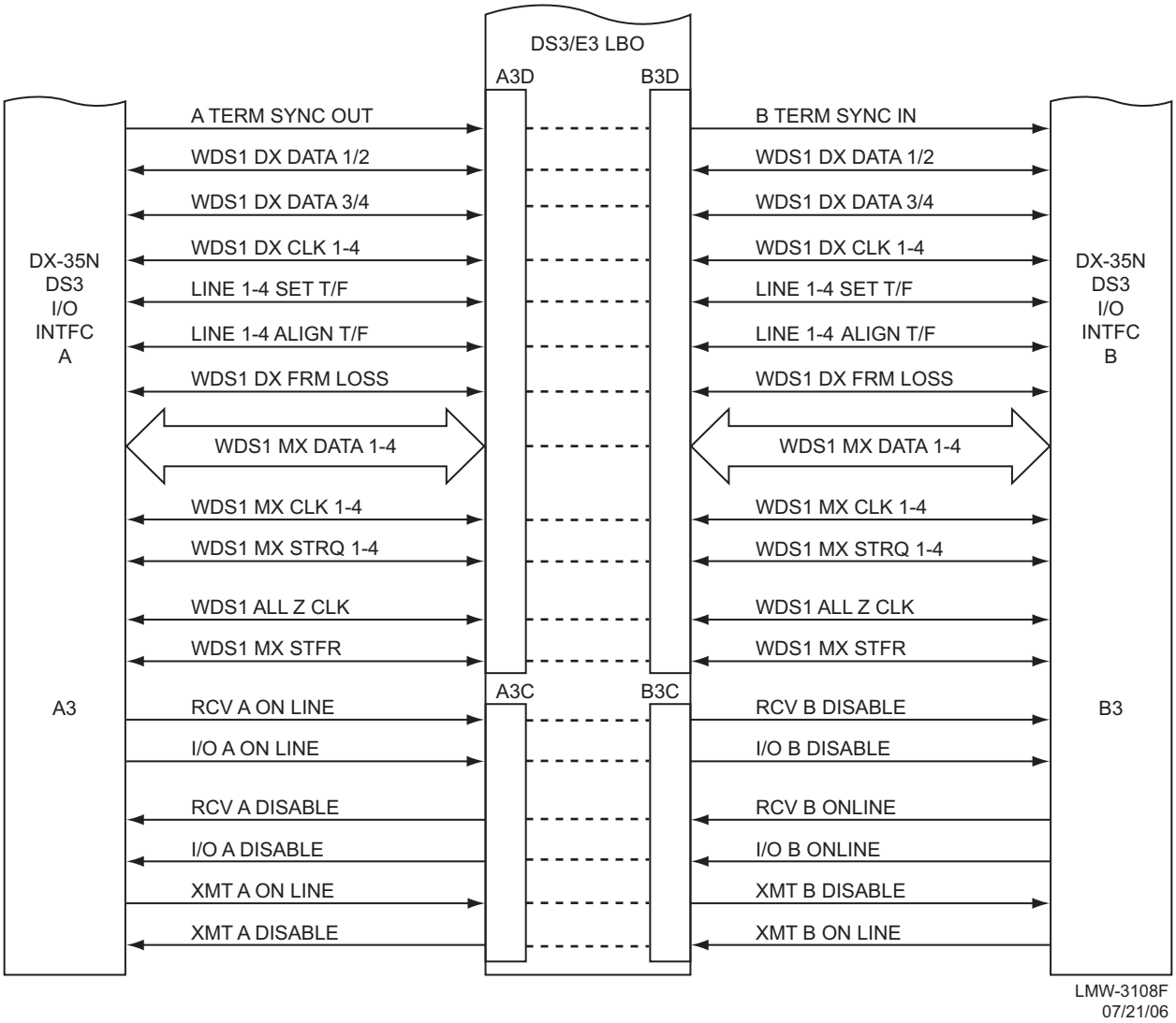


Figure 3-16 DS3 LBO Interconnect Diagram (Sheet 1 of 2)

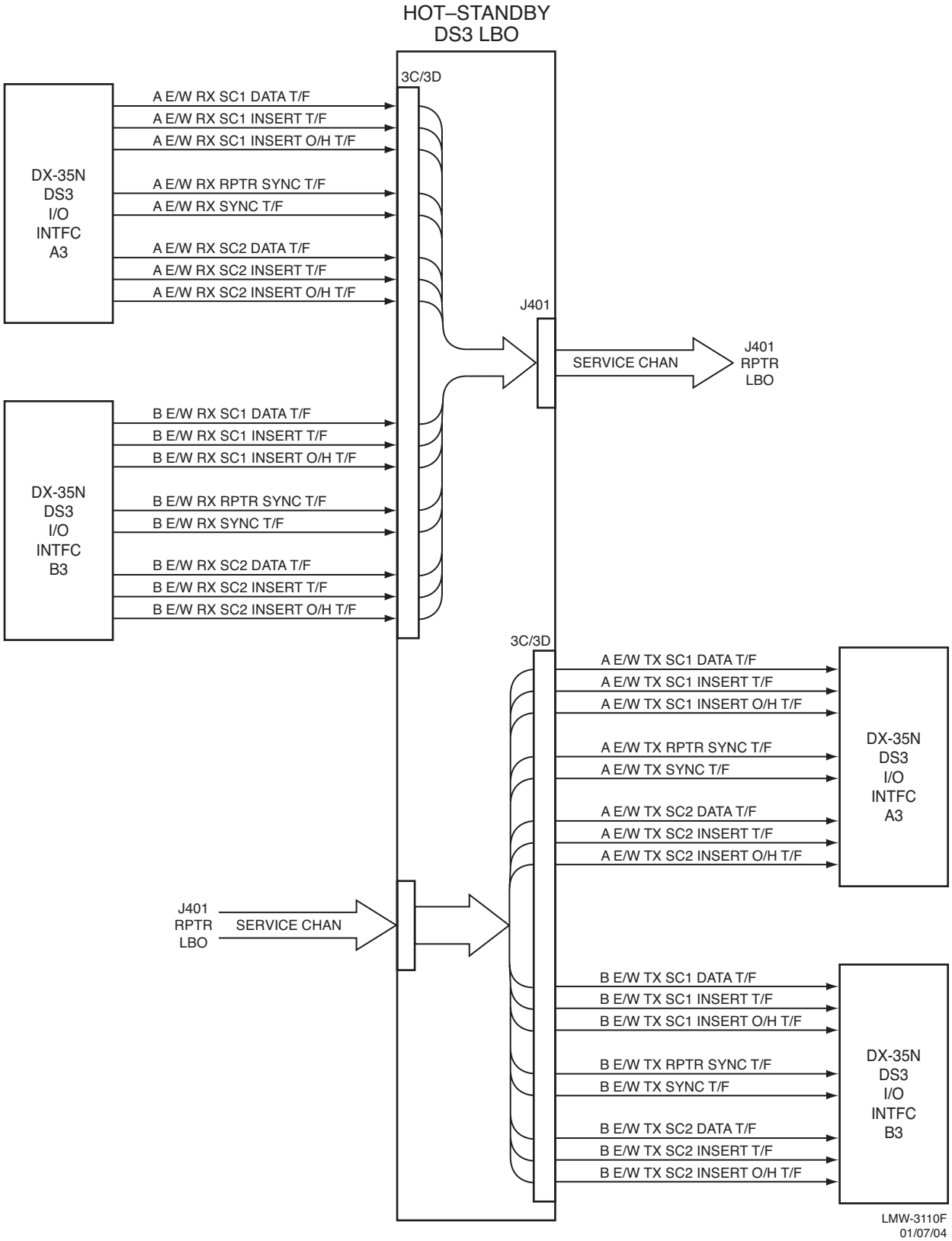


Figure 3-16 DS3 LBO Interconnect Diagram (Sheet 2 of 2)

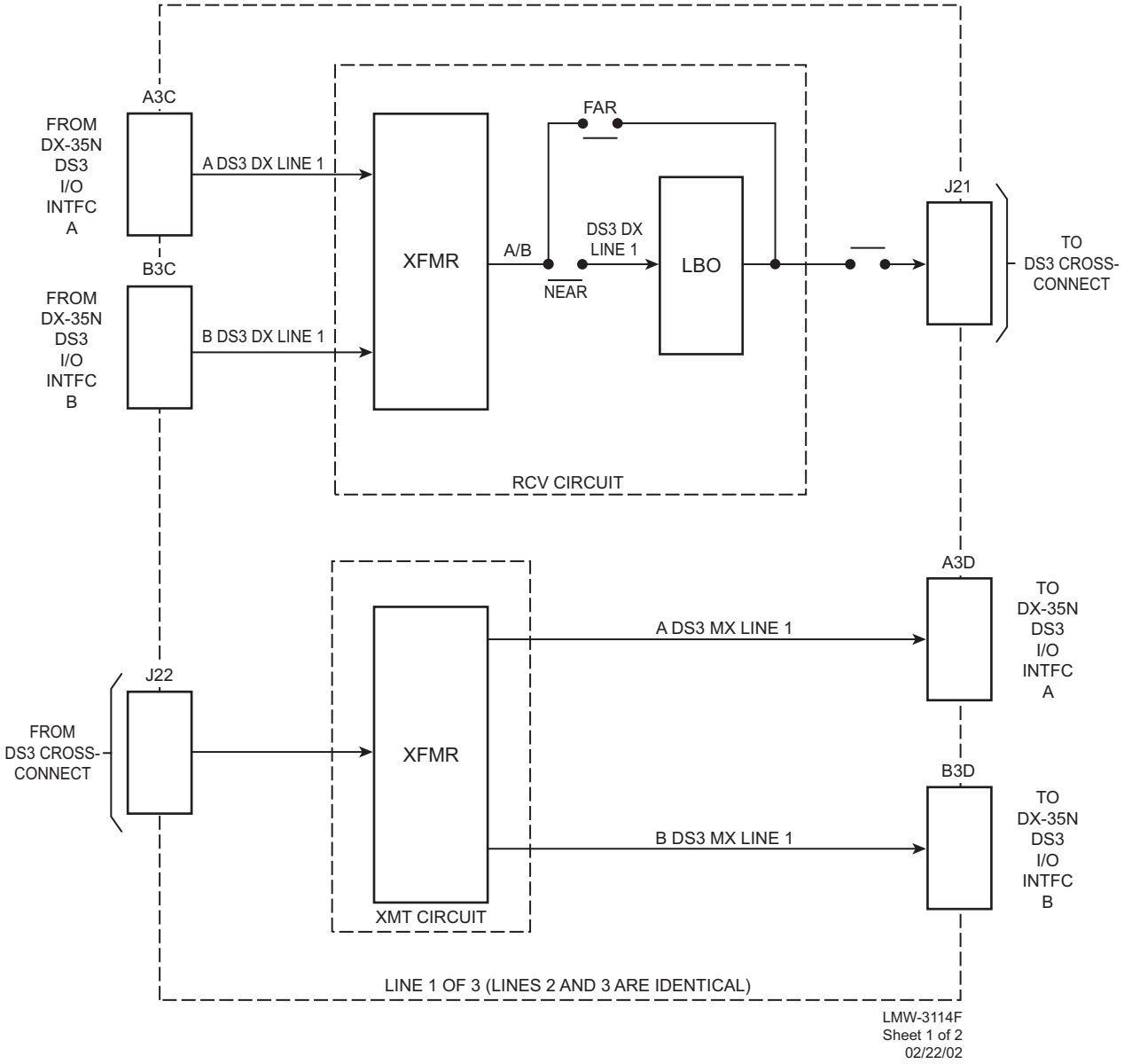


Figure 3-17 DS3 LBO Functional Block Diagram (Sheet 1 of 2)

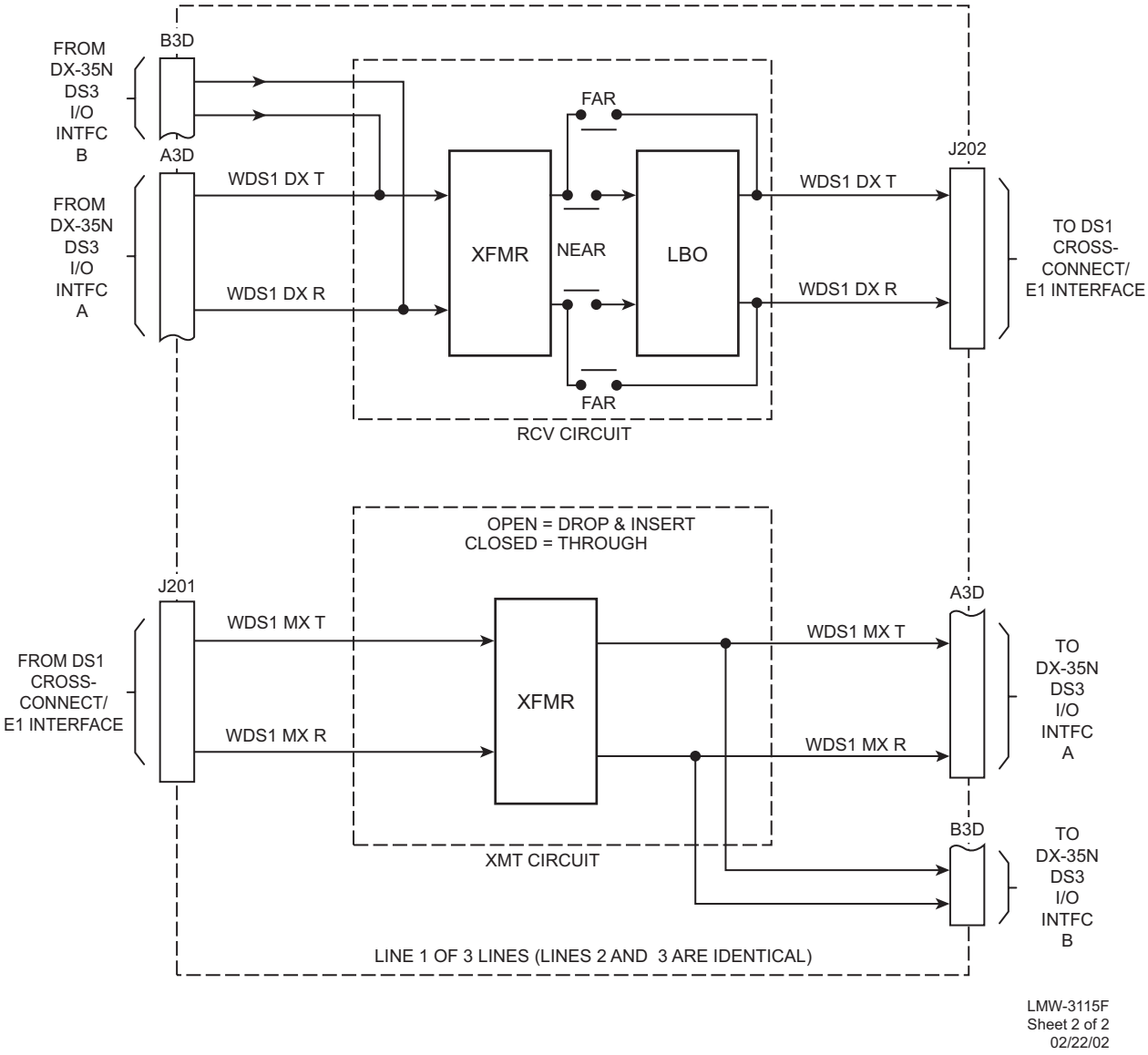


Figure 3-17 DS3 LBO Functional Block Diagram (Sheet 2 of 2)

3.5.2.4 DS3 RCV Circuit

The demultiplexed signals (A/B DS3 DX LINE 1) from the DX-35N DS3 I/O Interface module(s) are transformer coupled to the strapping for the LBO circuit. If the LBO is strapped for NEAR, the LBO circuit simulates lengths of twisted-pair cable to meet cross-connect requirements. If the LBO is strapped for FAR, the LBO circuit is bypassed.

3.5.2.5 Wayside DS1 RCV Circuit

The demultiplexed signals (WDS1 DX T/R) from the DX-35N DS3 I/O Interface module(s) are transformer coupled to the strapping for the LBO circuit. If the LBO is strapped for NEAR, the LBO circuit simulates lengths of twisted-pair cable to meet cross-connect requirements. If the LBO is strapped for FAR, the LBO circuit is bypassed.

3.5.2.6 Repeater Signal Distribution

In a hot-standby configuration, the DS3 LBO distributes SC1 and SC2 TX and RX service channel data, insert data, insert off-hook, and repeater and TX sync to/from RPTR connector J401 and the A and B I/O interface modules.

3.5.2.7 I/O Interface-to-I/O Interface Data Distribution

The DS3 LBO distributes redundant data between I/O interface A and I/O interface B. I/O interface A-to-B data is wired directly to connectors A3D and B3D. Receive On-Line and I/O On-Line are also cross-coupled to provide a make-before-break switch control.

3.5.3 OC3/STM-1 Aux Interface

The MDR-8000 is equipped with an auxiliary (aux) interface to interface wayside DS1 data, I/O interface-to-I/O interface data and controls, and repeater data. See Figure 3-18 for to/from signal information and application information.

3.5.3.1 Wayside DS1 XMT Circuit

See Figure 3-19. Transformers couple the DS1 in tip and ring (DS1 IN T/R) signals at J201 to DX-35P OC3/STM-1 I/O Interface A (via connector A3E), and B (via connector B3E) if the system is hot-standby.

3.5.3.2 Wayside DS1 RCV Circuit

The demultiplexed signals (DS1 OUT T/R) from the DX-35P OC3/STM-1 I/O Interface module(s) are transformer coupled to the DS1 cross-connect via connector J202.

3.5.3.3 Repeater Signal Distribution

In a hot-standby configuration, the OC3/STM-1 aux interface distributes SC1 TX and RX service channel data, insert data, insert off-hook, and repeater and TX sync to/ from RPTR connector J203 and the A and B I/O interface modules. The SC2 service channel is wired but not used.

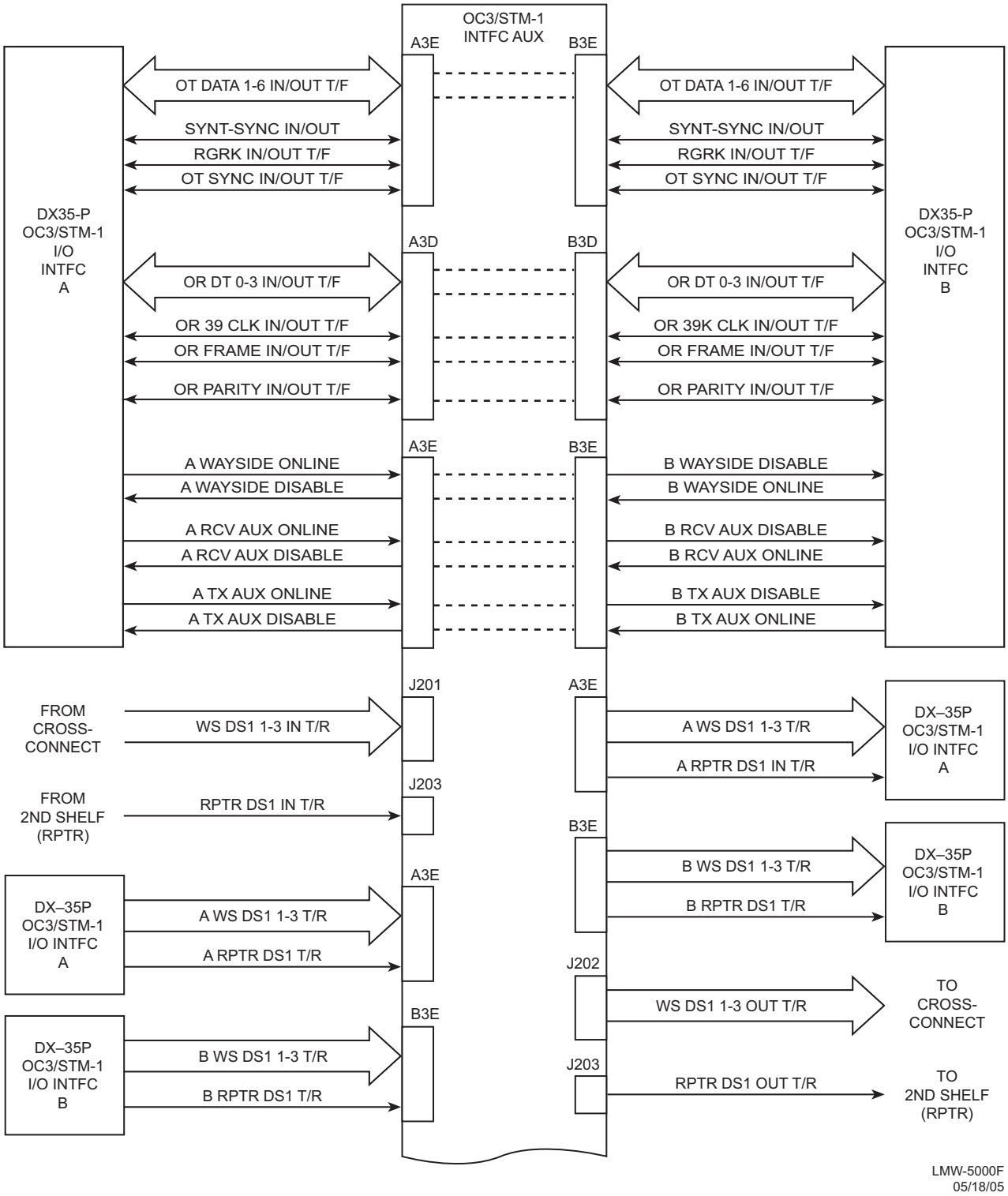


Figure 3-18 OC3/STM-1 Aux Interface Interconnect Diagram

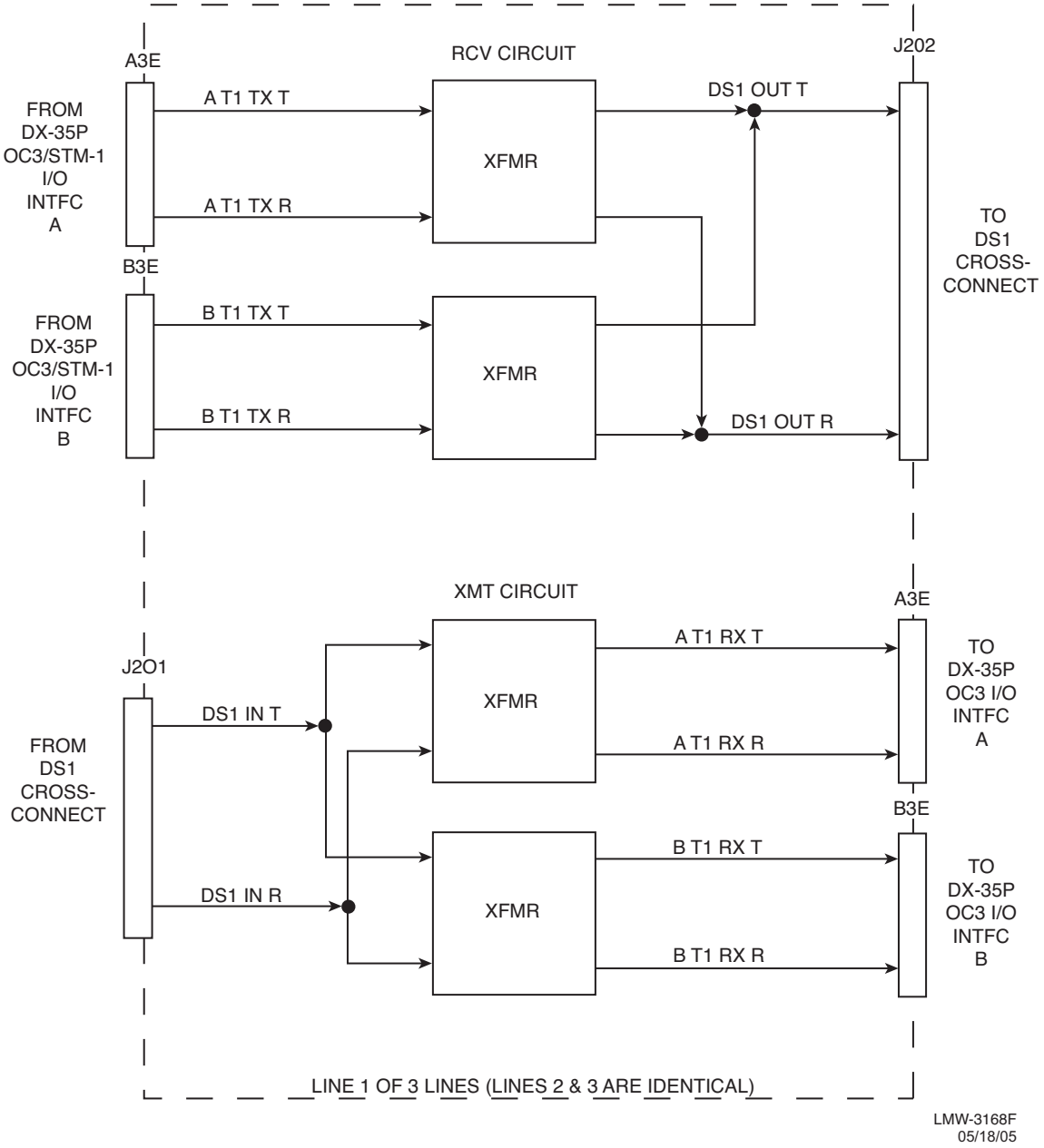


Figure 3-19 OC3/STM-1 Aux Interface Functional Block Diagram

3.5.4 Ethernet Aux Interface

The MDR-8000 is equipped with an auxiliary (aux) interface to interface up to four DS1, I/O interface-to-I/O interface data and controls, and repeater data. See Figure 3-20 for to/from signal information and application information.

3.5.4.1 DS1 XMT Circuit

See Figure 3-21. Transformers couple the DS1 in tip and ring (DS1 IN T/R) signals at J201 to DX-35P OC3/STM-1 I/O Interface A (via connector A3E), and B (via connector B3E) if the system is hot-standby.

3.5.4.2 DS1 RCV Circuit

The demultiplexed signals (DS1 OUT T/R) from the DX 35P OC3/STM-1 I/O Interface module(s) are transformer coupled to the DS1 cross-connect via connector J202.

3.5.4.3 Repeater Signal Distribution

In a hot-standby configuration, the OC3/STM-1 aux interface distributes SC1 TX and RX service channel data, insert data, insert off-hook, and repeater and TX sync to/from RPTR connector J203 and the A and B I/O interface modules. The SC2 service channel is wired but not used.

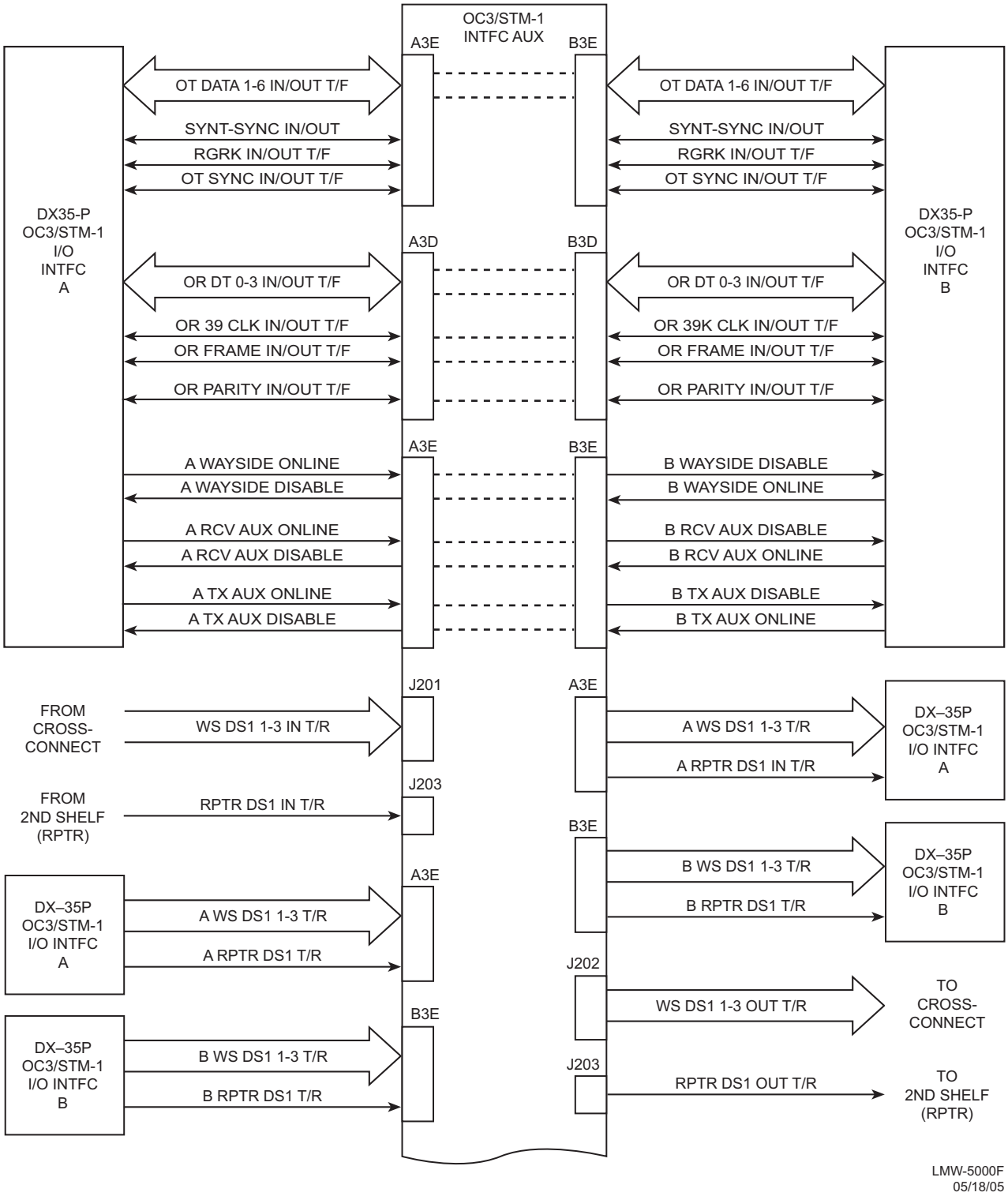


Figure 3-20 Ethernet Aux Interface Interconnect Diagram

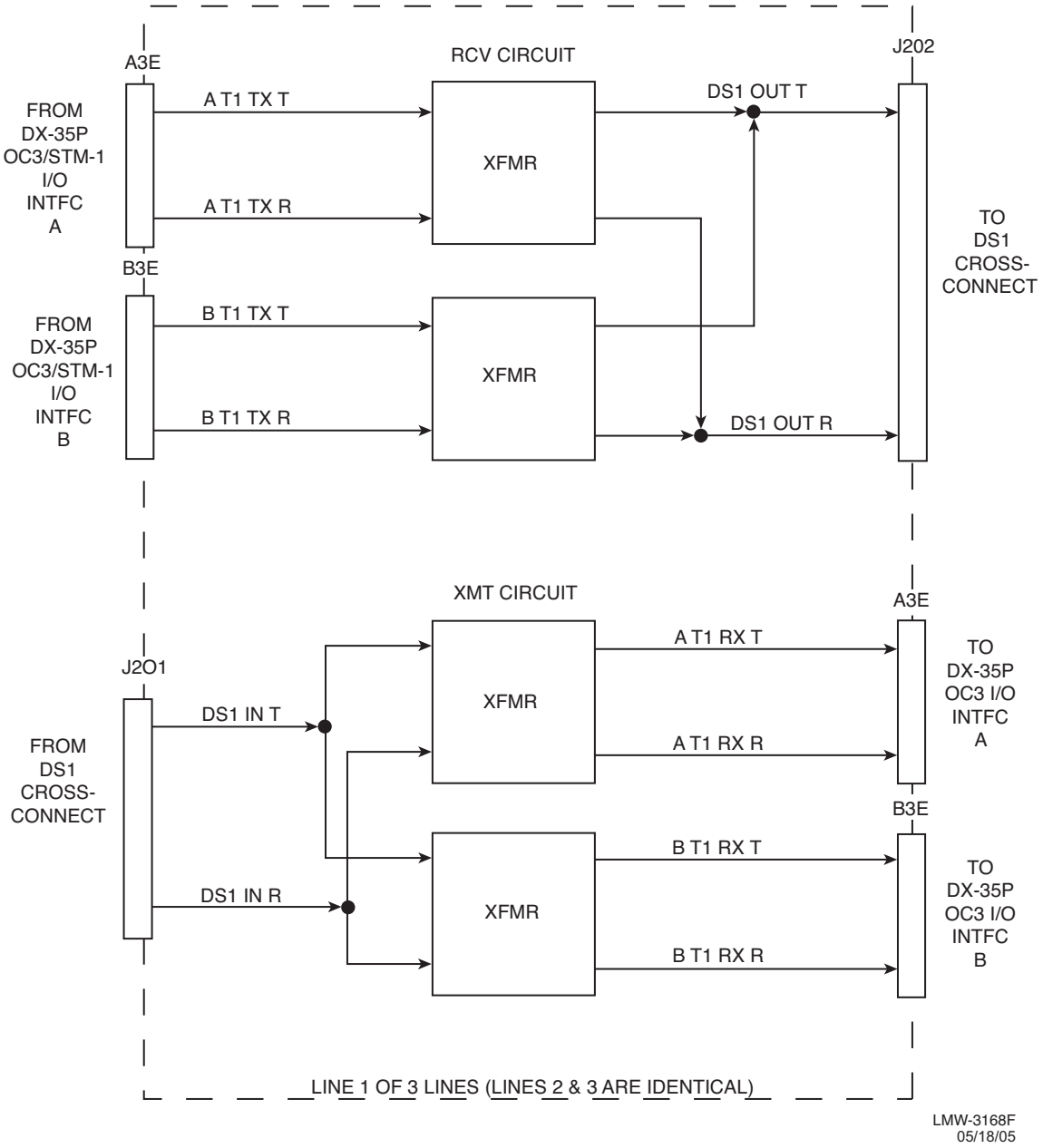


Figure 3-21 Ethernet Aux Interface Functional Block Diagram

3.5.5 ETH T1 Line Interface

The ETH T1 Line Interface is equipped with connectors to interface up to 32 T1 lines, I/O interface-to-I/O interface data and controls, and repeater data. See Figure 3-22 for to/from signal information and application information.

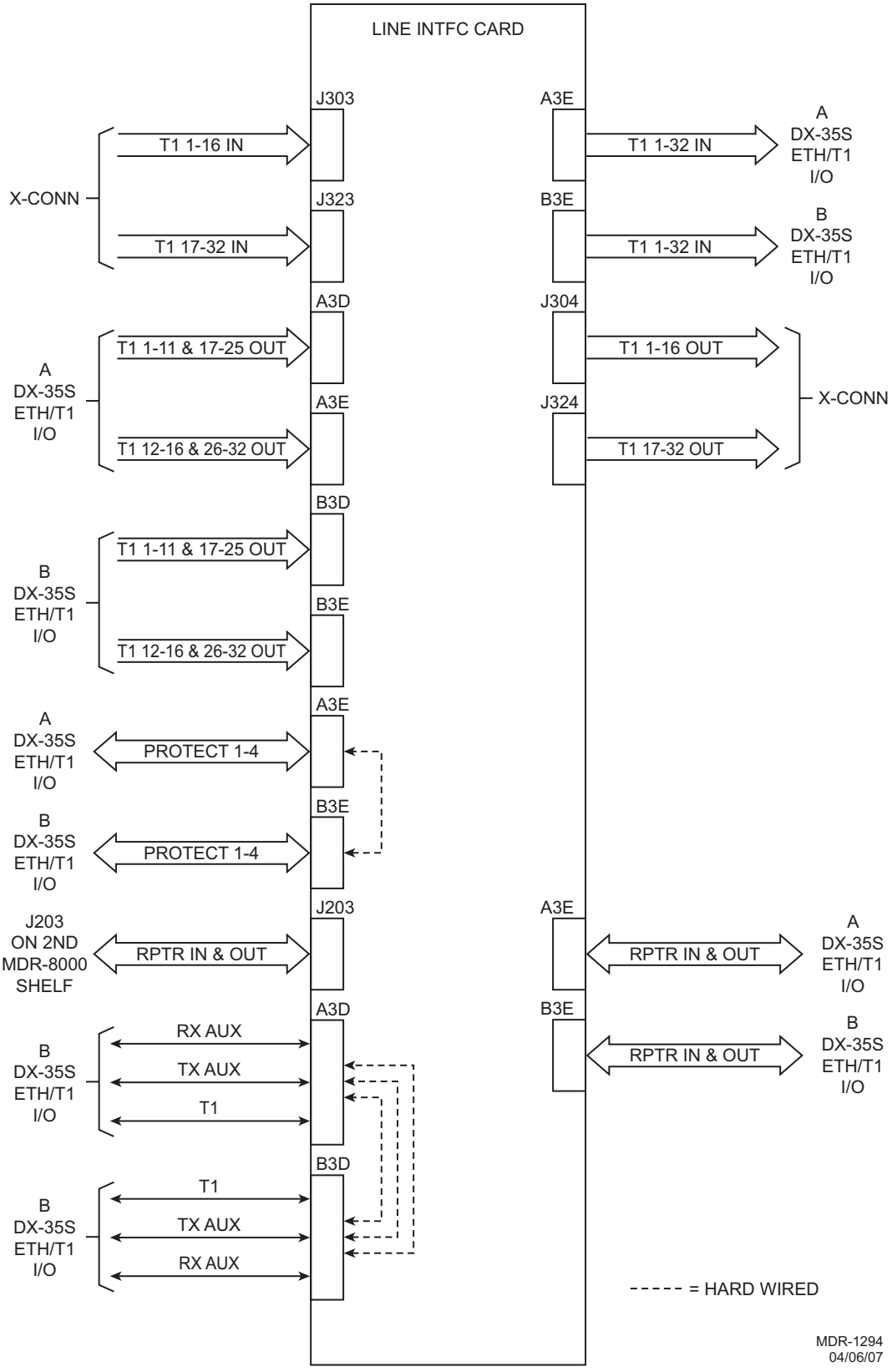


Figure 3-22 ETH Line Interface Interconnect Diagram

3.5.5.1 T1 XMT Circuit

See Figure 3-23. Transformers couple the T1 IN tip and ring (T1 IN T/R) signals at J303 (1-16) and J323 (17-32) to DX-35S ETH/T1 I/O A (via connector A3E), and B (via connector B3E) if the system is hot-standby.

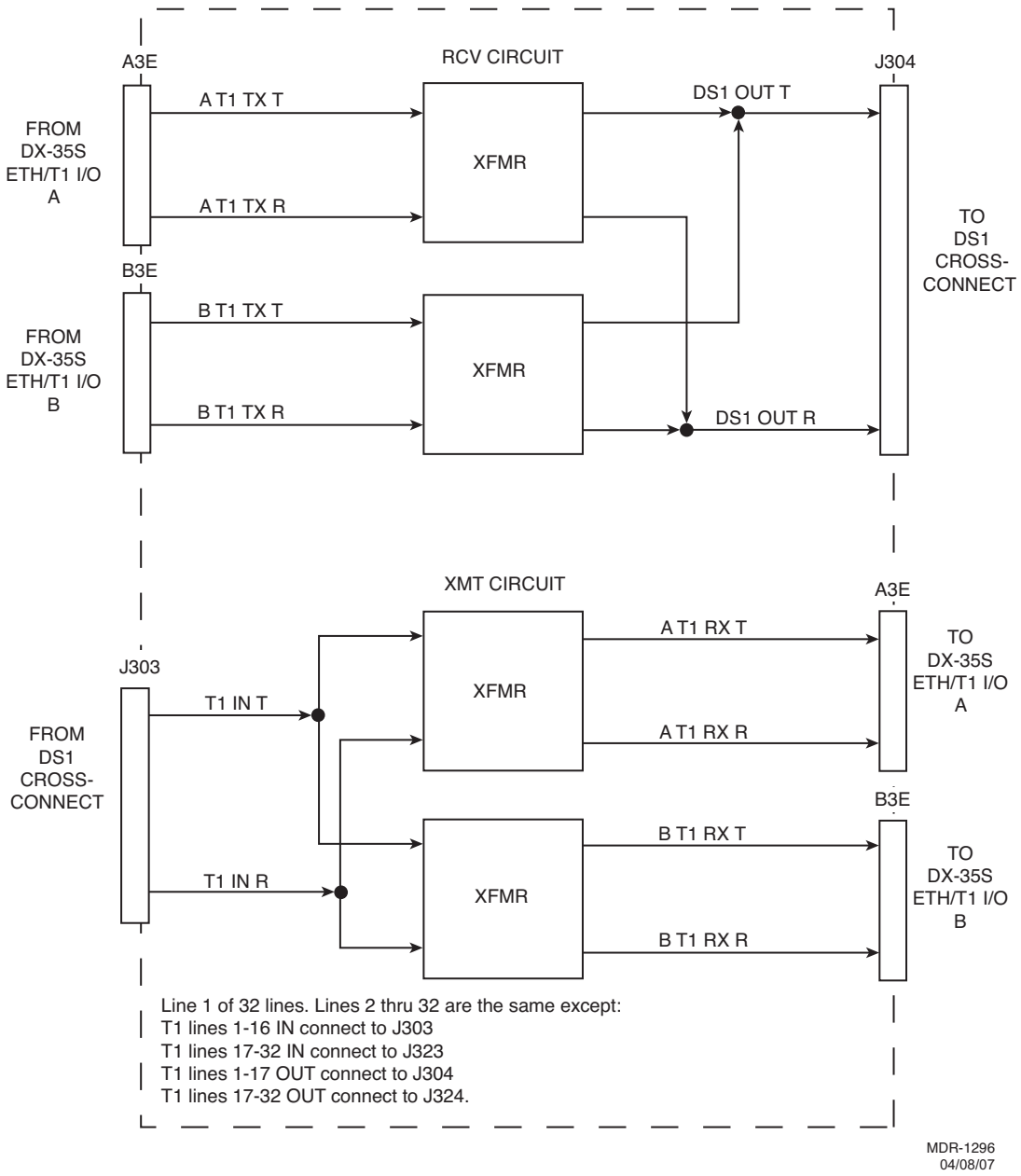


Figure 3-23 ETH/T1 Line Interface Functional Block Diagram

3.5.5.2 T1 RCV Circuit

The demultiplexed signals (T1 TX T/R) from the DX-35S ETH/T1 I/O module(s) are transformer coupled to the cross-connect via connectors J304 (1-16) and J324 (17-32).

3.5.5.3 Repeater Signal Distribution

In a hot-standby configuration, the ETH T1 Line interface distributes SC1 TX and RX service channel data, insert data, insert off-hook, and repeater and TX sync to/from RPTR connector J203 and the A and B ETH/T1 I/O modules. The SC32 service channel is wired but not used.

3.5.5.4 I/O Interface-to-I/O Interface Data Distribution

The OC3/STM-1 aux interface distributes redundant data between I/O interface A and I/O interface B. I/O interface A-to-B data is wired directly to connectors A3E and B3E. WAYSIDE ONLINE/DISABLE, RCV AUX ONLINE/DISABLE, AND TX AUX ONLINE/DISABLE CONTROLS are cross-coupled to provide a make-before-break switch control.

3.5.6 DX-35M-1/2 DS1/E1 I/O Interface

The DX-35M-1/2 DS1/E1 I/O Interface multiplexes/demultiplexes up to 16 DS1/E1 channels, up to four X/Y data rail pairs, and service channel data in the MDR-8000 radio. The DX-35M-1 (PN 3DH 03131 AA) operates with North American data while the DX-35M-2 (PN 3DH 03131 AB) is compatible with international (E1) data rates.

See Figure 3-24 for to/from signal information and application information. The I/O Interface consists of several functional blocks each of which is described in the following paragraphs.

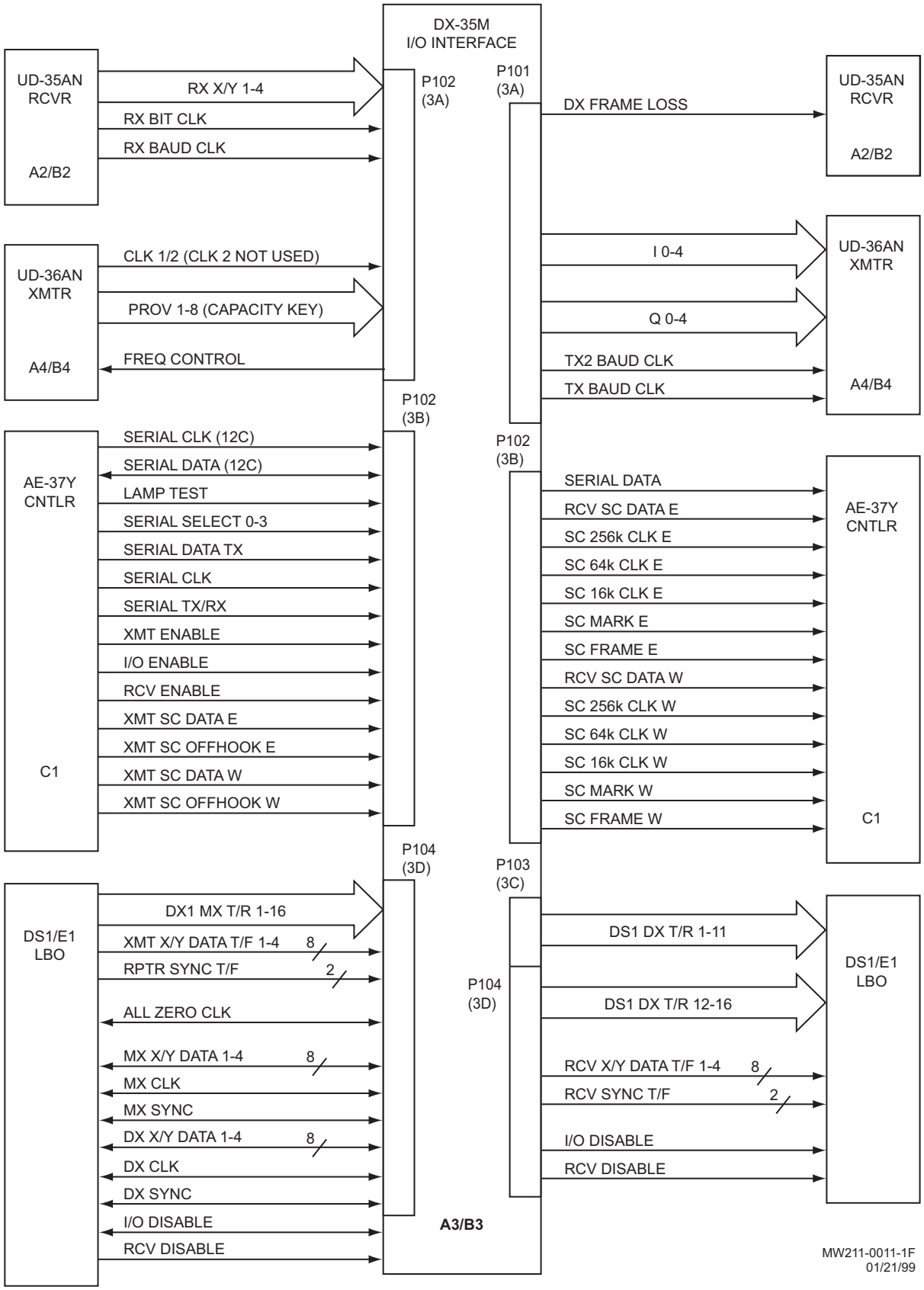


Figure 3-24 DX-35M DS1/E1 I/O Interface Interconnect Diagram

3.5.6.1 Signal Crossover

See Figure 3-25. Crossover occurs in the LIO ASIC in both XMT and RCV directions. Crossover signals include data, sync, and clock. Refer to Table 3-2 for switching characteristics. Refer to Table 3-3 for switching priorities.

Table 3-2 I/O Interface Switching

Radio Config	XMT Switch	I/O Switch	RCV Switch
Terminal	Independent Switching	Independent Switching	Tracks on-line RCVR
Repeater with all lines provisioned ON	Independent Switching	Independent Switching	Tracks on-line RCVR
Repeater with all through lines provisioned NM	Independent Switching	Independent Switching	Tracks on-line RCVR
Repeater with all through lines provisioned OFF	Tracks on-line XMTR	Tracks on-line I/O	Tracks on-line RCVR

Table 3-3 I/O Interface Switching Priorities

I/O Switch	RCV Switch
Override (Switch on Controller Front Panel)	Override (Switch on Controller Front Panel)
Module Not Present	Module Not Present
Leghorn ASIC Failure	Radio Frame Loss
XMT/RCV Alarm on Leghorn ASIC	High CRC Error Rate
Common Loss Alarm	Eye Closure
Manual Switch (Switch on Controller Front Panel)	Path Distortion
	AGC Alarm
	Manual Switch (Switch on Controller Front Panel)

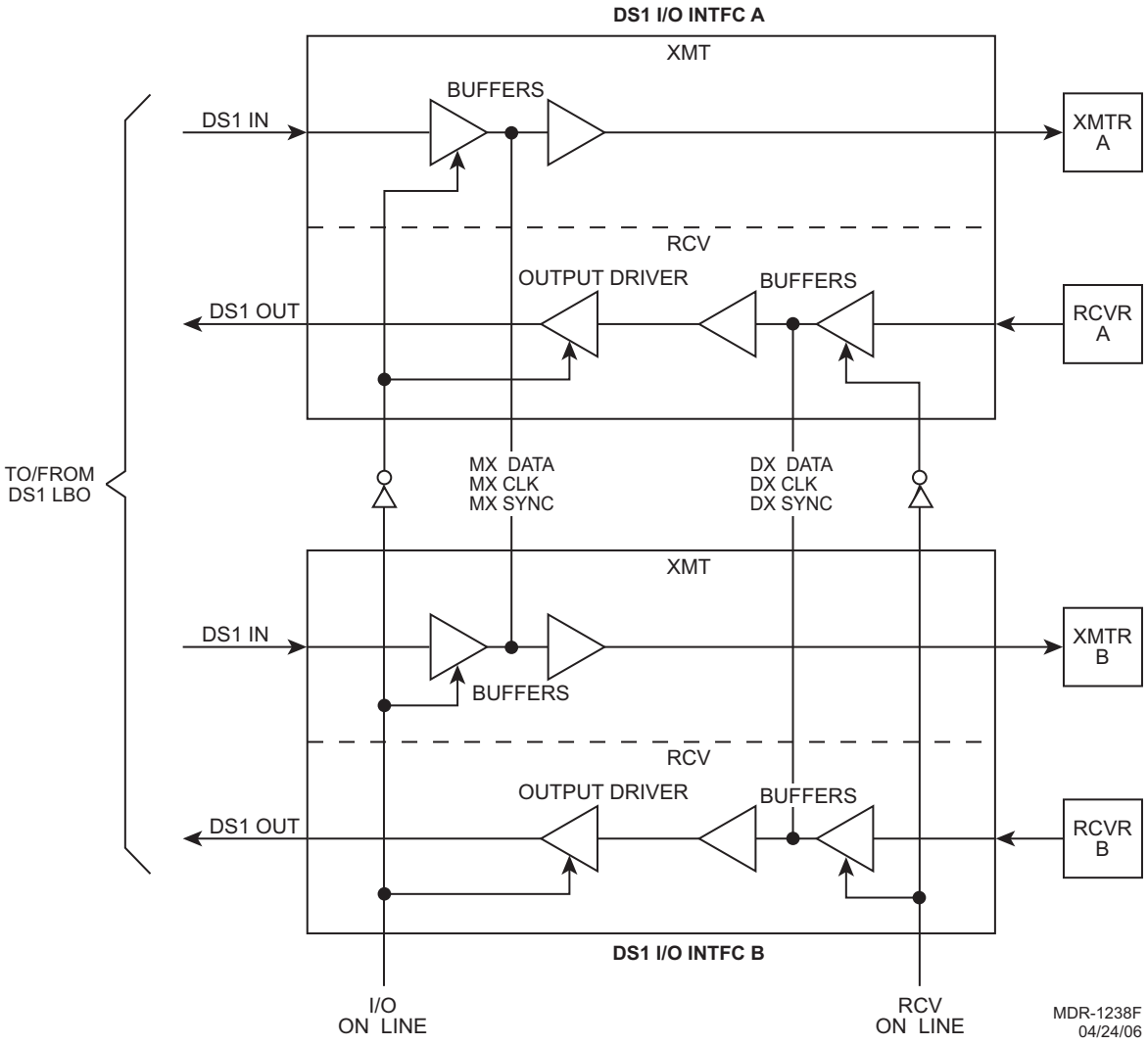


Figure 3-25 DS1 Crossover Functions Simplified Functional Block Diagram

3.5.6.2 Multiplex Signal Flow

The I/O interface module receives 16 DS1/E1 channels from the DS1/E1 LBO via connector P104. Each channel (CHAN 1-16 DS1/E1) consists of positive (P) and negative (N) data streams in RZ format. The channel inputs are applied to appropriate DS1/E1 interface ASICs. The I/O interface module sends four I and Q data rails to the UD-35( ) Transmitter module via connector P101.

3.5.6.2.1 DS1/E1 Interface ASIC MUX

There are eight DS1/E1 interface ASICs that serve as DS1 or E1 line interface processors. Each of these ASICs processes two DS1 or E1 channels and performs clock recovery, clock smoothing, elastic buffering, and line encoding and decoding (AMI, B8ZS, HDB3). The RZ data pairs (Chan 1-16 In Tip and Ring) entering the multiplex section of the DS1/E1 interface gate arrays are bridged onto one channel, converted to NRZ format, B8ZS or HDB3 decoded, and then written into an elastic buffer by the recovered clock. In the elastic buffer, stuff requests are generated whenever the two clocks writing into (recovered clock) and reading from (Mux Clock) the elastic buffer are five states apart. The data is re timed off the rising edge of the Mux Clock and sent to the output pins as MUX CHAN 1-4 DATA. The outputs of two of the DS1/E1 interface ASICs (1 and 2) are applied directly to the low capacity I/O (LIO) ASIC. The outputs of the remaining six DS1/E1 interface ASICs (3 through 8) are applied to the MUX/DEMUX EPLD.

3.5.6.2.2 Low Capacity I/O ASIC MUX

The multiplexer circuits in the low capacity I/O ASIC combines inputs from the following sources (redundant, if the system is hot-standby): 1) rail X/Y 1-4 data from repeater via connector J314 on the LBO, 2) channel 1 MUX data from DS1/E1 interface ASIC #1, 3) channel 2 MUX data from DS1/E1 interface ASIC #1, 4) channel 3 MUX data from DS1/E1 interface ASIC #2, 5) channel 4 MUX data from DS1/E1 interface ASIC #2, 6) rail X/Y 2-4 data (multiplexed channels 5-16) from the muldem ASIC, and 7) loopback data from demultiplexer circuits in the muldem ASIC and the low capacity I/O ASIC.

In the low capacity I/O ASIC, the MUX CHAN 1-4 DATA outputs of the DS1/E1 interface ASICs are combined and converted to an X/Y data rail pair. Using control bits from the serial interface, this data may be inserted into the rail pairs, overwriting the repeater data. Service channel and auxiliary channel data is converted for insertion into the X/Y data rail pair.

The four X/Y data rail pairs are scrambled into pseudo-random bit sequences and then multiplexed and modulated to form a 32 or 128 TCM encoded data set. The data set is output as I and Q data (TX I/Q 1-4) to the transmitter module via connector P101.

3.5.6.2.3 Muldem PLD MUX

In the multiplex section of the muldem PLD, twelve data outputs from the six DS1/E1 interface ASICs are combined into 3 pairs of data rails, MX X/Y DATA 2-4, which are sent to the on-line low capacity I/O interface ASIC.

The muldem PLD provides the rail clock (MX CLK) and frame pointer (MX SYNC) necessary to regenerate the transmit radio frame counters. For each of the 12 data streams emanating from the DS1/E1 interface ASICs, a clock derived from the MX CLK is generated from these counters. Each of these twelve clocks are sent to the appropriate DS1/E1 interface ASIC to clock the data out of the MX elastic buffer and to place the data properly within the MX X/Y 2-4 DATA rails. Stuff requests from the DS1/E1 interface ASICs are processed to provide stuff code bits in the radio frame overhead and to keep the MX elastic buffer pointers aligned.

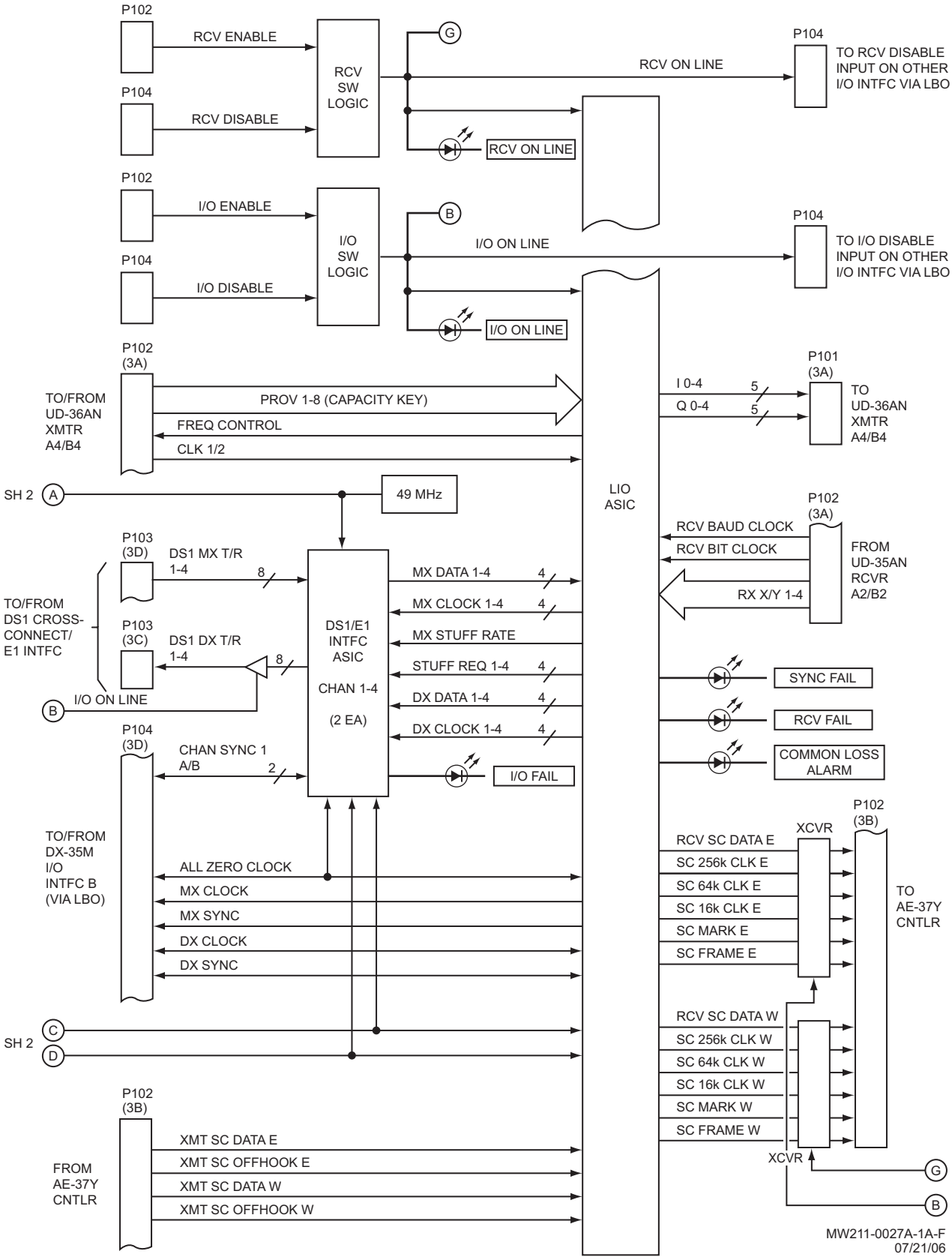


Figure 3-26 DX-35M DS1/E1 I/O Interface Functional Block Diagram (Sheet 1 of 3)

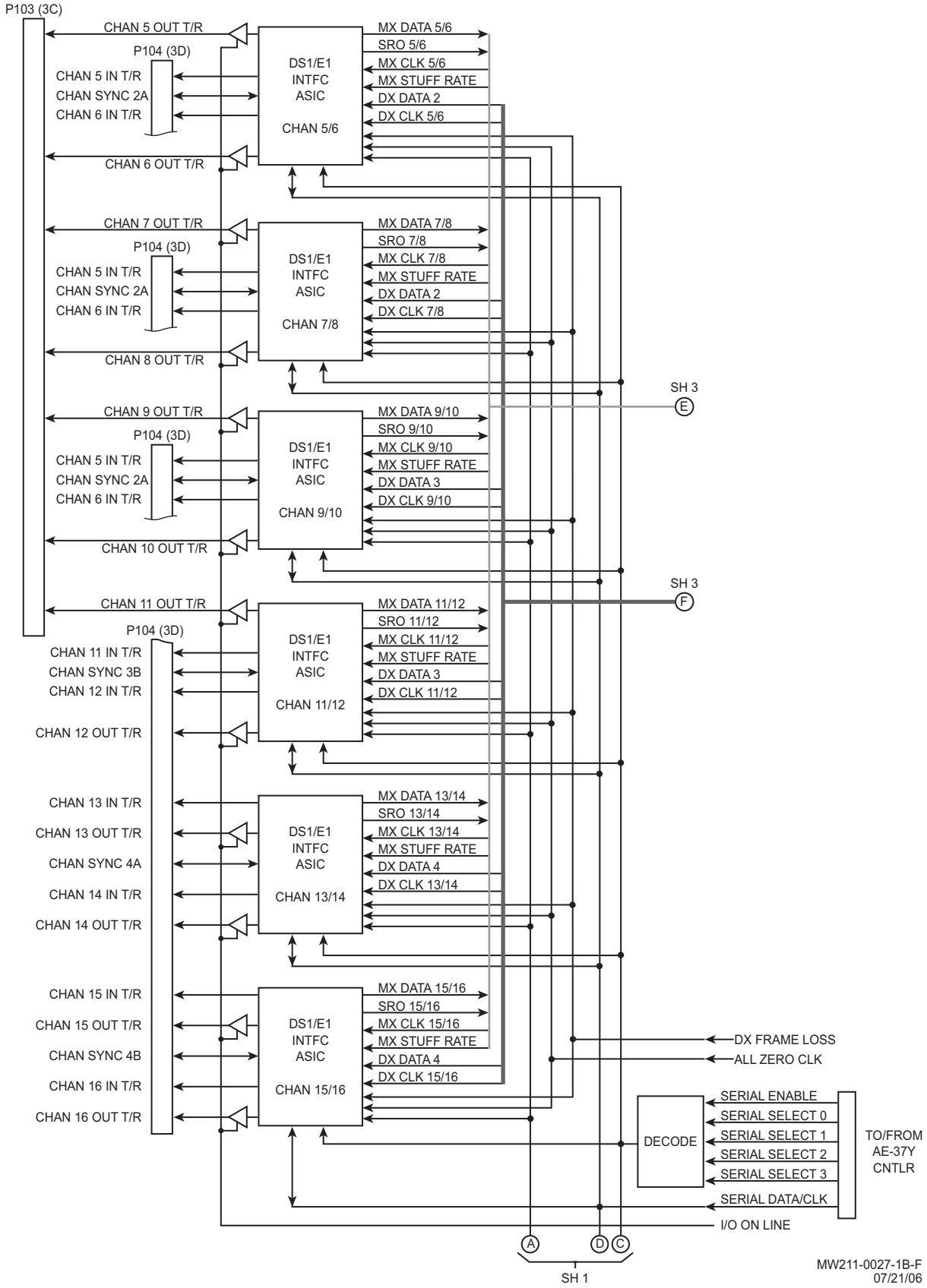


Figure 3-26 DX-35M DS1/E1 I/O Interface Functional Block Diagram (Sheet 2 of 3)

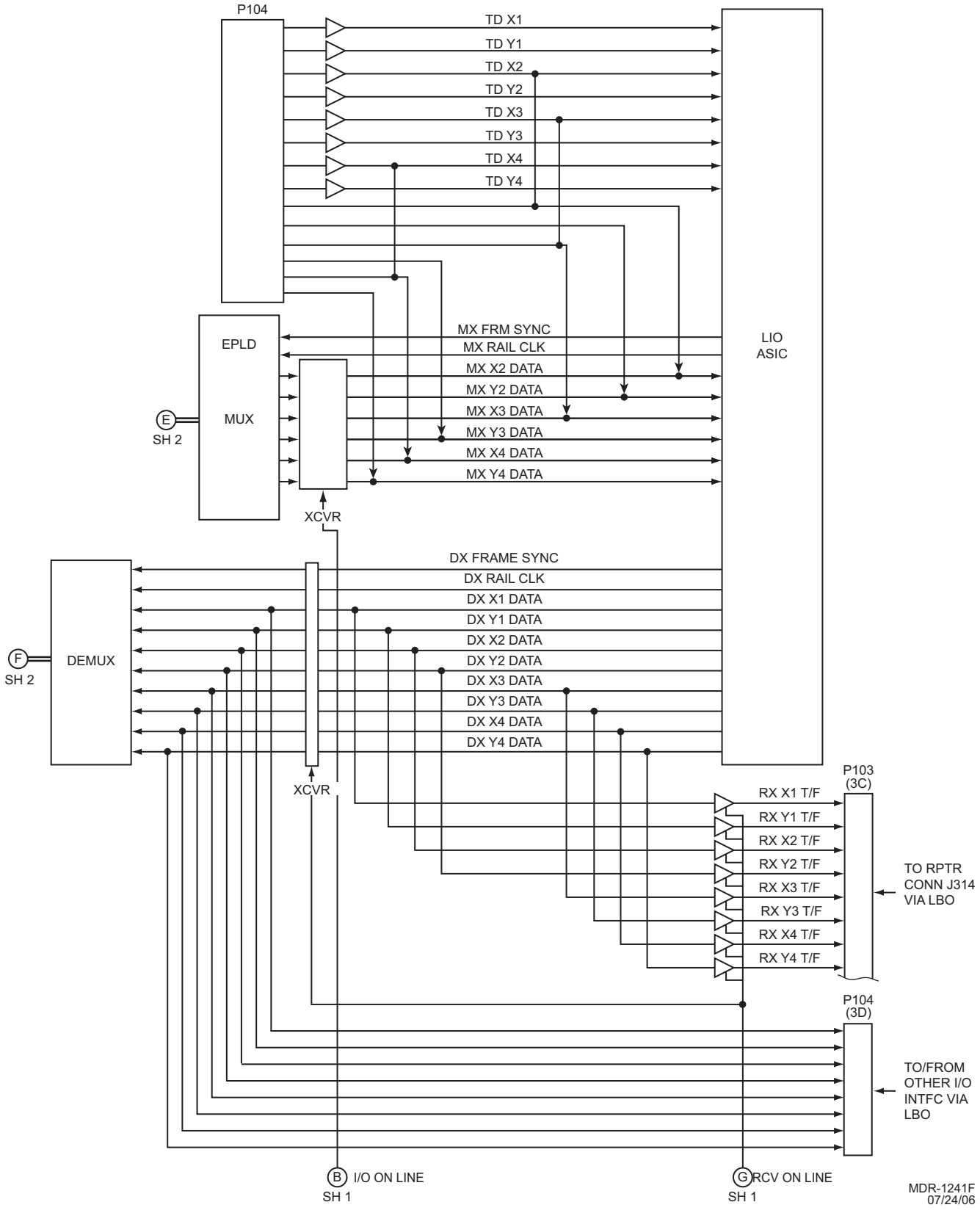


Figure 3-26 DX-35M DS1/E1 I/O Interface Functional Block Diagram (Sheet 3 of 3)

3.5.6.3 Demultiplex Signal Flow

The I/O interface module receives four RX X/Y data rails from the UD-36( ) Receiver module via connector P102. The I/O interface module sends 16 DS1/E1 channels to the DS1/E1 LBO via connector P103. Each channel (CHAN 1-16 DS1/E1) consists of positive (P) and negative (N) data streams in RZ format.

3.5.6.3.1 Low Capacity I/O ASIC DEMUX

The low capacity I/O (LIO) ASIC receives RX X/Y data rails from the UD-36( ) Receiver module (connector P102). The data is demultiplexed, according to the modulation mode (determined by the capacity key), and DADE'ed, to align the receive portion of the ASIC with the on-line ASIC, which is necessary for errorless switching.

Each X and Y rail contains four channels of data. Rail number 1 channel number 1 also contains auxiliary data, including service channel. The X/Y rail number 1 data is decoded and de-scrambled and service channel and auxiliary channel data is recovered. The received service channel data (recovered from the first rail pair) is sent to the OSS circuit in the AE-37( ) Controller module. Repeater service channel data from the OSS circuit is inserted back into the first rail pair.

The four X/Y rail pairs of the on-line module (RCV) are then sent to the DS1/E1 demultiplexing sections of the A and B I/O Interface modules, and the repeater port connectors. X/Y rail pair 1 is sent to the DS1/E1 interface ASICs TI CHANNELS 1-4. X/Y rail pairs 2, 3, and 4 are applied to the MUX/DEMUX EPLD.

The LIO ASIC may bridge onto any of the X/Y rail channels and route that channel data to the line interface arrays for lines 1-4 (channel is selectable by provisioning). This data may originate in the on-line low capacity I/O ASIC or the off-line ASIC.

3.5.6.3.2 DS1/E1 Interface ASICs, Lines 1-4

Each DS1/E1 interface ASIC (Leghorn) can process two DS1/E1 lines. The DS1/E1 interface ASICs numbers 1 and 2 provide a smooth clock and elastic buffer for each line 1-4. Line coding is added and the coded P and N data from the on-line module (I/O) is sent to lines 1-4 of the DS1/E1 LBO module.

3.5.6.3.3 MUX/DEMUX EPLD

The MUX/DEMUX EPLD regenerates the receive frame counters using the clock and frame sync from the LIO array. It bridges onto the second, third, and fourth X/Y rail pairs and routes the channel data to the DS1/E1 interface ASICs for lines 5-16.

In the demultiplex section, the multiplexed receive rail data from the low capacity I/O ASIC (DX X/Y 2-4) is converted into three DS2 signals (DX DATA 2-4). Each DX DATA signal is applied to a pair of DS1/E1 Interface ASICs for ultimate conversion to four DS1/E1 data streams (DX DATA 2 is applied to DS1/E1 Interface ASIC #3 and #4, DX DATA 3 is applied to DS1/E1 Interface ASIC #5 and #6, and DX DATA 4 is applied to DS1/E1 Interface ASIC #7 and #8). The muldem PLD provides the rail clock (DX CLK 5-16)) and frame pointer (DX SYNC) necessary to regenerate the receive radio frame counters. These counters are used to provide the twelve clocks necessary for clocking the DX DATA into the DS1/E1 Interface ASIC DX elastic buffers. Stuff code bits contained within DX X/Y rail overhead are used to gap the DX elastic buffer clocks so that the receive DS1/E1 data rate equals the transmit DS1/E1 data rate.

3.5.6.3.4 DS1/E1 Interface ASICs, Lines 5-16

The DS1/E1 interface ASICs provide a smooth clock and elastic buffer for each line. Line coding is added and the coded P and N data from the on-line module is sent to lines 5-16 of the DS1/E1 LBO.

The demultiplex section of each DS1/E1 interface ASIC receives 6.312 MHz data (2DXDT, containing four channels of DS1/E1 data), a 1.544 or 2.048 MHz DEMUX gapped clock (E1DXCK), the 49 MHz reference clock (49 MHZ), and a 1.544 or 2.048 MHz MUX gapped clock (E1DXCK). Normally the DEMUX clock is used. In an out of frame condition the integrity of the DEMUX clock is lost and the MUX clock is selected. The 6.312 MHz NRZ data, and the stuffed gapped clock are re timed by the 49 MHz reference clock. The data is then clocked by the gapped clock to remove the appropriate two channels of data. The two channels of data are clocked into an elastic buffer by the gapped clock. The data is then converted to a quasi-RZ format and encoded, according to the modulation mode. The encoded data is sampled in an AIS detector for loss of signal, demultiplexed onto two (T&R) channels, and converted to RZ data. In the DS1 mode only, TEO (trailing edge overshoot) pulses are added to the RZ data so that the pulses conform to cross-connect requirements without the need of an external equalizer. Tip and ring outputs for each channel (DS1/E1 Chan 1-16 Out T/R) are applied to the MDR-8000 DS1/E1 LBO module via connectors P103 and P104.

3.5.6.3.5 Service Channel

At a terminal, the LIO ASIC multiplexes the 256 kb/s data stream (comprised of three 64 kb/s service channels and one 16 kb/s auxiliary channel from the AE-37( ) Controller) together with the MX DATA 1-( ) and MX X/Y DATA (hot-standby only) inputs into radio frames. The radio frames are then converted into four X/Ys rail pairs (XMT X/Y RAILS 1-4 P/N) and clocked into the encoder/decoder circuit by the BAUD CLK.

The XMT X/Y 1-4 T/F and REPEATER SYNC T/F inputs from connector J103, via LBO connector J401, are the primary inputs to the I/O in a drop and insert or through-repeater configuration. If the repeater is hot-standby, the I/O multiplexes the 256 kb/s data stream (comprised of three 64 kb/s service channels and one 16 kb/s auxiliary channel from the AE-37X Controller) together with the XMT X/Y 1-4 T/F repeater inputs (J103) and MX X/Y DATA (J106) from the off-line DX-35L I/O interface. The REPEATER SYNC T/F syncs the repeater LIOs. Insert data consists of MX DATA 1-4 and MX X/Y DATA 5-16. The insert data is inserted into the rail pairs, overwriting the repeater data.

3.5.6.4 Control and Monitor Functions

3.5.6.4.1 Provisioning

PROV 1-8 inputs from the provisioning key, located on the UD-35( ) Transmitter module, select the type of radio and trellis coded modulation scheme (32/128 TCM).

3.5.6.4.2 I^2C Bus

The I^2C (Inter-Integrated Circuit) bus communicates module part number, serial number, and revision history information to the AE-37( ) Controller.

3.5.6.4.3 I/O and RCV Enable

In a hot-standby system, an I/O ENABLE signal from the controller turns on the DS1/E1 output drivers in the RCV circuits on the on-line module and turns off the output drivers on the redundant off-line I/O interface module. The RCV ENABLE signal from the controller turns on the MX X/Y 1-4 rail drivers on the inputs to LIO ASIC and turns on the repeater X/Y rail drivers (RCV X/Y DATA T/F 1-4) on the output of LIO.

3.5.6.4.4 Loopback Controls

Refer to loopback information on the Control screen for details. To access the Control screen:

1. Click here to enter Controls guide. Main screen will open.
2. On the Main screen, on dropdown for type of radio, click on DS1. DS1 Status Alarm screen will open.
3. On DS1 Status Alarm screen, on tool bar, click on User Control. User control screen will open.
4. On User Control screen, click on loopback function.

3.5.6.4.5 Alarms

- I/O FAIL – red LED, indicates loss of signal, bipolar violation detected, or failure on one of the active DS1/E1 lines.
- SYNC FAIL – red LED, indicates a transmit synchronization failure between I/O interface modules in a hot-standby configuration.
- RCV FAIL – red LED, indicates a loss of receive frame synchronization.
- COMMON LOSS ALARM – red LED, indicates a far end transmit common loss alarm. A transmit Common Loss Alarm (CLA) is generally an indication of a silent failure (no alarm activated) at the transmitter. The common loss alarm, generated by the AE-37( ) Controller, triggers when both A-side and B-side downstream receivers have a radio frame loss or channel failure. In a hot-standby hop, loss of both receivers initiates a request to switch to the standby transmitter, even though no transmit alarms are present. If the path is nominal, the transmitter switches in 5 seconds. If the path is in a fade (ATPC is in active range), the transmitter switches in 30 seconds. If the downstream alarms clear within 5 seconds, a CLA is initiated on the off-line side to indicate a silent transmit failure. If alarms still exist, the transmitter continues to switch every 30 seconds. This process continues until the receive alarms clear, but no CLA is activated.

3.5.6.4.6 Status

- I/O ON LINE – green LED, indicates the module is in service.

3.5.7 DX-35N-1 DS3 I/O Interface

The DX-35N I/O Interface multiplexes/demultiplexes up to three DS3 channels, P/N data pairs, and service channel data in the MDR-8000 radio. The DX-35N-1 (PN 3DH 03169 AA) operates with North American data rates.

There are two capacity/modulation versions and three generations of I/O interface modules. The different versions and generation modules functionally perform the same. The differences include front panel controls and DADEing requirements.

3.5.7.1 Capacity/Modulation Versions

The DS3 I/O interface module is available in a 1 or 3-line 64 QAM version or a 2-line 32 TCM version. The 2-line 32 TCM version of the modules, introduced in the second generation, are typically used for applications in the 6.875 to 7.125 GHz Broadcast Auxiliary Service Band. The typical RF bandwidth for this 2-line application is 25 MHz. The RF bandwidth requirement for 3 DS3 lines is 30 MHz.

3.5.7.1.1 First Generation

The first generation modules (part number 3DH03169AA, AB, and AG) require both radio and line DADE, manually, using the front panel controls.

3.5.7.1.2 Second Generation

The second generation modules (part number 3DH03169AH, and AJ) have automatic line DADE capability. Manual radio DADE is required using the front panel controls. Second generation modules can be mixed and matched with the first generation modules that have the same modulation scheme, however when mixed in the same shelf, both radio and line DADE must be performed manually.

3.5.7.1.3 Third Generation

The third generation modules (part number 3DH03169AK, AL, AM, and AN) have automatic radio and line DADE capability. Third generation modules with AK and AL variants have front panel controls. Third generation modules with AM and AN variants do not have front panel controls.

Third generation modules with part numbers 3DH03169AK and AL can be mixed and matched in the same shelf with first, second, and third generation modules that have the same modulation scheme. When third generation modules with AK and AL variants are mixed with first generation modules, both radio and line DADE must be performed. When AK and AL modules are mixed with second generation modules, only radio DADE must be performed. Radio DADEing may be required when a third generation AK is matched with another AK module or AL is matched with another AL module. This requirement is configuration dependent. Refer to Chart 3 DS3 I/O Interface Removal and Replacement procedure in the Maintenance section for details. No DADEing is required when mixing third generation modules with AM and AN variants with other third generation modules.

See Figure 3-27 for to/from signal information and application information.The DS3 I/O Interface consists of several functional blocks each of which is described in the following paragraphs.

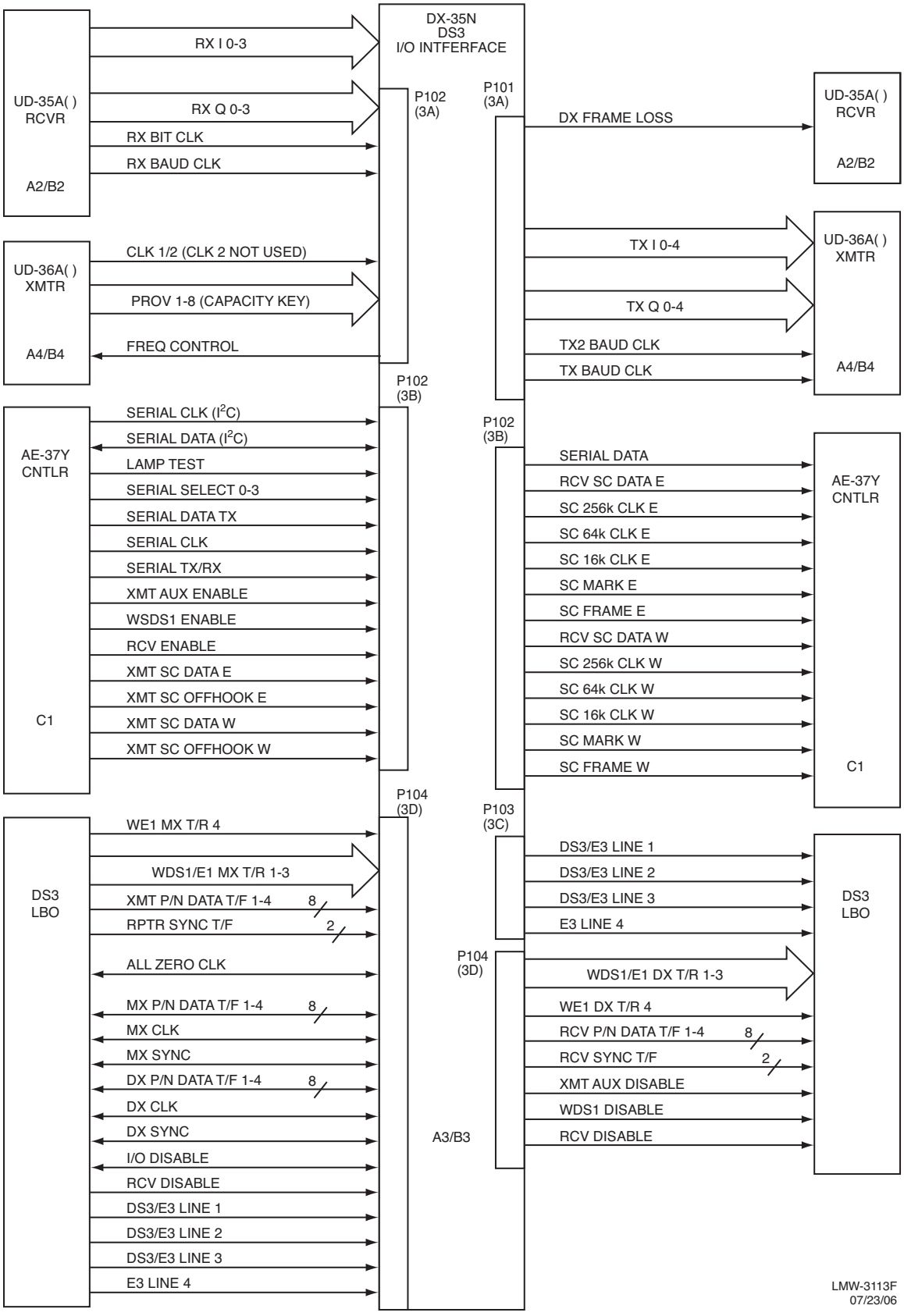


Figure 3-27 DX-35N DS3 I/O Interface Interconnect Diagram

3.5.7.2 Multiplex Signal Flow

The DX-35N DS3 I/O Interface multiplexes three DS3 data streams of primary traffic, three DS1 data streams of secondary traffic (wayside DS1/E1), and low-speed data streams for miscellaneous signaling and communication, creating the radio frame output I/Q data.

The XMT circuits (Figure 3-28) receive DS3 data, auxiliary (overhead data), and a reference sync signal. The overhead data contains a 262 kb/s service channel, a 1.544 Mb/s WDS1 per each DS3, and two 16 kb/s command path channels. (The 262 kb/s SC data interfaces from the service channel muldem where four 64 kb/s data streams are multiplexed into the 262 kb/s SC data stream.) A UNIXMT gate array multiplexes/encodes these inputs to form parallel I, Q data signals, and clock.

3.5.7.2.1 DS3 Interface

The DX-35N contains three identical DS3 interface circuits. A fourth identical interface circuit is wired but not used. The DS3 signals are applied to the DS3 interface circuits via connector P103. Each interface circuit consists of a DS3 processor that converts the bi-polar DS3 data into positive (P) and negative (N) uni-polar digital pulses and recovers the clock (CK) used to clock the data into the UNIXMT ASIC.

The P and N data clocked into the UNIXMT ASIC is B3ZS decoded and frame synchronized. Parity violations are monitored and removed from the data. The data is passed through an elastic buffer and then multiplexed with the overhead data. The multiplexed data is scrambled, differentially and gray encoded, and converted to I and Q data. The I and Q data is applied to the XMT EPLD for FEC. The UNIXMT ASIC also creates low-speed clock (MCK) from the recovered DS3 clock that is used to clock wayside DS1 data (MDT) and stuffing signals (MSR) into the UNIXMT ASIC.

3.5.7.2.2 Forward Error Correction (FEC)

The XMT EPLD performs XMT FEC functions on the I and Q signals from the UNIXMT ASIC. The encoding function uses the Nakamura Single Lee Error Correcting (SLEC) codes. One 3-bit symbol is added by ENFEC to the I channel data and to the Q channel data every 27 data symbols, increasing the bit rate from 81 to 84. Removal of the 3-bit symbols, correcting the data, and decoding are functions of the UNIRCV ASIC, described later in this section.

The TX I (2:0) and TX Q (2:0) data is applied to the transmitter module via connector P101.

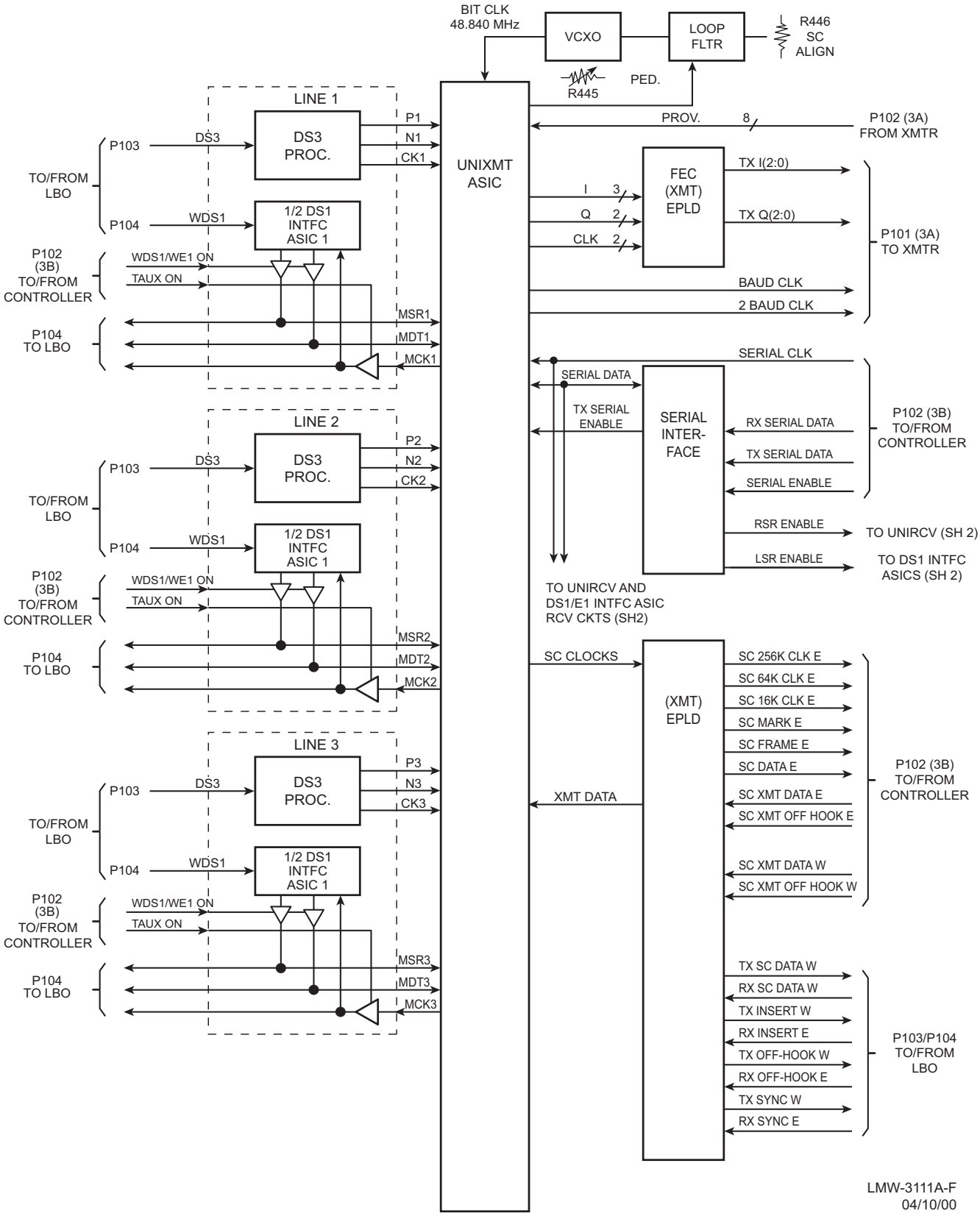


Figure 3-28 DX-35N DS3 I/O Interface Functional Block Diagram (Sheet 1 of 2)

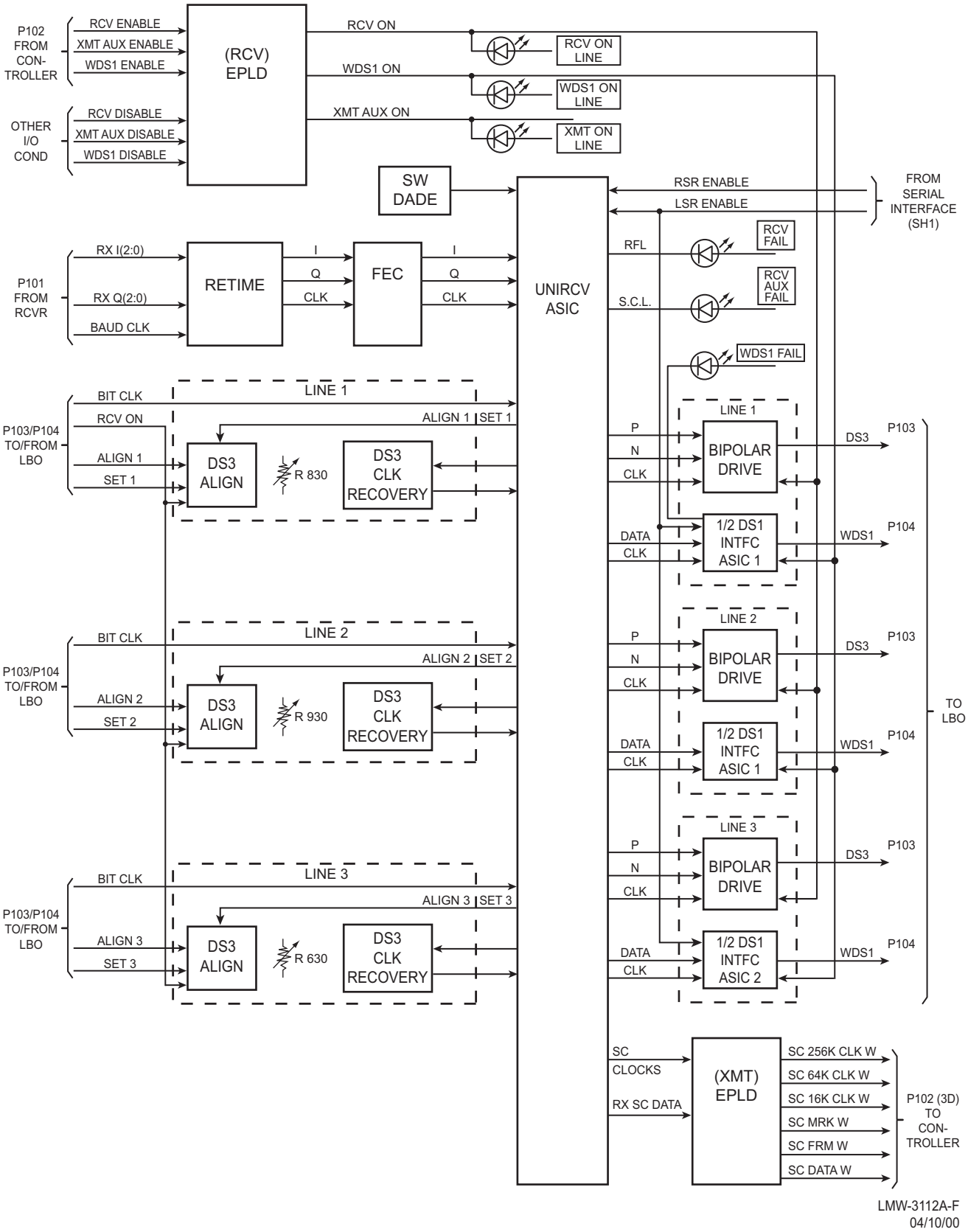


Figure 3-28 DX-35N DS3 I/O Interface Functional Block Diagram (Sheet 2 of 2)

3.5.7.2.3 Wayside DS1 Interface

The wayside DS1 interface circuits use one-half of a Leghorn ASIC to provide clock recovery, clock smoothing, elastic buffering and line encoding for each wayside DS1 (WDS1) channel. Each DS1 interface circuit is controlled by the WDS1 ON and TAUX ON inputs from the AE-37Y-1 controller module. The WDS1 ON control signal turns on the driver that supplies the MCK( ) to the DS1 interface circuits. The TAUX ON control signal turns on the output drivers that provide WDS1 data (MDT) and stuff requests (MSR) to the UNIXMT ASIC, and in protected systems, to the off-line I/O conditioner module (P104).

The wayside DS1 tip and ring signals (WSDS1-1 MXT and WSDS1-1 MXR) are applied to the DS1 interface circuits via connector P104. The balanced tip and ring signals consist of pulsed square waves at 1.544 Mb/s. The DS1 interface circuit bridges the RZ data onto one channel, converts the balanced tip and ring signals to NRZ data, B3ZS encodes the data, and using the recovered clock, writes the data into an elastic buffer. In the elastic buffer, the recovered clock is compared to the low-speed clock (MCK) created by the UNIXMT ASIC and if a mismatch is detected, stuffing bits are inserted. The output of the DS1 interface circuit is clocked into the UNIXMT ASIC by the low-speed clock (MCK) generated by the UNIXMT ASIC.

3.5.7.2.4 Service Channel Interface

Service channel data is processed by the XMT EPLD. The XMT EPLD receives east and west insert service channel data (RX SC DATA E and W) and sync signals (RX SYNC E and W) from the LBO via connectors P103 and P104. The XMT EPLD receives through service channel data from the AE-37Y-1 controller module via connector P102. The through service channel data consists of the clocks (SC 256K, 64K, and 16K CLK E and W) mark and frame bits (MARK and FRAME E and W), and off hook clocks (SC XMT OFF-HOOK E and W).

In the XMT EPLD, the service channel insert data is clocked into time slots in the through data stream by the SC XMT OFF-HOOK E and/or W signals to provide the XMT DATA output to the UNIXMT ASIC. The service channel insert data is inserted into the radio frame overhead when the off-hook command is active high. The through-data is inserted into the radio frame overhead when the off-hook command is active low. If there is no insert service channel data, the through data is passed to the UNIXMT ASIC, and vice versa.

3.5.7.2.5 Clock Source and Sync

Note

When provisioned as a terminal, the A-side I/O interface is automatically put on pedestal and the B-side I/O interface automatically locks to the A-side I/O interface. When provisioned as a repeater, both A and B sides (on-line and off-line) sync to the recovered clock. Loss of sync causes the I/O interface to be put on the fixed pedestal voltage.

A Phase Locked Loop (PLL) controls the frequency of the Voltage Controlled Crystal Oscillator (VCXO) generated clock (48.840 BIT CLK) that is the clock source for the UNIXMT ASIC. See Figure 3-29. The PLL consists of the Voltage Controlled Crystal Oscillator (VCXO), a phase detector circuit in the UNIXMT ASIC, an analog MUX, an activity detector circuit, and a loop filter. The UNIXMT ASIC generates clocks from the BIT CLK that enable the UNIXMT to multiplex DS3, DS1, AUX channels, and overhead, generating the radio frame.

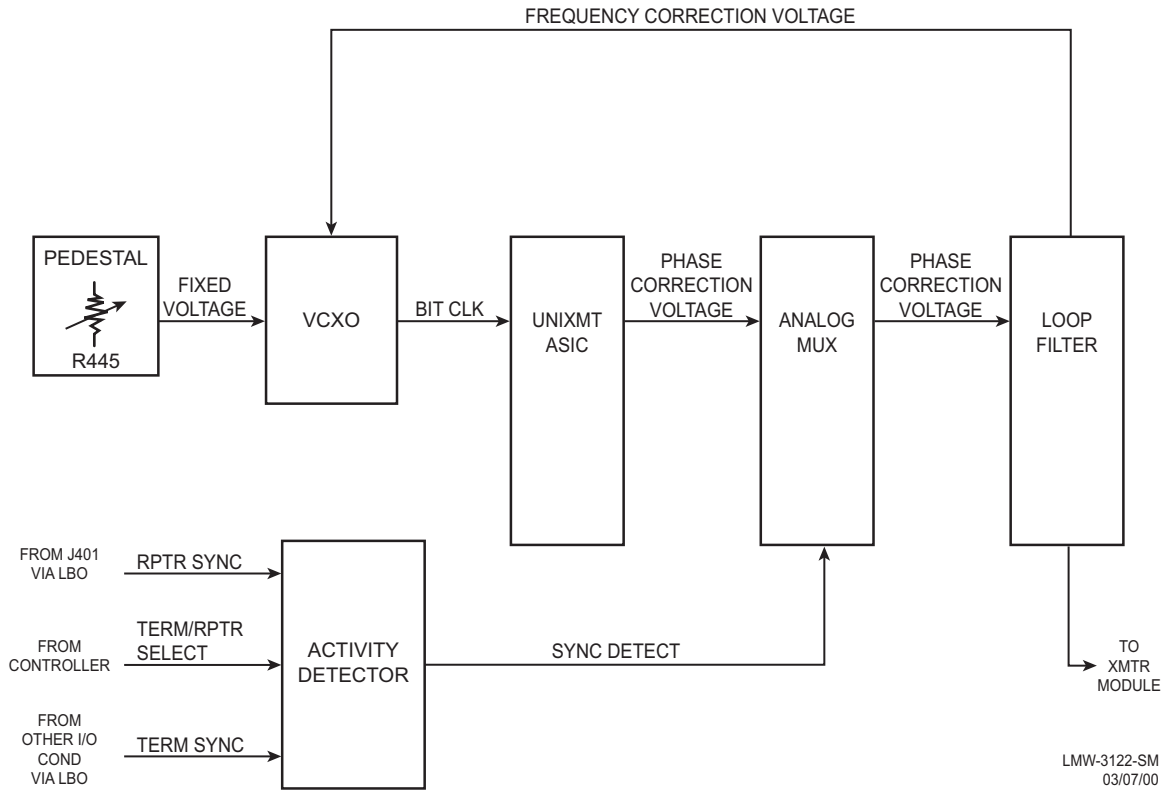


Figure 3-29 Phase-Lock Loop Functional Block Diagram

The 48.840 BIT CLK is phase detected by the phase detector circuit in the UNIXMT ASIC and a resulting correction voltage is applied to the analog MUX. The analog MUX is controlled by the SYNC DETECT signal from the activity detector. Activity detected on the RPTR SYNC input or TERM SYNC input turns on the analog MUX and the correction voltage from the UNIXMT ASIC is applied to the loop filter. The loop filter completes the PLL by looping the correction voltage to the VCXO, correcting the frequency of the BIT CLK. If no activity is detected by the activity detector on the RPTR SYNC input or TERM SYNC input. the analog MUX is turned off, and the correction voltage path to the loop filter is opened. This action places the VCXO under pedestal voltage control. The pedestal voltage is factory adjusted for VCXO center frequency by potentiometer R445.

The TERM/RPTR control line selects the TERM or the RPTR SYNC input to the activity detector. This is a software control and automatically selects the input when TERM or RPTR is provisioned on the USI screen.

The loop filter provides a FREQ CONTROL output to the capacity key located in the XMTR module to sync the VCXO (clock source) in the XMTR module to the VCXO in the I/O conditioner.

3.5.7.3 Demultiplex Signal Flow

The DX-35N DS3 I/O Interface RCV circuits (Figure 3-28) receive parallel I, Q data signals (RX I and Q 2:0), and BAUD CLK from the RCVR module. The UNIRCV ASIC demultiplexes/decodes these inputs to form DS3 data, auxiliary (overhead data), and a reference sync signal. The overhead data contains a 262 kb/s service channel, a 1.544 Mb/s WDS1 per each DS3, and two 16 kb/s command path channels.

3.5.7.3.1 RCVR Interface

RCVR module interface circuits consist of a retime circuit and FEC circuit. RX I (2:0) and RX Q (2:0) signals from the RCVR are clocked into the retime circuit by the BAUD CLK. The retime circuit retimes the I and Q signals to the baud clock and the I and Q signals are applied to the FEC circuit. The FEC circuit removes the FEC encoding that was placed on the data stream by the MDR-8000 XMTR. The I and Q outputs are clocked out of the FEC circuit and into the UNIRCV ASIC by the CLK.

3.5.7.3.2 UNIRCV ASIC

The UNIRCV ASIC performs differential and gray decoding for 64 QAM, descrambling, radio frame detection and alignment, extracting service channel and DS1 overhead channels, elastic buffering, DS3 frame detection and B3ZS encoding, PVMR, data rate adjustment to interface with FEC array, and phase/frequency detection and alignment signal generation.

3.5.7.4 DS3 Interface

The DX-35N contains three identical DS3 interface circuits. A fourth identical interface circuit is wired but not used. Each DS3 interface circuit consists of a DS3 alignment circuit, DS3 clock recovery circuit, and a bipolar drive circuit.

3.5.7.4.1 DS3 Clock Recovery

The DS3 clock recovery circuit recovers the DS3 clock from the I and Q inputs to the UNIRCV ASIC. The UNIRCV ASIC uses the DS3 clock to clock the P and N data out of the UNIRCV ASIC to the bipolar drive circuits.

3.5.7.4.2 Bipolar Drive

The bipolar drive circuits convert the framed P and N input signals into framed DS3 data. The circuits are enabled by the RCV ON output of the RCV EPLD. The DS3 outputs are routed through connector P103 to the DS3 LBO.

3.5.7.4.3 DS3 Alignment Circuit

For errorless switching, SET and ALIGN lines are connected between the A- and B-side I/O conditioner modules. The SET input is used to synchronize the B3ZS encoder of the off-line channel to the on-line channel for errorless switching. The ALIGN input is used to synchronize the DS3 framing of the off-line channel to the DS3 of the on-line channel for errorless switching.

3.5.7.4.4 DADE

Each DS3 data line for the radio has adjustable delay processed in the UNIRCV gate array. This allows factory DADE alignment using S2 ALIGN switch.

3.5.7.4.5 UNIRCV VMR

Parity bits are continuously monitored and a parity error pulse is generated when a mismatch is detected. If the VMR (Violation Monitor and Removal) is enabled (by the controller through the serial interface) parity bits are replaced with new calculated parity bits. Otherwise they are not changed.

3.5.7.4.6 UNIRCV Blue Signal

The blue signal detector is enabled when DS3 is out of frame. The blue signal generated is a DS3 frame with valid framing bits, C bits set to zero, and information bits have a 101010..... pattern.

3.5.7.4.7 UNIRCV AIS

The AIS detector is enabled when DS3 is out of frame. The AIS generated is an unframed all 1's pattern.

3.5.7.5 Wayside DS1 Interface

The DX-35N contains three identical wayside DS1 interface circuits. A fourth identical interface circuit is wired but not used. Each DS1 interface circuit uses a Leghorn ASIC (hereafter referred to as DS1 interface ASIC) for DS1 signal processing. The demultiplex section of each DS1 interface ASIC receives 6.312 MHz data (2DXDT, containing four channels of DS1 data), a 1.544 DEMUX gapped clock (DXCK), the 49 MHz reference clock (49 MHZ), and a 1.544 MHz MUX gapped clock (DXCK). Normally the DEMUX clock is used. In an out of frame condition the integrity of the DEMUX clock is lost and the MUX clock is selected. The 6.312 MHz NRZ data and destuffed gapped clock are retimed by the 49 MHz reference clock. The data is then clocked by the gapped clock to remove the appropriate two channels of data. The two channels of data are clocked into an elastic buffer by the gapped clock. The data is then converted to a quasi-RZ format and encoded, according to the modulation mode. The encoded data is sampled in an AIS detector for loss of signal, demultiplexed onto two (T&R) channels, and converted to RZ data. TEO (trailing edge overshoot) pulses are added to the RZ data so that the pulses conform to cross-connect requirements without the need of an external equalizer. Tip and ring outputs for each channel (DS1 Chan 1-4 Out T/R) are applied to DS1 LBO circuits on the MDR-8000 DS3 LBO module via connectors P103 and P104.

3.5.7.6 Service Channel Interface

Service channel data from the UNIRCV ASIC is clocked into the XMT EPLD by the 256K CLK in the SC CLKS. The XMT EPLD separates and applies the SC 256K, 64K, and 16K CLK E and W, MARK and FRAME E and W, and SC DATA E and W to AE-37Y-1 controller module via connector P102.

3.5.7.7 Control and Monitor Functions

3.5.7.7.1 Serial Interface

The serial interface is used to transfer alarm and status information to the AE-37( ) Controller. It is also used to receive control information from the AE-37( ) Controller.

Alarms generated in the UNIXMT ASIC are latched in the serial interface until they are acknowledged by the system controller. Alarms provided for each DS3 line are loss of input, buffer spill, and frame alarm. Status provided for each DS3 line are summary line and blue signal detect. A counter is provided for each DS3 line, which counts parity errors.

Data is sent and received during a two-byte transfer. The first byte is a poll byte that selects the device ID and register address. It also controls whether a read or write operation is taking place. The second byte contains data from the selected register.

3.5.7.7.2 Provisioning Inputs

- Provisioning inputs (PROV 1-8) from capacity keys on the XMTR and RCVR modules, control the following functions:
- Select 64 QAM modulation scheme.
- Select local oscillator control source (pedestal voltage or PLL).
- Select DS3 operation and number of DS3 lines enabled.
- Select data scrambler or passes data through unmodified.
- Select stuff rate source for stuffing DS1/E1 signals in radio frame (average stuff rate or stuff request signals from Leghorns).
- Enables or disables data scrambler stuck pattern (all 1's, all 0's, or alternating 1's and 0's).

3.5.7.7.3 I^2C Bus

The I^2C (Inter-Integrated Circuit) bus communicates module part number, serial number, and revision history information to the AE-37( ) Controller.

3.5.7.7.4 ON-Line / Off-Line Enable / Disable

In a hot-standby system, a XMT AUX ENABLE, RCV ENABLE, and WDS1 ENABLE signals from the AE-37Y Controller module turn on the respective XMT, RCV and wayside DS1 circuits on the on-line DS3 I/O interface module. This results in XMT AUX DISABLE, RCV DISABLE, and WDS1 DISABLE signals being generated in the on-line I/O conditioner that turn off the respective circuits in the off-line DS3 I/O interface module.

3.5.7.7.5 Loopback Controls

3.5.7.7.6 Alarms

Refer to loopback information on the Control screen for details. To access the Control screen:

1 Click here to enter Controls guide. Main screen will open.

2 On the Main screen, on dropdown for type of radio, click on DS3. DS3 Status Alarm screen will open.

3 On DS3 Status Alarm screen, on tool bar, click on User Control. User control screen will open.

4 On User Control screen, click on loopback function.

- I/O FAIL – red LED, indicates loss of signal, bipolar violation detected, or failure on one of the active DS1/E1 lines.
- SYNC FAIL – red LED, indicates a transmit synchronization failure between I/O interface modules in a hot-standby configuration.
- RCV FAIL – red LED, indicates a loss of receive frame synchronization detected by UNIRCV ASIC.
- RCV SC FAIL – red LED, indicates a loss of service channel receive frame synchronization detected by UNIRCV ASIC.
- WDS1 FAIL – red LED, indicates loss of signal, bipolar violation detected, or failure on one of the active WDS1 lines.

3.5.7.7.7 Status

- RCV ON LINE - green LED, indicates UNIRCV circuits are enabled, allowing transfer of data to DS1 interface circuit.
- XMT ON LINE - green LED, indicates UNIXMT circuits are enabled, allowing transfer of data to encoder/decoder circuits.
- WDS1 ON LINE - green LED, indicates DS1 interface circuit output drivers are enabled.

3.5.8 DX-35P-1 OC3/STM-1 I/O Interface

The DX-35P I/O Interface multiplexes/demultiplexes up to three STS1 channels (OC3/STM-1), wayside DS1/E1, and service channel data in the MDR-8000/i/s radio. Two types of DX-35P are available to comply with wayside DS1 and E1 data rates. The DX-35P-1 accepts wayside DS1. The DX-35P-2 accepts wayside E1. Both types accept multimode and single mode fiber.

See Figure 3-30 for to/from signal information and application information. The DS3 I/O Interface consists of several functional blocks each of which is described below.

3.5.8.1 Adjacent I/O Interface Module Interface

The adjacent I/O interface module interface at connector J3E.

3.5.8.1.1 Signal Crossover

See Figure 3-31. Crossover occurs in a framer on the SMCRA in Optical Receive (OR) and Radio Receive (RR) directions. Optical RCV crossover signals include OR DATA, OR PARITY, OR FRAME, and OR 39CLK. Radio RCV crossover signals include Optical XMT (OT) DATA, and OT SYNC.

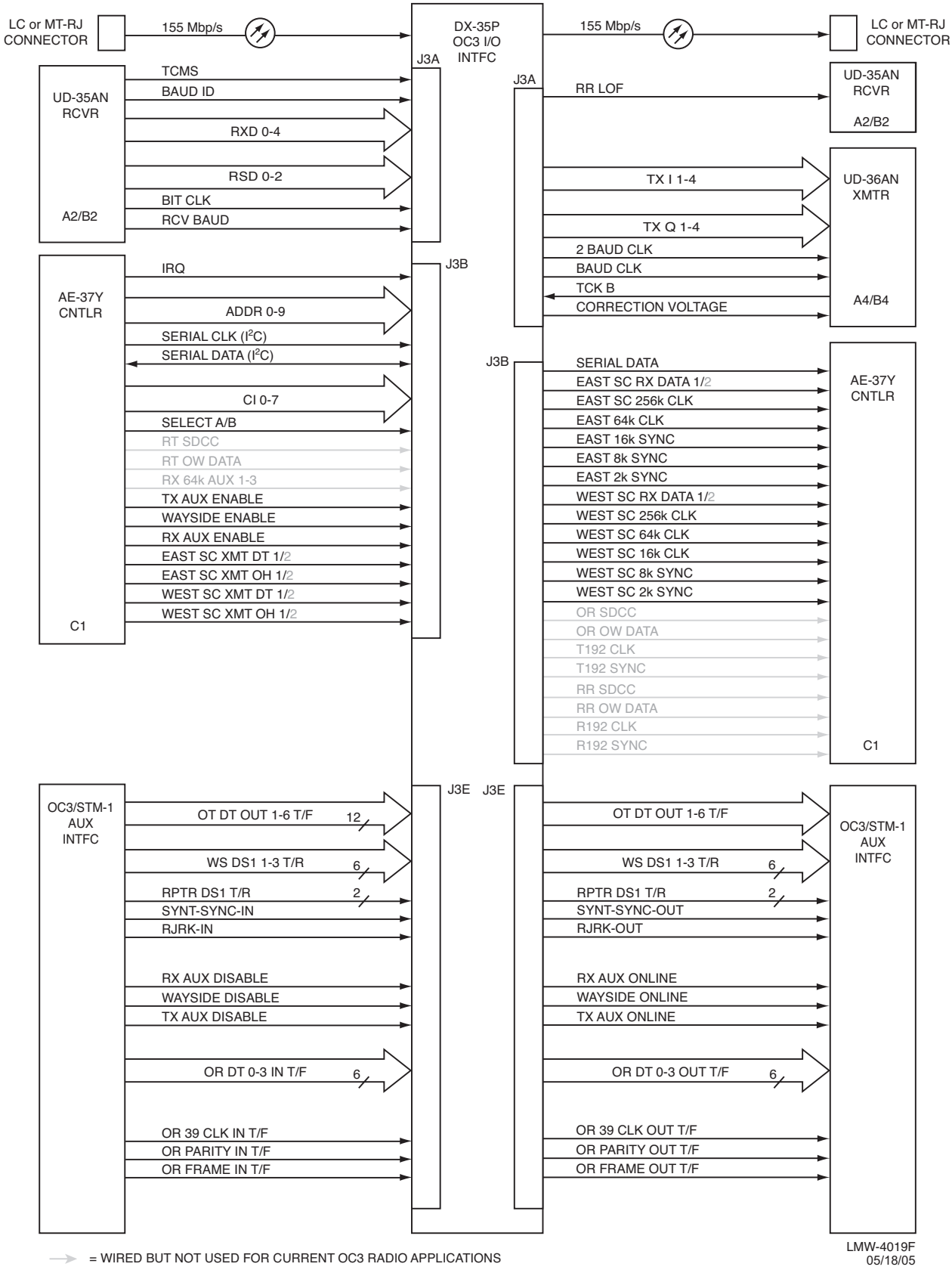


Figure 3-30 DX-35P OC3/STM-1 I/O Interface Interconnect Diagram

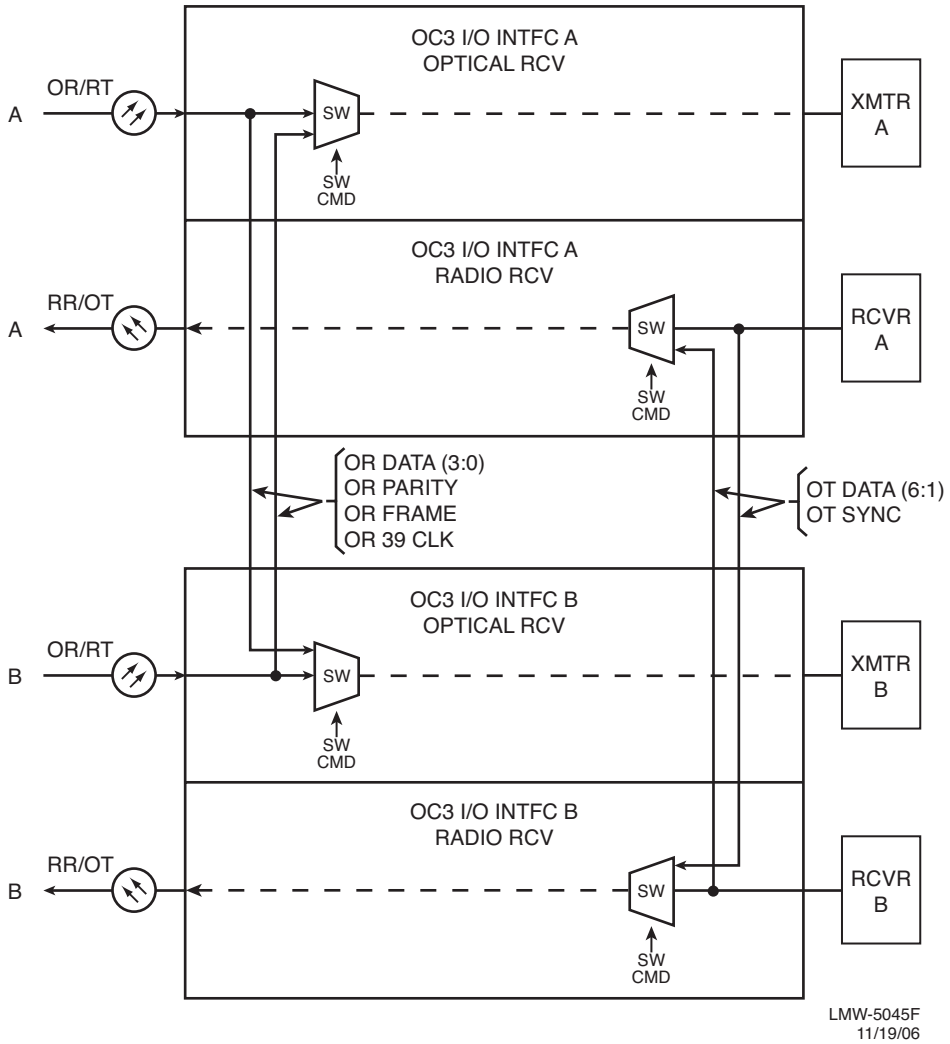


Figure 3-31 OC3/STM-1 Crossover Functions Simplified Functional Block Diagram

3.5.8.2 Optical RCV/Radio XMT Signal Flow

See Figure 3-32. The DX-35P I/O interface receives the OC3 optical signal on the front panel and routes the optical signal to the laser hybrid. The laser hybrid converts the optical data into an electrical data stream at 155 mb/s. The data stream is applied to the clock recovery circuit. In the clock recovery circuit, a 39 mb/s clock is separated from the data stream. The clock is used to clock the serial data into the 4 X 39 translator circuit. The 4 X 39 translator separates the applied data in the data stream into four data streams, each containing 4-bit nibble data at 39 mb/s. The nibble data is applied to the SONET Media Converting Regenerator Array (SMCRA). The SMCRA multiplexes the nibble data with data from the serial service channel interface and converts the multiplexed data, first to STS1 and then X/Y data streams. The X/Y data is buffered in an elastic buffer and then applied to a multiplexer. In the multiplexer the X/Y data is combined with overhead data and the serial data is applied to a scrambler. The scrambled X/Y data is applied to a Forward Error Correction (FEC) encoder circuit. Forward Error Correction (FEC) is provided using Trellis Coded Modulation and Reed-Solomon coding. The encoded X/Y data steams are converted to I and Q data steams that are clocked out of the SMCRA by the T CLK B input from the XMTR module. The TX I 1-4 and TX Q 1-4 data is applied to the transmitter module via connector J3A.

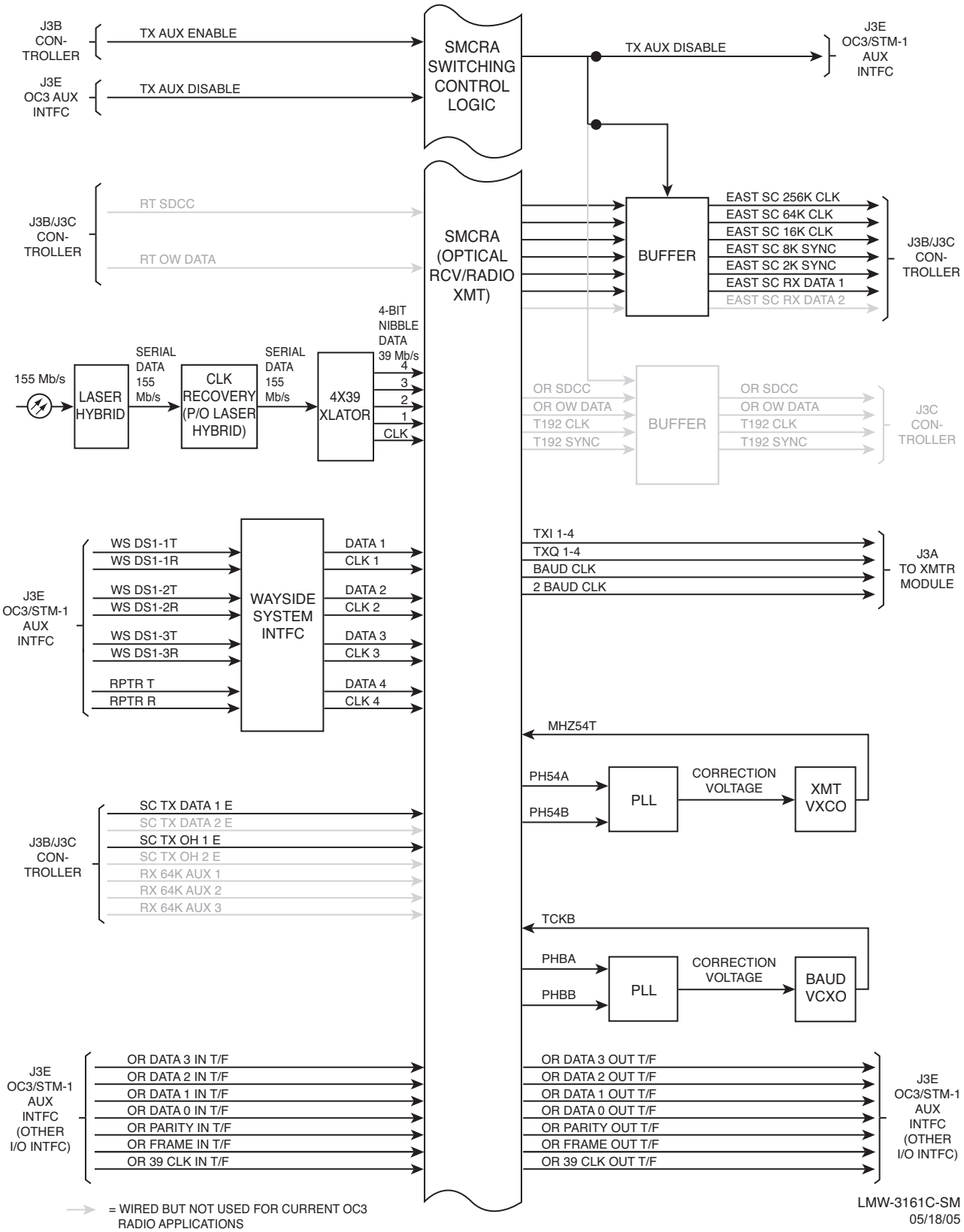


Figure 3-32 DX-35P OC3/STM-1 I/O Interface Functional Block Diagram (Sheet 1 of 3)

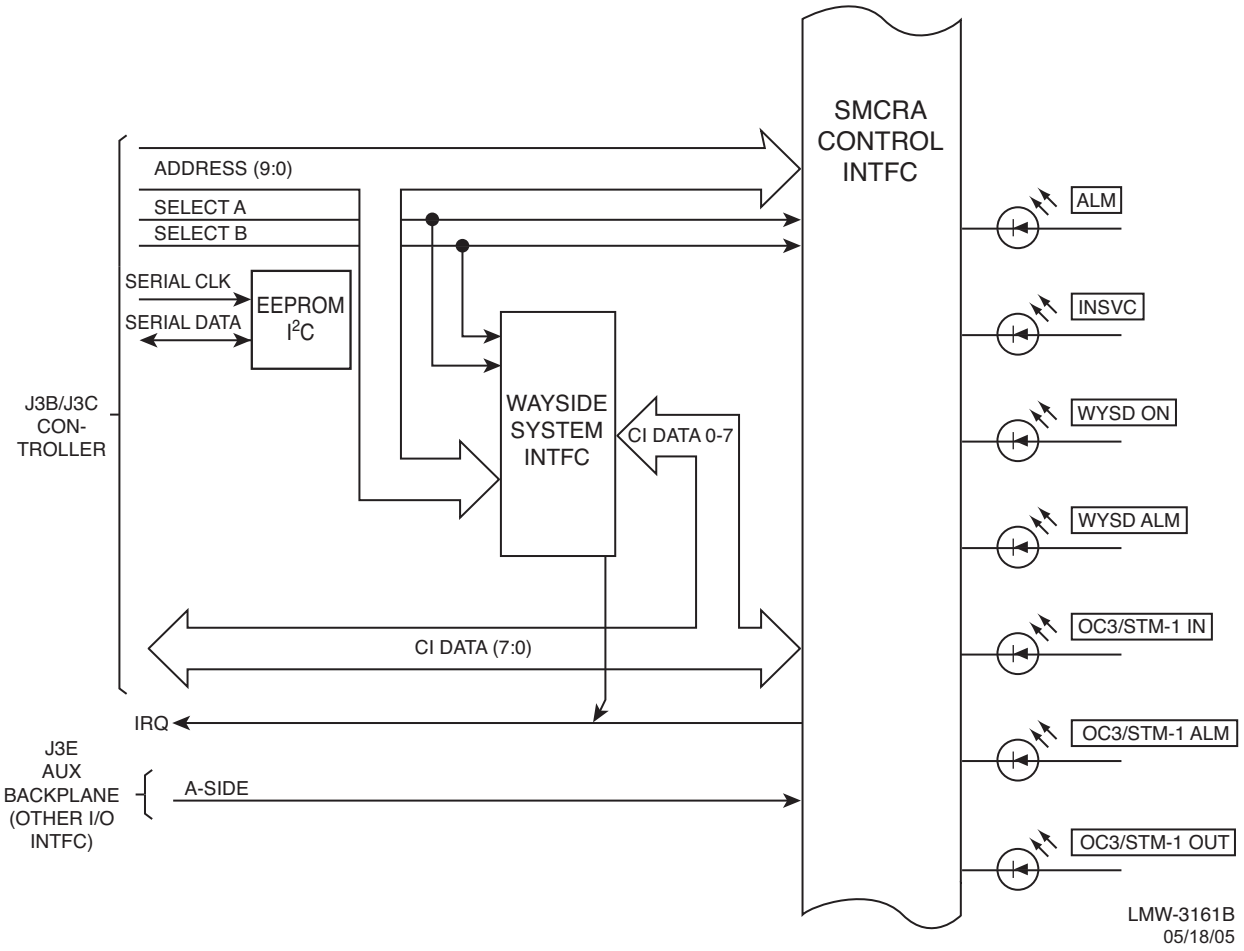


Figure 3-32 DX-35P OC3/STM-1 I/O Interface Functional Block Diagram (Sheet 2 of 3)

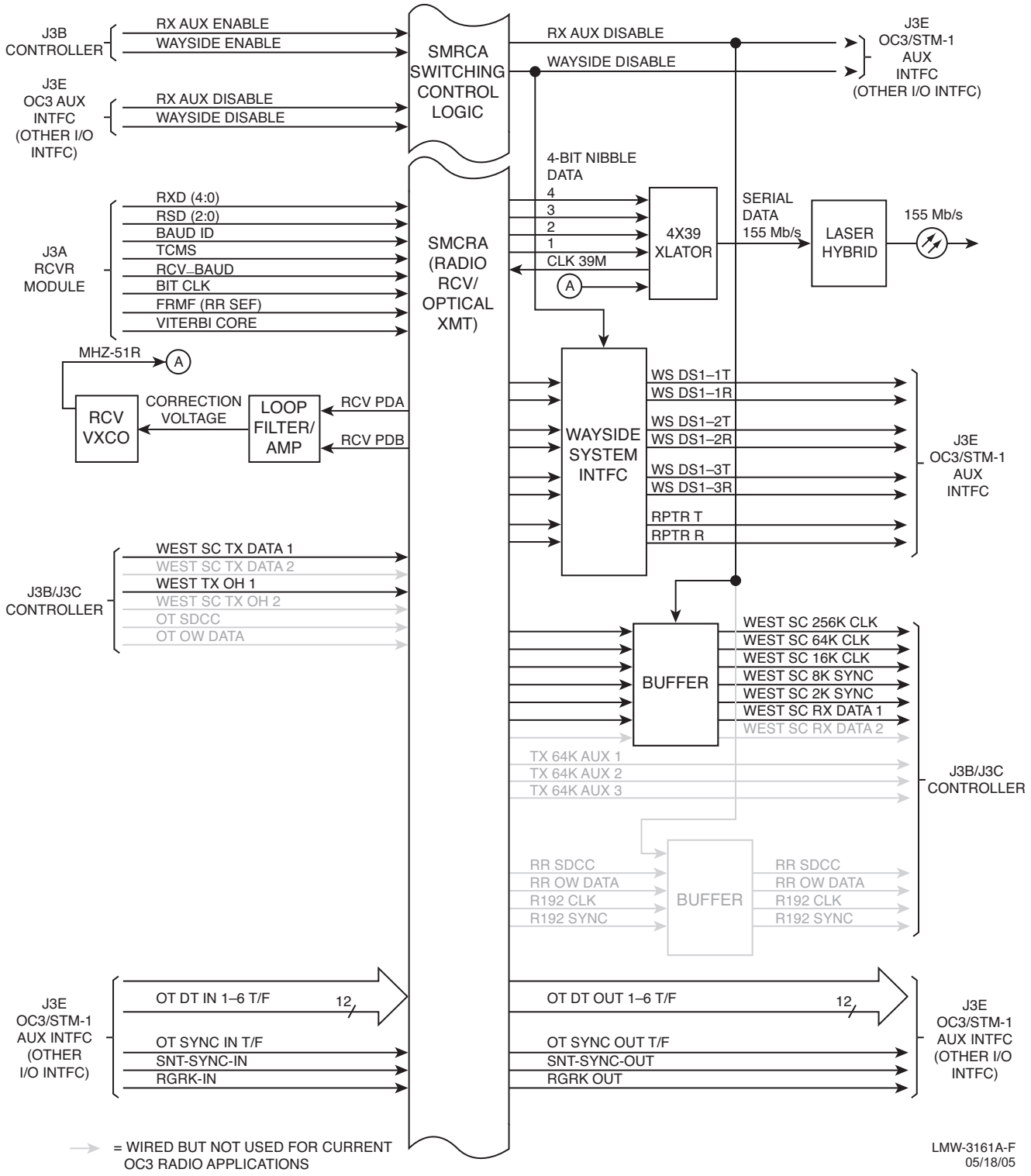


Figure 3-32 DX-35P OC3/STM-1 I/O Interface Functional Block Diagram (Sheet 3 of 3)

3.5.8.2.1 RCVR Module Interface

The RCVR module interface at connector J3A consists of Receive Data (RXD), Receive Subset data (RSD), BAUD Identification (ID), Trellis Code Modulation Sync (TCMS), Receive BAUD clock (RCV BAUD), Bit Clock (CLK), (FRMF) and Viterbi Correcting Errors (VITERBI CORE).

3.5.8.2.2 Wayside DS1 Interface

The wayside DS1 interface circuit provides clock recovery, clock smoothing, elastic buffering and line encoding for each wayside DS1 (WS DS1-1-3 T/R) channel.

The wayside DS1 tip and ring signals (WS DS1-1T and WS DS1-1R) are applied to the DS1 interface circuits via connector J3E. The balanced tip and ring signals consist of pulsed square waves at 1.544 Mb/s. The DS1 interface circuit bridges the RZ data onto one channel, converts the balanced tip and ring signals to NRZ data, B3ZS encodes the data, and using the recovered clock, writes the data into an elastic buffer. In the elastic buffer, the recovered clock is compared to the low-speed clock created by the SMCRA and if a mismatch is detected, stuffing bits are inserted. The DATA 1-4 outputs of the DS1 interface circuit are clocked into the SMCRA by the respective four output clocks (CLK 1-4) .

3.5.8.2.3 Service Channel Interface

Figure 3-33 and Figure 3-34 show XMT and RCV signal flow. Refer to service channel demultiplex description later in this section for RCV details. The DX-35P receives inserted service channel 1 data from the AE-37Y-1 controller module via connector J3B. Service channel 2 data from the controller is wired (J3C) but not used for the OC3/STM-1 radio applications.

3.5.8.2.3.1 Terminal

See Figure 3-33. At a terminal, the service channel interface at the SMRCA in the I/O interface consists of the EAST SC XMT DT input and EAST SC CLKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST SC 8K SYNC, and EAST SC 2K SYNC) outputs. The EAST SC XMT DT input consists of four 64kb/s channels multiplexed into a single 256 kb/s signal.

Overhead MUX circuitry in the SMRCA receives local insert-service channel data (EAST SC XMT DT) from the service channel muldem in the controller module. The EAST SC XMT DT is clocked into the SMCRA by the controller using the EAST SC CLOCKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST SC 8K SYNC, and EAST SC 2K SYNC) provided by the SMCRA. In the SMCRA, the service channel insert data (EAST SC XMT DT) is inserted into the radio frame overhead.

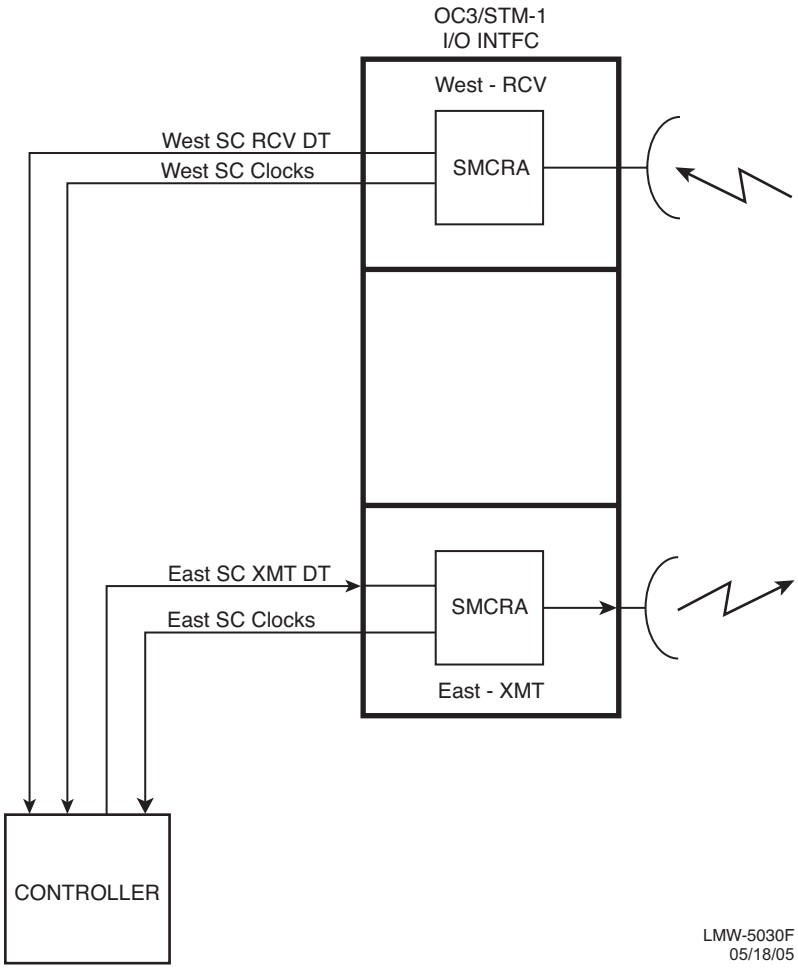


Figure 3-33 OC3/STM-1 Terminal Service Channel Signal Flow

3.5.8.2.3.2 Repeater

The service channel interface at the SMRCA in rack 2 I/O interface consists of the EAST SC XMT DT and EAST SC XMT OH inputs and EAST SC CLKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST SC 8K SYNC, and EAST SC 2K SYNC) outputs, and rack 1 data input via the RPTR cable. Each data (DT) input and output consists of four 64kb/s channels multiplexed into a single 256 kb/s signal.

When EAST SC XMT OH is low (No off hook from rack 2 controller) data received over the repeater cable by the frame in/frame out (FIFO) circuit (EAST SC RCV DT) is passed through the MUX and inserted into the radio frame overhead.When EAST SC XMT OH is high (off hook), EAST SC RCV DT is clocked into the rack 2 controller by the EAST SC CLKS. The rack 2 controller multiplexes the EAST SC RCV DT with local insert-data and the combined signal (EAST SC XMT DT) is passed through the MUX and inserted into the radio frame overhead.

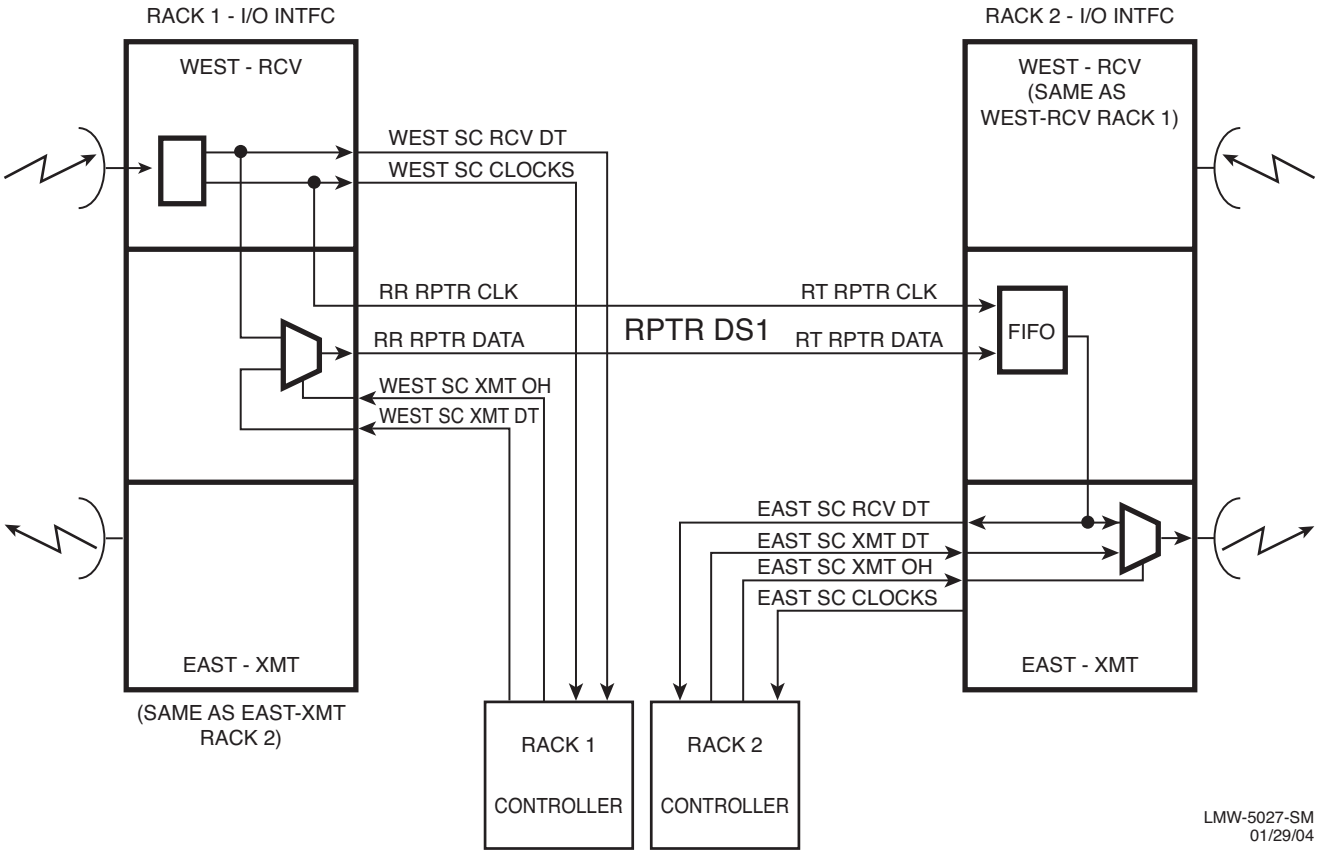


Figure 3-34 OC3/STM-1 Repeater Service Channel Signal Flow

3.5.8.2.4 Clock Source and Sync

The I/O interface locks to the incoming fiber. It is only put on pedestal upon LOS or LOF alarm.

3.5.8.2.5 Normal Operation

The 39 MHz clock, recovered from the fiber input is used for front-end SMCRA function (all functions before the elastic buffer). The 39 MHz clock is used to perform frame sync, LOS, LOF, and B1 Bit error checks in framer. Crossover occurs after the framer.

3.5.8.2.6 XMT VCXO

The input clock (MHZ54T) from the XMT VCXO is used to generate radio XMT STS1 data, sync, and clock. A Phase Locked Loop (PLL) controls the frequency of the Voltage Controlled Crystal Oscillator (VCXO) generated clock that is the clock source for SMRCA XMT functions. The PLL consists of the Voltage Controlled Crystal Oscillator (VCXO). a phase detector circuit in the SMCRA, a loop filter/amplifier.

Phase Detector A/B (PH54A/B) complimentary outputs provide relative phase difference between pointers in STS elastic buffer. The phase difference is converted to a correction voltage in the PLL to control the frequency of the VCXO.

3.5.8.2.7 Holdover

When LOS or LOF is declared, the holdover condition is enabled. The SAMPLE voltage from the loop amplifier holds the oscillator to the frequency at the time the alarm occurred. The oscillator stays close to frequency and then over time slowly migrates to pedestal.

The SAMPLE voltage is applied to the holdover switch circuits and is switched to the analog MUX. The analog MUX selects the sample voltage to output to the loop filter. The loop filter/amplifier develops a correction voltage from the phase difference and uses the voltage to drive the VCXO.

3.5.8.2.8 Pedestal

The oscillator is placed on a fixed voltage (pedestal) before lockup, when forced to pedestal for test, and after holdover has migrated to pedestal.

When pedestal is selected by the analog MUX holdover switching is disabled, and the fixed pedestal voltage is applied to the pedestal circuit. This action places the VCXO under pedestal voltage control. The pedestal voltage is factory adjusted for VCXO center frequency by potentiometer R418.

An LOS in the laser receiver, a loss of activity on all four of the input data bits, or an input SEF condition will cause the holdover circuits to stop sampling the control voltage for the 54 MHz oscillator. A LOS in the laser receiver, a loss of activity on all four of the input data, or an input LOF condition will force an AIS condition in the STS insert circuits and force the loop into holdover.

3.5.8.2.9 Baud VCXO

TCKB – The input clock (TCKB) from the baud VCXO is used to generate the baud and nibble clocks. Frequency dependent. Phase Detector A/B (PHBA/B) complimentary outputs provide relative phase difference between pointers in an elastic buffer.

3.5.8.3 Radio RCV / Optical XMT Signal Flow

The DX-35P OC3/STM-1 I/O Interface RCV circuits (Figure 3-28) receive parallel I, Q data signals (RX I and Q 2:0), and BAUD CLK from the RCVR module. The SMCRA demultiplexes/decodes these inputs to form STS1 data, auxiliary (overhead data), and a reference sync signal. The overhead data contains a 262 kb/s service channel, a 1.544 Mb/s WDS1 per each DS3, and two 16 kb/s command path channels.

3.5.8.3.1 RCVR Module Interface

The RCVR module interface at connector J3A consists of Receive Data (RXD), Receive Subset data (RSD), BAUD Identification (ID), Trellis Code Modulation Sync (TCMS), Receive BAUD clock (RCV BAUD), Bit Clock (CLK), (FRMF) and Viterbi Correcting Errors (VITERBI CORE).

RCVR module interface circuits consist of a retime circuit and FEC circuit. RX I (2:0) and RX Q (2:0) signals from the RCVR are clocked into the retime circuit by the BAUD CLK. The retime circuit retimes the I and Q signals to the baud clock and the I and Q signals are applied to the SMCRA FEC circuit. The FEC circuit removes the FEC encoding that was placed on the data stream by the MDR-8000 XMTR at the other end of the hop.

3.5.8.3.2 SMCRA Functions

The SMCRA performs Reed-Solomon decoding, descrambling, radio frame detection and alignment, extracting service channel and DS1 overhead channels, elastic buffering, STS1 frame detection, PVMR, data rate adjustment to interface with FEC array, phase/frequency detection, and alignment signal generation.

3.5.8.3.3 RCV VCXO

The input clock (MHZ-51R) from the RCV VCXO is used to generate the 39 MHz clock that is used for all SMCRA RCV functions and to generate the RCV baud and nibble clocks used by the 4X39 translator RCV circuits. A Phase Locked Loop (PLL) controls the frequency of the Voltage Controlled Crystal Oscillator (VCXO) generated clock. The PLL consists of the Voltage Controlled Crystal Oscillator (VCXO), a phase detector circuit in the SMCRA, and a loop filter/amplifier.

RCV PDA/B - Receive Phase Detector A/B. Complimentary outputs provide relative phase difference between pointers in local or adjacent SMCRA elastic buffers. The loop filter/amplifier develops a correction voltage from the phase difference and uses the voltage to drive the RCV VCXO.

3.5.8.3.4 Errorless Switching

Errorless switching is performed using elastic buffers in the A and B I/O interface modules and a common read clock between the modules, in a protected system.

3.5.8.3.5 DADE

DADE is an automatic function of the SMRCA and is performed using the elastic buffers in the A and B I/O interface modules.

3.5.8.3.6 B1 Byte

Parity bits are continuously monitored and a parity error pulse is generated when a mismatch is detected.

3.5.8.3.7 AIS (K1/K2 Byte)

An AIS detector is enabled when STS1 is out of frame.

3.5.8.4 Wayside DS1 Interface

The DX-35P uses a DS1 interface ASIC for DS1 signal processing. The demultiplex section of the DS1 interface ASIC receives four channels of DS1/E1 data and clocks (WS DS1-1 through 3 T/R and RPTR T/R). The four channels of data are clocked into an elastic buffer. The data is then converted to a quasi-RZ format and encoded, according to the modulation mode. The encoded data is sampled in an AIS detector for loss of signal, demultiplexed onto two (T&R) channels, and converted to RZ data. TEO (trailing edge overshoot) pulses are added to the RZ data so that the pulses conform to cross-connect requirements without the need of an external equalizer. Tip and ring outputs for each channel (DS1 Chan 1-4 Out T/R) are applied to DS1 LBO circuits on the MDR-8000 OC3/STM-1 AUX interface via connector J3E.

3.5.8.5 Service Channel Interface

Figure 3-33 and Figure 3-34 show XMT and RCV signal flow. Refer to service channel multiplex description previously described in this section for XMT details. The DX-35P sends service channel 1 data to the AE-37Y-1 controller module via connector J3B. Service channel 2 data from the controller is wired (J3C) but not used for the OC3/STM-1 radio applications.

3.5.8.5.1 Terminal

See Figure 3-33. At a terminal, the service channel interface at the SMRCA in the I/O interface consists of the WEST SC RCV DT and WEST SC CLKS (WEST SC 256K CLK, WEST SC 64K CLK, WEST SC 16K SYNC, WEST 8K SYNC, and WEST SC 2K SYNC) outputs. The WEST SC XMT DT output is a single 256 kb/s multiplied signal that contains four 64kb/s channels.

In the SMRCA, the service channel data (WEST SC RCV DT) is removed from the radio frame overhead and is sent to the service channel muldem in the controller module. The WEST SC RCV DT is clocked into the controller by the SMRCA using the WEST SC CLOCKS provided by the SMRCA.

3.5.8.5.2 Repeater

See Figure 3-34. The service channel interface at the SMRCA in the rack 1 I/O interface consists of the WEST SC XMT DT and WEST SC XMT OH inputs and WEST SC CLKS (WEST SC 256K CLK and WEST SC 2K SYNC) outputs. The WEST SC XMT DATA input consists of four 64kb/s channels multiplexed into a single 256 kb/s signal.

When WEST SC XMT OH is low (No off hook from rack 1 controller) data received over the RF path (WEST SC RCV DT) is passed through the MUX and put on the repeater cable to rack 2. When WEST SC XMT OH is high (off hook), WEST SC RCV DT is clocked into the rack 1 controller by the WEST SC CLKS. The rack 1 controller multiplexes the WEST SC RCV DT with local insert-data and the combined signal is passed through the MUX and put on the repeater cable to rack 2.

3.5.8.6 Control and Monitor Functions

3.5.8.6.1 Controller Interface

The controller interface is used to transfer alarm and status information to the AE-37( ) Controller. It is also used to receive control information from the AE-37( ) Controller.

Alarms generated in the SMCRA are latched in the controller interface until they are acknowledged by the system controller. Optical receive/radio transmit alarms generated by the SMCRA include: Severely Errored Frame (SEF), Loss of Frame (LOF), B1 Bit Error (B1 ERROR), and Loss of Signal (LOS).

3.5.8.6.2 SEF

SEF is declared when a minimum of four consecutive errored framing patterns has been received. SEF is cleared when a minimum of two consecutive error-free framing patterns have been received.

3.5.8.6.3 LOF

LOF is declared if the SEF state persists for a count comparable to 23 frames. LOF is cleared when the signal remains in-frame for a minimum of one millisecond.

3.5.8.6.4 B1 ERROR

The B1 parity checker calculates BIP-8 parity over all the bytes of the STSn frame and checks this calculated parity against the RCV parity (B1 byte) in the next frame. B1 ERROR is declared if a mis-compare or error is detected.

3.5.8.6.5 LOS

LOS is declared when an all zeros pattern is received on all four bits of nibble data (a minimum of 100 microseconds).

Data is sent and received during a two-byte transfer. The first byte is a poll byte that selects the device ID and register address. It also controls whether a read or write operation is taking place. The second byte contains data from the selected register.

3.5.8.6.6 Provisioning Inputs

The I/O interface receives the following provisioning inputs (PROV 1-8) from capacity keys on the XMTR and RCVR modules:

- modulation scheme
- local oscillator control source (pedestal voltage or PLL)
- STS1 operation and number of STS1 lines enabled
- data scrambled or passed data through unmodified
- stuff rate source for stuffing DS1/E1 signals in radio frame (average stuff rate or stuff request signals from DS1 interface ASIC)
- enables or disabled data scrambler stuck pattern (all 1's, all 0's, or alternating 1's and 0's).

3.5.8.6.7 I^2C Bus

The I^2C (Inter-Integrated Circuit) bus communicates module part number, serial number, and revision history information to the AE-37( ) Controller.

3.5.8.6.8 ON-Line / Off-Line Enable / Disable

In a hot-standby system, a XMT AUX ENABLE, RCV ENABLE, and WDS1 ENABLE signals from the AE-37Y Controller module turn on the respective XMT, RCV and wayside DS1 circuits on the on-line OC3/STM-1 I/O interface module. This results in XMT AUX ONLINE, RCV ONLINE, and WDS1 ONLINE signals being generated in the on-line I/O interface that are applied to the OC3/STM-1 AUX interface. The XMT AUX DISABLE, RCV DISABLE, and WDS1 DISABLE output signals from the OC3/STM-1 AUX interface turn off the respective circuits in the off-line OC3/STM-1 I/O interface module.

3.5.8.6.9 Loopback Controls

Refer to loopback information on the Control screen for details. To access the Control screen:

1. Click here to enter Controls guide. Main screen will open.
2. On the Main screen, on dropdown for type of radio, click on OC3. OC3 Status Alarm screen will open.
3. On OC3 Status Alarm screen, on tool bar, click on User Control. User control screen will open.
4. On User Control screen, click on loopback function.

3.5.8.6.10 Alarms

- ALM – red LED, indicates I/O interface module failure.
- OC3/STM-1 ALM – red LED, indicates OC3/STM-1 signal failure.
- WYSD FAIL – red LED, indicates loss of signal, bipolar violation detected, or failure on one of the active WDS1 lines.

3.5.8.6.11 Status

- RF ON – green LED, indicates I/O on-line.
- OC3/STM-1 ON – green LED, indicates OC3/STM-1 on-line.
- WDS1 ON – green LED, indicates DS1 interface circuit output drivers are enabled.

3.5.9 DX-35R-1/2 Ethernet I/O Interface

There are two versions of the DX-35R Ethernet I/O Interface module. The earlier version, (DX35R-1 (PN 3EM16610AA), supports electrical ethernet applications and is equipped with one front-panel mounted RJ-45 connector. The later version, DX35R-2 (PN 3EM16610AB) replaces the DX-35R-1 and supports both electrical and optical Ethernet applications. The DX-35R-2 module is equipped with a front-panel mounted RJ-45 connector for electrical Ethernet connection and an SFP (Small Form factor Pluggable) module receptacle for optical Ethernet connection. The SFP plugs into the SFP receptacle and XMT and RCV fiber optic cables connect to the SFP. One interface (electrical or optical) is active, the other interface is backup and becomes active if the already active interface fails.

The DX-35R Ethernet I/O Interface multiplexes/demultiplexes up to three data channel pairs, DS1, and service channel data in the MDR-8000 Ethernet radio. The Ethernet data input/output is via Ethernet cable connected to an RJ45 connector. The input/output between the I/O interface and the MDR-8000 radio is via the radio backplane output between the I/O interface and the MDR-8000 radio is via the radio backplane through J3A, J3B, and J3C. There is also connection to the AUX card via J3D and J3E.

See Figure 3-35 for to/from signal information and application information. The Ethernet I/O Interface consists of several functional blocks each of which is described below.

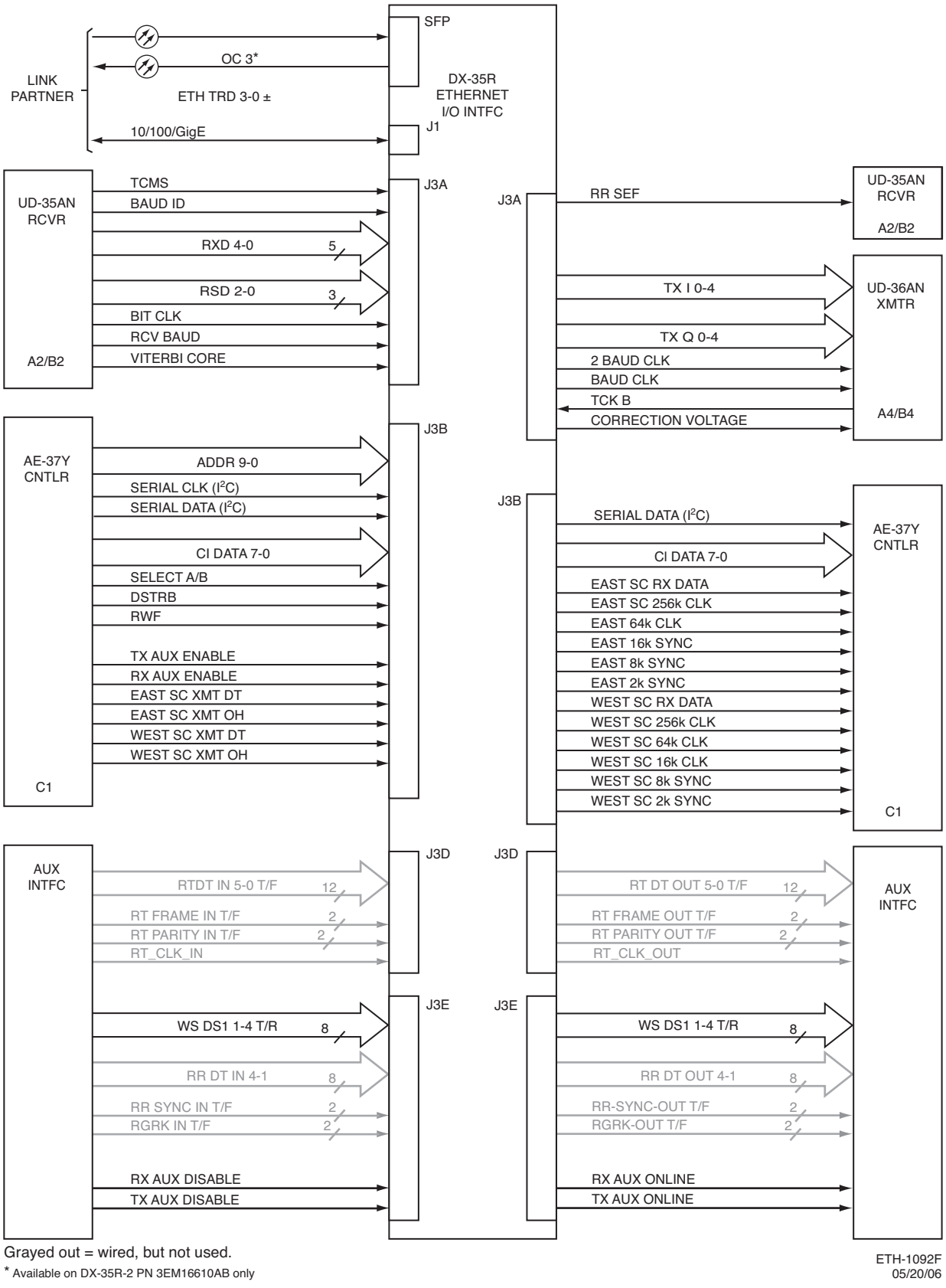


Figure 3-35 DX-35R Ethernet I/O Interface Interconnect Diagram

3.5.9.1 Modes of Operation

Provisionable modes of operation include: A Only, A and B Switched, A and B Separate, and A and B Summed. Refer to signal flow drawings in Initial Turnup section.

Note

For all modes of operation, only the Eth Out associated with the active Eth In is allowed to put out data.

3.5.9.1.1 A Only

The A Only mode allows external equipment, that has a single input and a single output port, to connect to an MDR-8000E that has one or two I/O interface modules. Only the A Eth In and A Eth Out ports are active.

In the XMT direction, the A Eth In data is connected to the A I/O interface modules. Cross-over data is sent to the B I/O interface module (if equipped).

In the RCV direction, the A Eth Out data is connected to the A I/O interface modules. Cross-over data is sent from the B I/O interface module (if equipped).

3.5.9.1.2 A & B Switched

A failure on A or a manual switch, switches Ethernet data on A Ethernet In and A Ethernet Out ports to the B Ethernet I/O interface. Data is not automatically returned to A when the alarm is cleared. The data remains on B until an alarm or manual switch on B switches the data to A.

3.5.9.1.3 A & B Separate

In this mode, A and B are two completely separate unprotected data channels.

In the XMT direction, data from the A I/O interface Eth In port is applied to the A XMTR module and data from the B I/O interface Eth In port is applied to the B XMTR module. If a failure occurs, data on that channel is lost.

In the RCV direction, the A Eth Out port uses data only from the farend A XMTR and the B Eth Out port uses data only from the farend B XMTR. If a failure occurs, data on that channel is lost.

3.5.9.1.4 A & B Summed

This mode can be used to provide Ethernet link protection for hops with one RF link.

In the XMT direction, both the A and B Ethernet I/O interface modules receive data on the Eth In port. When there is only one RF link, the data from both the A and B I/O interface Eth In ports are combined into a single data stream and the composite signal is applied to the active XMTR module. Frames are tagged to indicate the data source. When there are two RF links, this mode functions the same as A and B Separate with A and B operating as separate, independent channels. In this scenario, data from both the A I/O interface Eth In port is applied to the A XMTR module and data from both the B I/O interface Eth In port is applied to the B XMTR module.

In the RCV direction, the A Eth Out port uses data only from the farend A XMTR and the B Eth Out port uses data only from the farend B XMTR. If a failure occurs, data on that channel is lost.

3.5.9.2 Ethernet Switching

See Figure 3-36. In the A and B Switched mode, when an I/O switch is initiated by an alarm or a manual switch (refer to Table 3-4), the A ETH R/RT (Ethernet In) and A RR/ETH T (Ethernet Out) signals are switched simultaneously to B. B will remain in service until it alarms or a manual switch to A is initiated.

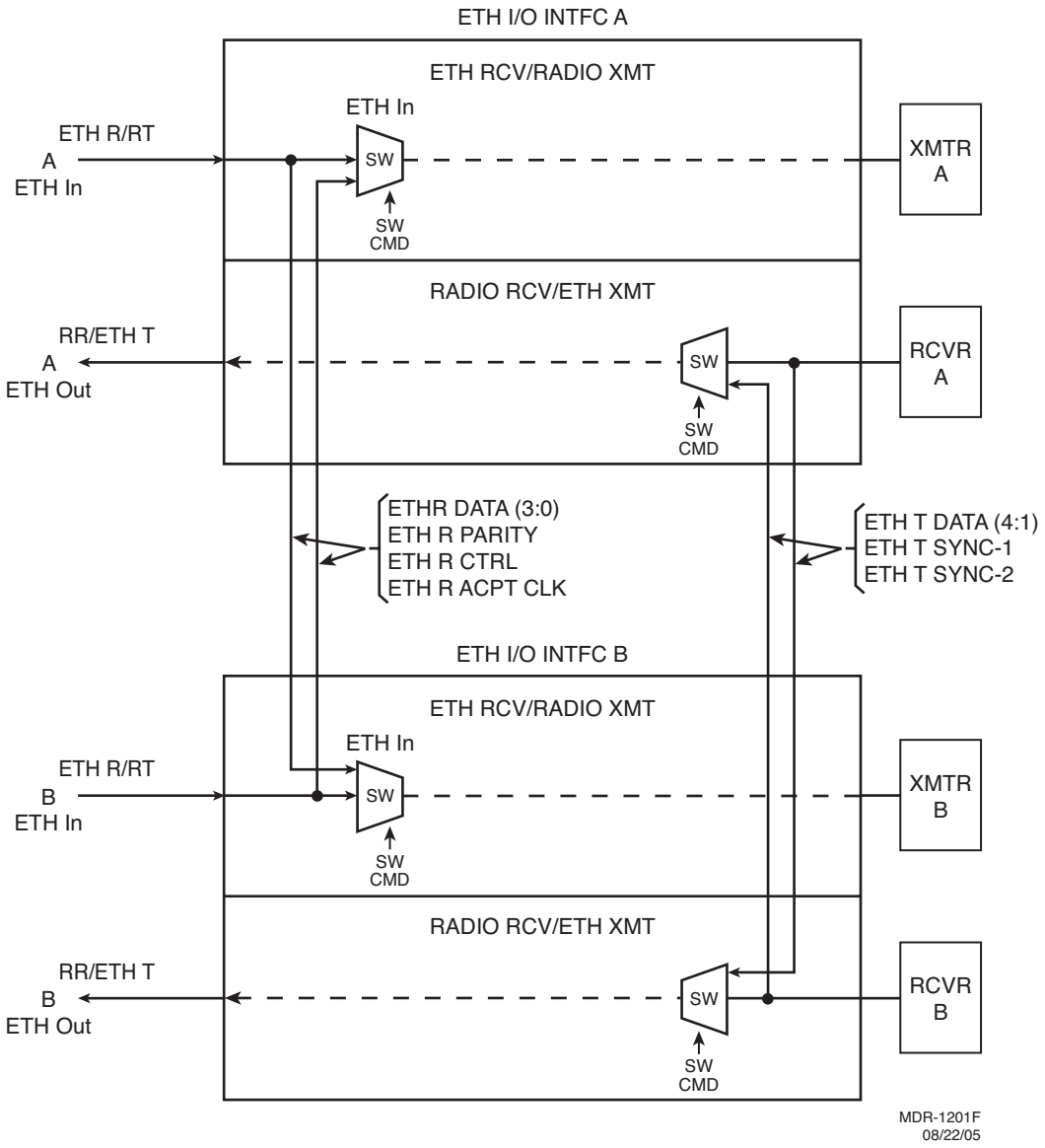


Figure 3-36 Ethernet Crossover Function Simplified Functional Block Diagram

Table 3-4 Ethernet In/Ethernet Out Switching Priorities

Priority	Function
5 Highest	Card Not Valid (the card is being stored in the B side, but is not provisioned and not being used)
4	Card Not Equipped
3	Override (using either the controls on the controller module front panel or the USI Control screen)
2	No Link or No Signal on Ethernet Data
1 Lowest	Manual Switch (using either the controls on the controller module front panel or the USI Control screen)

3.5.9.3 DS1 Switching

See Figure 3-37. DS1 and AUX channel switching is independent of the Ethernet data switching. In hot-standby, space-diversity, and frequency-diversity radios, in the radio XMT direction, DS1 data is applied to both the A and B I/O Interface modules, multiplexed with Ethernet data and AUX channel data, and applied to the A and B XMTRs.

In the radio RCV direction, DS1 data out of the A RCVR is applied to both the A and B I/O Interface modules. When a DS1 switch is initiated by an alarm or a manual switch (refer to Table 3-5), the A DS1 TX outputs from the A RCVR are switched to the B I/O Interface module.

DS1 switching is not revertive. DS1 RCV circuits on the B I/O Interface will remain in service until either B alarms or a manual switch to A is initiated.

Table 3-5 DS1 Switching Priorities

Priority	Function
4 Highest	Card not valid (the I/O Interface card is being stored on the B side, but is not provisioned and not being used).
3	I/O Card not present
2	Override
1 Lowest	Manual switch

3.5.9.4 10/100BASE-T Operation

The 10BASE-T and 100BASE-T radios employ half-duplex and full duplex baseband transmission over two pairs of category 5/5E (CAT5/5E) balanced cabling. The aggregate data rate of 10/100 Mb/s is achieved by transmission at a data rate of 10/100 Mb/s over each wire pair. The data is transmitted over the RF path in burst of up to 10 Mb/s and 100 Mb/s, respectively.

3.5.9.5 1000BASE-T Operation

The 1000BASE-T (sometimes referred to in the industry as GigE) radio employs full duplex baseband transmission over four pairs of category 5/5E balanced cabling. The aggregate data rate of 1000 Mb/s is achieved by transmission at a data rate of 250 Mb/s over each wire pair. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pair at the same time. Data from the link partner is received in bursts of up to 1000 Mb/s and is transmitted over the RF path in bursts of up to 150 Mb/s.

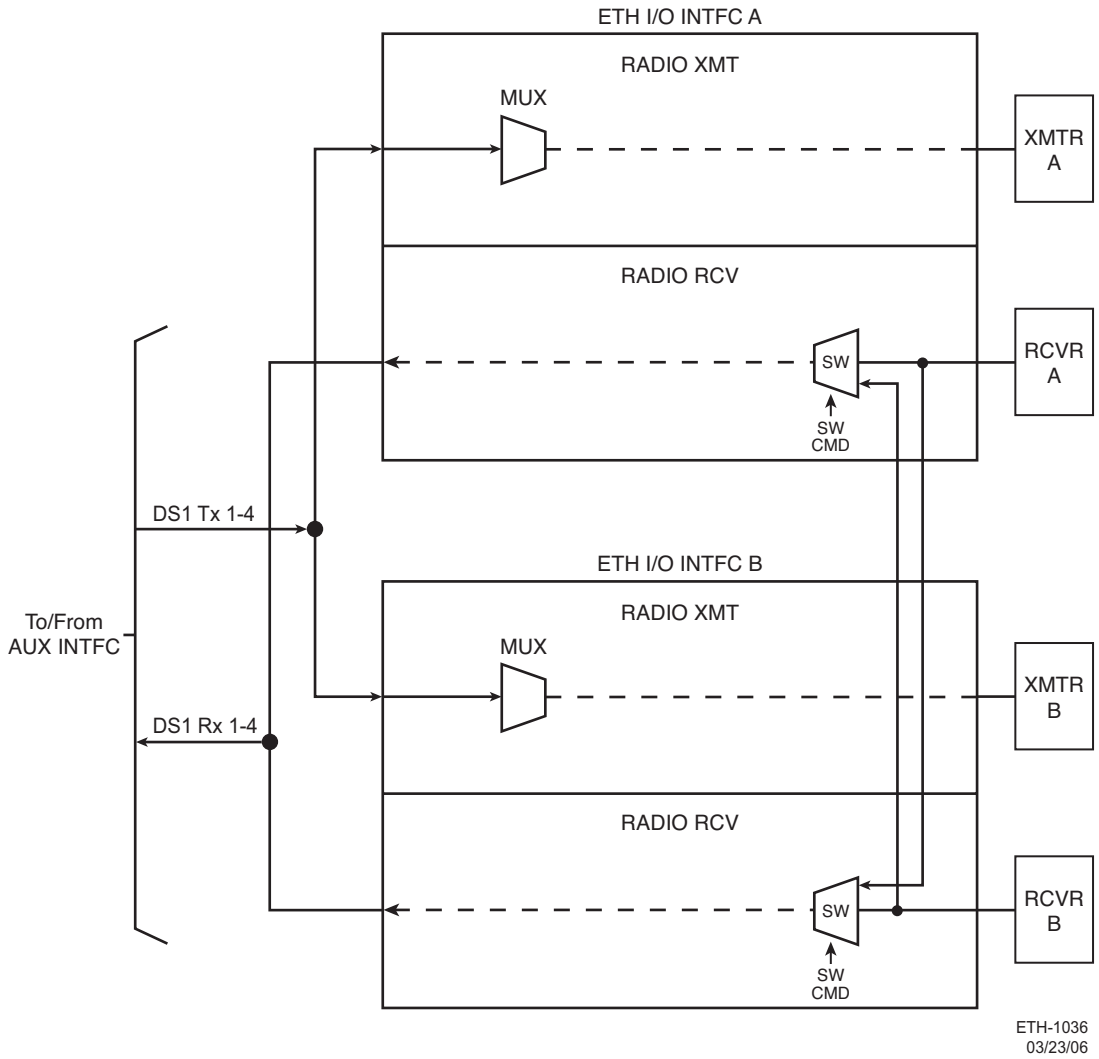


Figure 3-37 DS1 Switching

3.5.9.6 Ethernet Data Flow

See Figure 3-38. The DX-35R I/O Interface consists of the RJ45 connector, the Input/Output transformer, the Ethernet PHY, the ETHRA FPGA, and the T1/E1 Line Interface. A description of each follows.

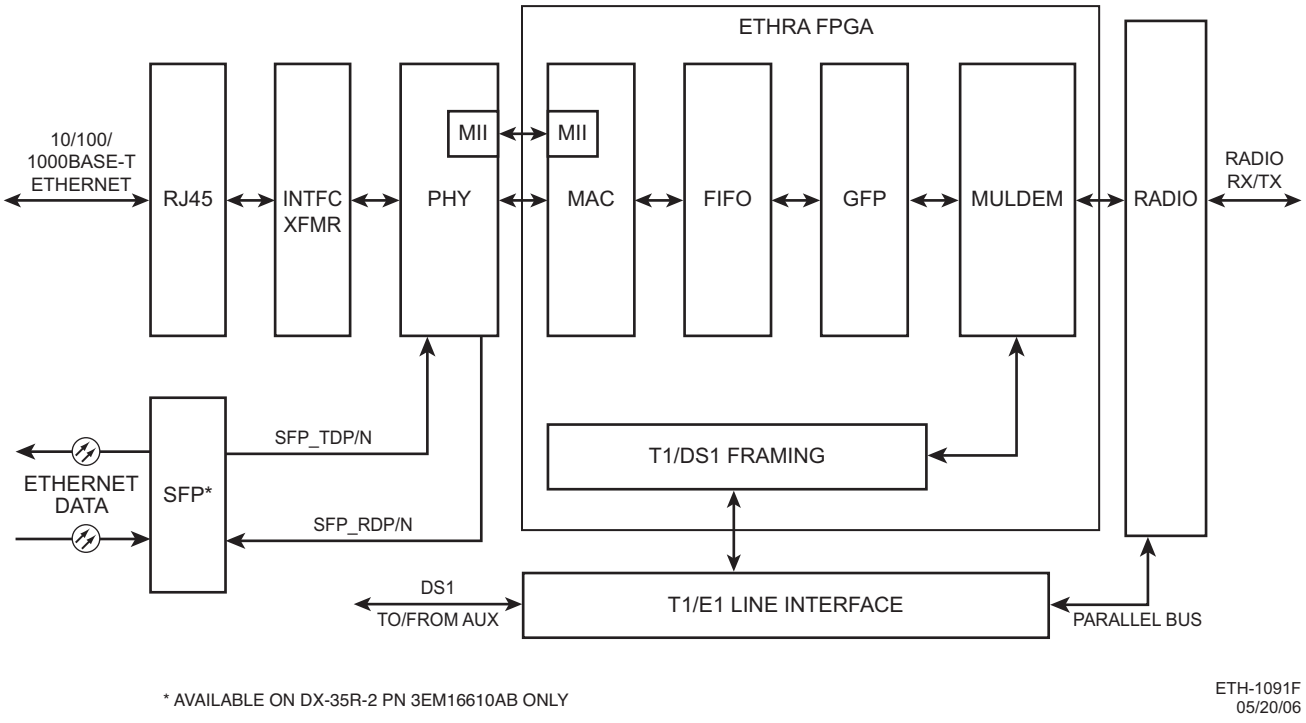


Figure 3-38 Ethernet Data Flow Block Diagram

3.5.9.6.1 RJ45 Connector

The RJ45 connector is the Ethernet cable connection to/from the interface transformer on the DX-35R Ethernet I/O Interface board.

3.5.9.6.2 Interface Transformer

The transformer is used for signal coupling between the RJ45 connector and the Ethernet PHY block. Transformer coupling provides spike filtering and termination.

3.5.9.6.3 SFP

The SFP is used for signal coupling between the fiber optic cable and the Ethernet PHY block.

3.5.9.6.4 Ethernet PHY

The PHY connects Ethernet media to the ETHRA FPGA (through Media Access Control) and defines the electrical signaling, line states, clocking guidelines, data encoding, and circuitry needed for data transmission and reception.

The PHY also performs auto-negotiation (detects the rate of incoming and/or outgoing data; 10BASE-T, 100BASE-T, 1000BASE-T) and selects the highest common input rate.

3.5.9.6.5 ETHRA FPGA (Ethernet Field Programmable Gate Array)

The main internal components of the FPGA are: MAC, FIFO, GFP, Muldem and T1/DS1 Framing block.

3.5.9.6.5.1 MAC (Media Access Control)

The MAC interfaces between the Physical Layer (PHY) and the FIFO and primarily performs Ethernet Framing to wit:

- When receiving Ethernet data from the PHY (for Radio XMT), this component recognizes where frames begin and end in the bit-streams received.
- When transmitting data to the PHY (during Radio RX), the MAC delimits the frame by inserting some extra bits into or among the frames being sent to enable the receiver(s) to recognize the beginning and ending of the frames.
- The MAC employs cyclical redundancy checks (CRC) by the use of checksums to ensure the integrity of the bits in the frame to verify the frame is intact.
- The MAC implements CSMA/CD during half-duplex Ethernet RX mode.

3.5.9.6.5.2 FIFO Buffer (First Frame In - First Frame Out)

The First In First Out buffer (FIFO) connects between the MAC and the GFP processor. Its purpose is to transfer Ethernet data to the GFP for framing encapsulation prior to insertion in the service channel for radio XMT, and to receive decapsulated framed data from the GFP for transfer to the MAC and further transmission over the Ethernet.

In the Ethernet RCV/Radio XMT direction the three modules are: System Receive module (receives data from the MAC), the Fabric receive module (sends data to the GFP), and the

Water Mark module. In the radio RCV/Ethernet XMT direction there are three sub-modules in the data path: the Fabric TX module (receives RF from the GFP), the System TX module (sends data to the MAC), and the Water Mark module (data flow control during data transfer). In both directions data is written to and read from the Generic Synchronous 2-port SRAM buffer.

During half-duplex operation, CSMA/CD mode is operational and collision effects are evaluated during data transfer. Excessive collisions will cause a cessation of transfer and removal of collision corrupted transferred data. During full-duplex operation, CAMA/CD is off and there are no collision effects to interrupt data flow.

In the Ethernet RCV/Radio XMT direction, Ethernet data is clocked into the egress FIFO eight bits at a time from the MAC through the System Receive module, written into FIFO memory in the sequence of arrival, read out of memory into the Fabric Transmit module, and then, four bytes at a time, sent to the GFP. To begin transfer of data, the MAC sends the FIFO a Ready-To-Send signal and awaits the FIFO reply Ready-To-Receive. As the MAC sends its Ethernet data to the FIFO, it runs data validity checks. If the data is invalid because of corruption, or excessive collision effects, FIFO is notified to abort reception. When data transmission resumes, the data is written into memory by the System receive module. The data at the same time is being read out of memory by the fabric receive module. This module hand shakes with the GFP (Ready to Send/Ready to Receive). When GFP acknowledgement is received, the data is sent to the GFP four bytes at a time. In the GFP the data frame is encapsulated for insertion into the radio service channel.

In the Radio RCV/Ethernet XMT direction, RF data is clocked into the ingress FIFO four bites at a time through the Fabric Transmit module, written to FIFO memory in the sequence of arrival, read out of memory into the System Receive module and then transferred eight bits at a time to the MAC. During reception from the GFP to the FIFO the data undergoes validity checking by the Fabric Transmit module. If data is invalid, the Fabric Transmit module notifies the GFP to quit sending the present data and restart a new frame sequence. A Water Mark module in the FIFO is used to control data flow and assure that data threshold levels at all points of transmission and reception are within limits. In the case of under-run, the FIFO holds data in the buffer until more is received from the GFP module. In the Radio RCV/Ethernet XMT direction, a short frame (less than 64 byte frame length) is considered an error frame and is discarded.

3.5.9.6.5.3 GFP (Generic Framing Procedure)

The Generic Framing Processor (GFP) processes received Ethernet signals for transport over the radio network and processes received radio signals for transport over the Ethernet network. The processor preserves original control information and incurs very short transmission delay. The framing process incurs very short transmission delay. The framing process includes encapsulation (for radio transmission) and decapsulation (for Ethernet transmission), header processing, digital encoding/decoding, performance monitoring and more. The processor contains a simplified FIFO interface to connect to the ingress/egress FIFO.

During Ethernet RCV/Radio XMT, the processor receives the Ethernet signals from the FIFO via the FIFO Interface. It aligns character and control code, and maps consecutive characters into block code. Eight block codes are grouped into a superblock with core and payload headers. There is also a CRC-16 error check code added which calculates and inserts core and payload header error control into each transmitting GFP frame. The superblocks are then encapsulated as payload into periodic, fixed length GFP frames and inserted in the radio service channel for RF transmission.

During Radio RCV/Ethernet XMT, the processor receives the radio frames from the service channel, performs frame delineation and validation (core/payload header error control) for each received GPF frame, and decapsulates the data into a set of superblocks. The superblocks are then decoded into 8-bit characters (data and control codes) and sent to the egress FIFO via the FIFO interface.

3.5.9.6.5.4 Muldem

The muldem contains the circuitry to perform framing, to insert Ethernet, Service Channel, and data into the frames for radio transmitting, and in the case of radio receiving, remove data from the overhead and transfer it to the PHY for feed to the Ethernet cable. In the case of DS1, the data is DS1 framed in the T1/DS1 ETHRA circuitry and directed through the T1/E1 Line Interface to the Aux Interface.

3.5.9.6.5.5 T1/DS1 Framing

Frames the DS1 data for transmission to the T1/E1 Line Interface.

3.5.9.6.5.6 T1 Line Interface

The T1 Line Interface interfaces between the ETHRA and the AUX card for WS DS1 signals and also connects to the backplane parallel bus for handling radio controller bi-directional data.

3.5.9.7 Ethernet RCV/Radio XMT Data Flow

See Figure 3-39. The DX-35R Ethernet I/O Interface board data flow follows from board input at the RJ45 connector to the Coupling Transformer to the Physical Layer Device (PHY) and into the ethernet Regenerator Array (ETHRA). From there it leaves the Ethernet I/O Interface board and enters the radio path.

The PHY chip on the I/O board serves as the controlling influence for Ethernet data flow. When enabled for Auto-Negotiation, the PHY establishes a communication link with the far end PHY on the other end of the Ethernet cable (if it, too, has Auto-Negotiate capability) and between them they compare their abilities and connect at the highest common data transfer rate or mode (10BASE-T, 100BASE-T, or 1000BASE-T). Auto-Negotiation makes automatic connection of the highest data rate available without intervention from the user or from management software and ensures data integrity. If Auto-Negotiation is not enabled, the transfer will occur at a pre-configured rate.

The coupling transformer filters and terminates the incoming Ethernet signal and from there the data is picked off by the PHY for application to the ETHRA. Connecting the PHY and the ETHRA is the Medium Independent Interface (MII) circuitry. Since the MII circuits interface between the PHY and the ETHRA, identical circuits are located in the PHY and also in the Media Access Control (MAC) circuitry within the ETHRA. The MII circuits convert the line signals received by the PHY into digital format signals and provide them to the ETHRA via the MAC. the ETHRA multiplexes the Ethernet data with data from the serial service channel interface and wayside interface and converts the final multiplexed data into two X/Y data rail pairs. The X/Y data pairs are then applied to a serial scrambler. The scrambled X/Y data is applied to a Forward Error Correction (FEC) encoder circuit which uses Trellis Coded Modulation and Reed-Solomon coding. The encoded X/Y data steams are converted to I and Q data steams and clocked out of the ETHRA by the T CLK B input from the XMTR module BAUD VCXO. The TX1 1-4 and TX Q 1-4 data are applied to the transmitter module via connector J3A.

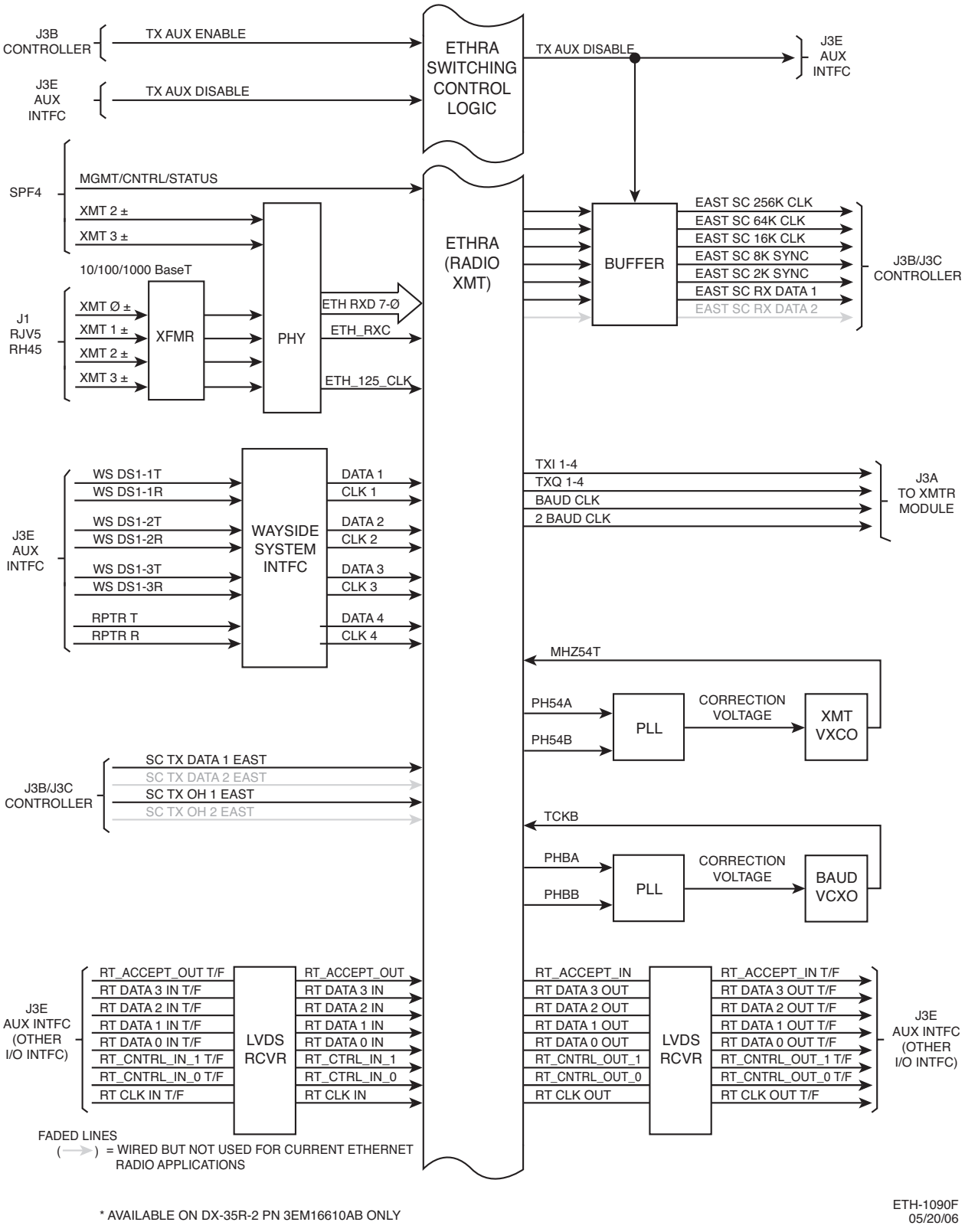


Figure 3-39 DX-35R Ethernet I/O Interface Ethernet RCV/Radio XMT Functional Block Diagram

3.5.9.7.1 XMTR Module Interface

The XMTR module interface at connector J3A receives Transmit Data (TX1 1-4 and TXQ 1-4), BAUD CLK, and 2 BAUD CLK (twice the frequency of BAUD CLK) from the ETHRA.

3.5.9.7.2 DS1 Interface

The DS1 interface circuit provides clock recovery, clock smoothing, elastic buffering and line encoding for each DS1 (WS DS1-1-3 T/R) channel.

The DS1 tip and ring signals (WS DS1-1T and WS DS1-1T and WS DS1-1R) are applied to the DS1 interface circuits via connector J3E. The balanced tip and ring signals consist of pulsed square waves at 1.544 Mb/s. The DS1 interface circuit bridges the RZ data onto one channel, converts the balanced tip and ring signals to NRZ data, B3ZS encodes the data, and using the recovered clock, writes the data into an elastic buffer. In the elastic buffer, the recovered clock is compared to the low-speed clock created by the ETHRA and if a mismatch is detected, stuffing bits are inserted. The DATA 1-4 outputs of the DS1 interface circuit are clocked into the ETHRA by the respective four output clocks (CLK 1-4).

3.5.9.7.3 Service Channel Interface

Refer to service channel demultiplex description later in this section for RCV details. The DX-35R ETHRA receives inserted service channel 1 data from the AE-37Y-1 controller module via connector J3B. Service channel 2 data from the controller is wired (J3C) but not used for the Ethernet radio applications.

Overhead MUX circuitry in the ETHRA receives local insert-service channel data (SC TX DATA 1 EAST, SC TX DATA 2 EAST, SC TX OH 1 E, and SC TX OH 2 E) from the service channel muldem in the controller module. The EAST SC TX DATA is clocked into the ETHRA by the controller using the EAST SC CLOCKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST C 8K SYNC, and EAST SC 2K SYNC) provided by the ETHRA. In the ETHRA, the service channel insert data (EAST SC TX DATA) is inserted into the radio frame overhead.

3.5.9.8 Radio RCV/Ethernet XMT Signal Flow

See Figure 3-40. The DX-35R ETHERNET I/O Interface RCV circuits receive parallel RX and RS data signals; an BAUD CLK from the RCVR module. The ETHRA demultiplexes/decodes these inputs to form Ethernet data, auxiliary (overhead data), and a reference sync signal. The overhead data contains a 262 kb/s service channel, a 1.544 Mb/s WDS1 per each DS1, and two 16 kb/s command path channels.

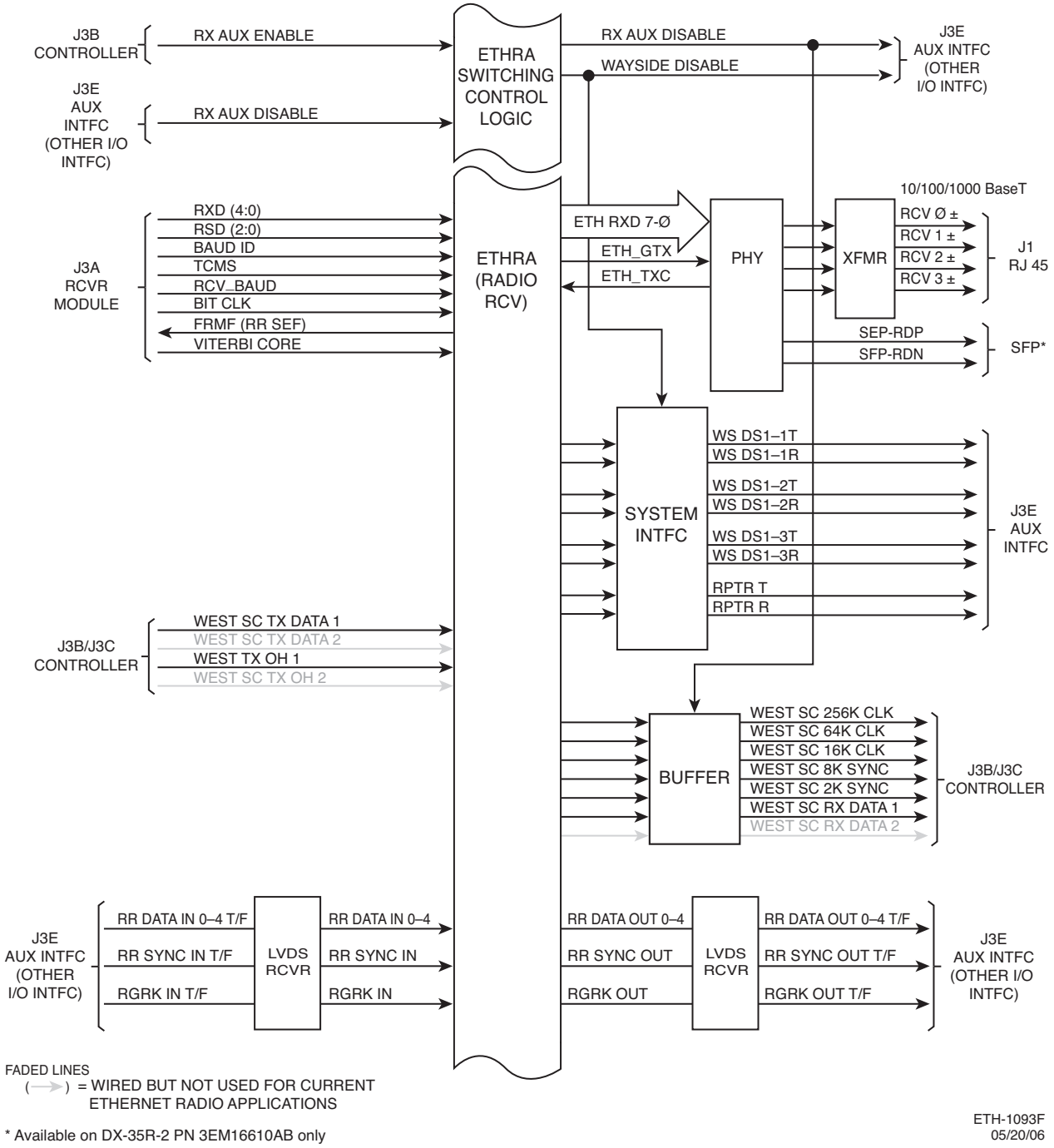


Figure 3-40 DX-35R Ethernet I/O Interface Radio RCV/Ethernet XMT Functional Block Diagram

3.5.9.8.1 RCVR Module Interface

The RCVR module interface at connector J3A consists of Receive Data (RXD), Receive Subset data (RSD), BAUD Identification (ID), Trellis Code Modulation Sync (TCMS), Receive BAUD clock (RCV BAUD), Bit Clock (CLK), Frame False (FRMF) and Viterbi Correcting Errors (VITERBI CORE).

RCVR module interface circuits consist of a retime circuit and Forward Error Correcting (FEC) circuit. RXD and RSD signals from the RCVR are clocked into the retime circuit by the BAUD CLK. The retime circuit retimes these to the baud clock and the signals are then applied to the ETHRA FEC circuit. The FEC circuit removes the FEC encoding placed on the data stream by the MDR-8000 XMTR at the other end of the hop.

3.5.9.8.1.1 ETHRA Functions

The ETHRA performs Reed-Solomon decoding, de scrambling, radio frame detection and alignment, extracting service channel and DS1 overhead channels, elastic buffering. STS1 frame detection, PVMR, data rate adjustment to interface with FEC array, phase/frequency detection, and alignment signal generation.

3.5.9.8.1.2 Parity Byte

Parity bits are continuously monitored and a parity error pulse is generated when a mismatch is detected.

3.5.9.8.2 DS1 Interface

The DX-35R uses a DS1 interface ASIC for DS1 signal processing. The demultiplex section of the DS1 interface ASIC receives four channels of DS1/E1 data and clocks (WS DS1-1 through 3 T/R and RPTR T/R). The four channels of data are clocked into an elastic buffer. The data is then converted to a quasi-RZ format and encoded, according to the modulation mode. The encoded data is sampled in an AIS detector for loss of signal, demultiplexed onto two (T&R) channels, and converted to RZ data. TEO (trailing edge overshoot) pulses are added to the RZ data so that the pulses conform to cross-connect requirements without the need for an external equalizer. Tip and ring outputs for each channel (DS1 Chan 1-4 Out T/R) are applied to DS1 LBO circuits on the MDR-8000 ETHERNET AUX interface via connector J3E.

3.5.9.8.3 Service Channel Interface

Refer to service channel multiplex description previously described in this section for XMT details. The DX-35R sends service channel 1 data to the AE37Y-1 controller module via connector J3B. Service channel 2 data from the controller is wired (J3C) but not used for the Ethernet radio applications.

See Figure 3-41. The service channel interface at the ETHRA in the Ethernet I/O interface consists of the WEST SC RX DATA, WEST SC CLKS (WEST SC 256K CLK, WEST SC 64K CLK, WEST SC 16K), and WEST SC SYNC (WEST SC 8K SYNC, WEST SC 2K SYNC) outputs. In the ETHRA, the service channel data (WEST SC RCV DT) is removed from the radio frame overhead and is sent to the service channel muldem in the controller module. The WEST SC RX DATA is clocked into the controller by the ETHRA using the WEST SC CLOCKS provided by the ETHRA.

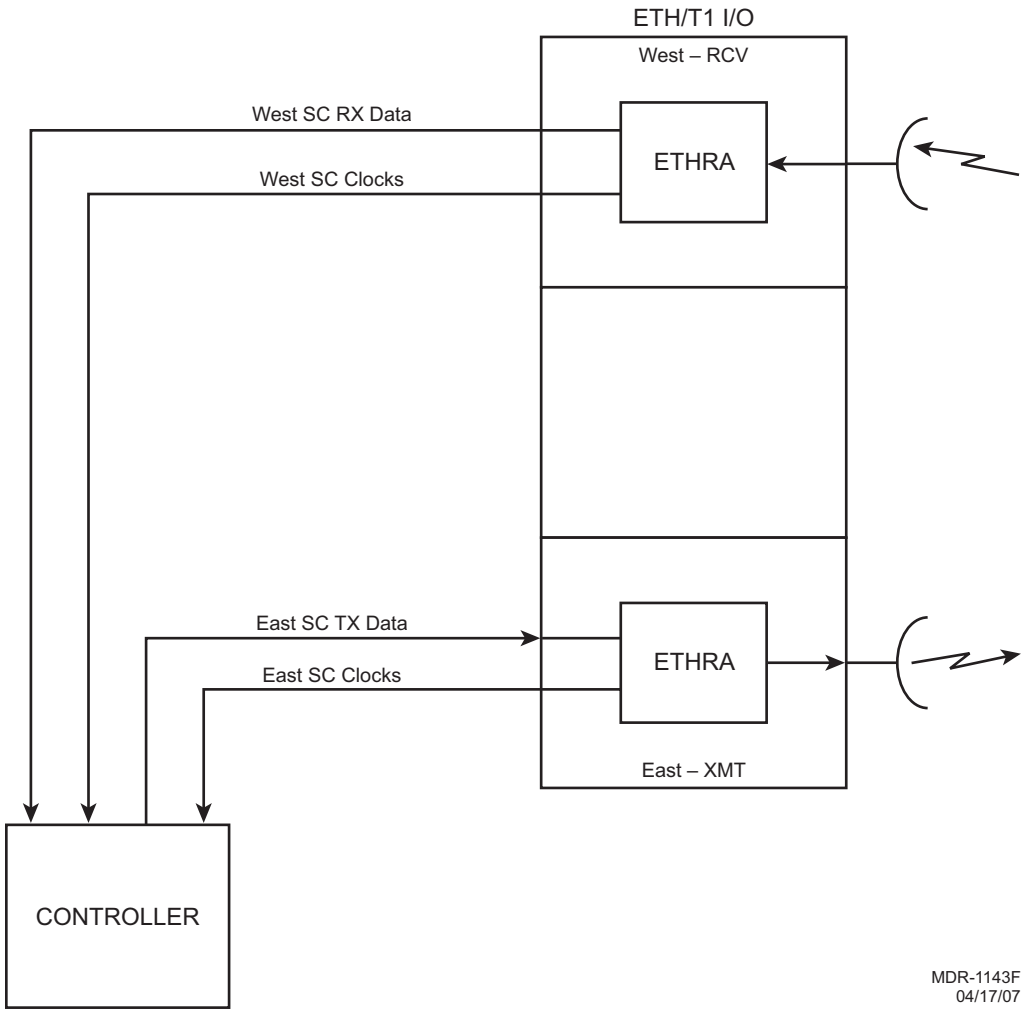


Figure 3-41 ETHRA Service Channel Interface Functional Block Diagram

3.5.9.9 Control and Monitor Functions

3.5.9.9.1 Controller Interface

See Figure 3-42. The controller interface is used to transfer alarm and status information to the AE-37( ) Controller. It is also used to receive control information from the AE-37( ) Controller.

Alarms generated in the ETHRA are latched in the controller interface until they are acknowledged by the system controller. Ethernet receive/radio transmit alarms generated by the ETHRA include: Severely Errored Frame (SEF), Loss of Frame (LOF), Parity Error, and Loss of Signal (LOS).

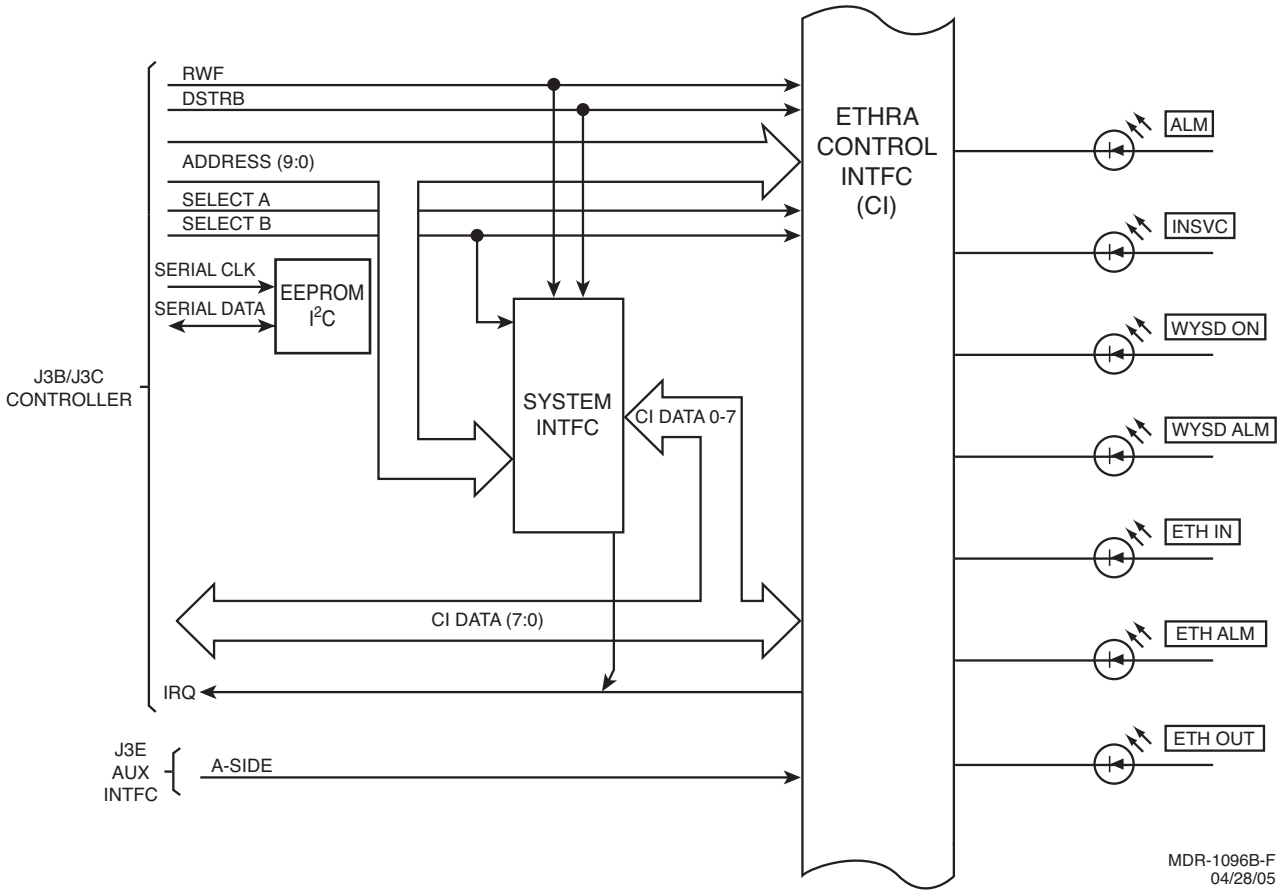


Figure 3-42 DX-35R Ethernet I/O Interface Controller Interface Functional Block Diagram

3.5.9.9.2 SEF

SEF is declared when a minimum of four consecutive errored framing patterns has been received. SEF is cleared when a minimum of two consecutive error-free framing patterns have been received.

3.5.9.9.3 LOF

LOF is declared if the SEF state persists for a count comparable to 23 frames. LOF is cleared when the signal remains in-frame for a minimum of one millisecond.

3.5.9.9.4 Parity Error

The parity checker calculates CRC-8 parity over all the bytes of the STSn frame and checks this calculated parity against the RCV parity (B1 byte) in the next frame. An error is declared if a mismatch or error is detected.

3.5.9.9.5 LOS

LOS is declared when an all zeros pattern is received on all four bits of nibble data (a minimum of 100 microseconds).

Data is sent and received during a two-byte transfer. The first byte is a poll byte that selects the device ID and register address. It also controls whether a read or write operation is taking place. The second byte contains data from the selected register.

3.5.9.9.6 Provisioning Inputs

The I/O interface receives the following provisioning inputs (PROV 1-8) from capacity keys on the XMTR and RCVR modules:

- modulation scheme
- local oscillator control source (pedestal voltage or PLL)
- STS1 operation and number of STS1 lines enabled
- data scrambled or passed data through unmodified
- stuff rate source for stuffing DS1/E1 signals in radio frame (average stuff rate or stuff request signals from DS1 interface ASIC)
- enables or disables data scrambler stuck pattern (all 1's, all 0's, or alternating 1's and 0's).

3.5.9.9.7 I^2C Bus

The I^2C (Inter-Integrated Circuit) bus is for inventory control and communicates module part number, serial number, and revision history information to the AE-37( )Controller.

3.5.9.9.8 Loopback Controls

Refer to loopback information on the Control screen for details. To access the Control screen:

1. Click here to enter Controls guide. Main screen will open.
2. On the Main screen, on dropdown for type of radio, click on ETH. ETH Status Alarm screen will open.
3. On ETH Status Alarm screen, on tool bar, click on User Control. User control screen will open.
4. On User Control screen, click on loopback function.

3.5.9.9.9 Alarms

- ALM – red LED, indicates I/O interface module failure
- ETH ALM – yellow LED, indicates ETHERNET receive circuit failure.

3.5.9.9.10 Status

- INSVC – green LED, indicates XMT and/or RCV circuits are passing data
- ETH IN – green LED, indicates data on input to ETHERNET RCV/RADIO XMT circuits
- ETH OUT – green LED, indicates data on output from RADIO RX/ETHERNET XMT circuits.

3.5.10 DX-35S-1 ETH/T1 I/O

The DX-35S-1 (PN 3EM16167AA) supports both electrical and optical Ethernet applications and provides interface for up to 32 DS1. The DX-35S-1 module is equipped with a front-panel mounted RJ-45 connector for electrical Ethernet connection and an SFP (Small Form factor Pluggable) module receptacle for optical Ethernet connection. The SFP plugs into the SFP receptacle and XMT and RCV fiber optic cables connect to the SFP. One interface (electrical or optical) is active, the other interface is backup and becomes active if the already active interface fails.

The ETH/T1 I/O multiplexes/demultiplexes up to 32 DS1, and service channel data in the MDR-8000 Ethernet radio. The Ethernet data input/output is via Ethernet cable connected to an RJ45 connector or optical cable connected to the ETH/T1 I/O via an SFP. The input/output between the I/O interface and the MDR-8000 radio is via the radio backplane through J3A, J3B, and J3C. There is also connection to the ETH/T1 line interface card via J3D and J3E.

See Figure 3-43 for to/from signal information and application information. The ETH/T1 I/O consists of several functional blocks each of which is described below.

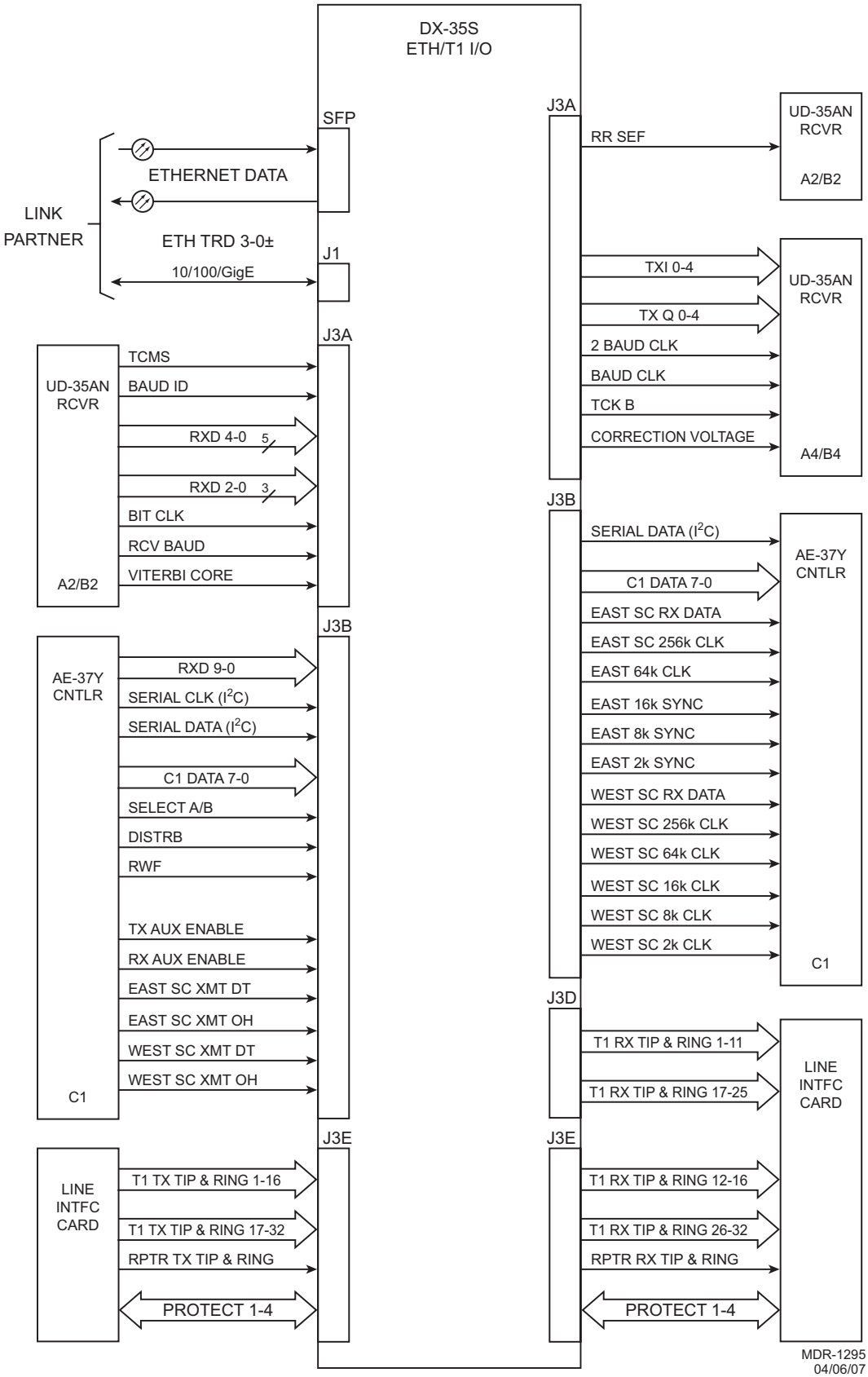


Figure 3-43 DX-35S ETH/T1 I/O Interconnect Diagram

3.5.10.1 Modes of Operation

Provisionable modes of operation include: A Only, A and B Switched, A and B Separate, and A and B Summed. Refer to signal flow drawings in the Initial Turnup Section.

Note

For all modes of operation, only the Eth Out associated with the active Eth In is allowed to put out data.

3.5.10.1.1 A Only

The A Only mode allows external equipment, that has a single input and a single output port, to connect to an MDR-8000E that has one or two ETH/T1 I/O modules. Only the A Eth In and A Eth Out ports are active.

In the XMT direction, the A Eth In data is connected to the A ETH/T1 I/O modules. Crossover data is sent to the B ETH/T1 I/O module (if equipped).

In the RCV direction, the A Eth Out data is connected to the A ETH/T1 modules. Crossover data is sent from the B ETH/T1 I/O module (if equipped).

3.5.10.1.2 A & B Switched

A failure on A or a manual switch, switches Ethernet data on A Ethernet In and A Ethernet Out ports to the B ETH/T1 I/O. Data is not automatically returned to A when the alarm is cleared. The data remains on B until an alarm or manual switch on B switches the data to A.

3.5.10.1.3 A & B Separate

In this mode, A and B are two completely separate unprotected data channels.

In the XMT direction, data from the A ETH/T1 I/O Eth In port is applied to the A XMTR module and data from the B ETH/I/O Eth In port is applied to the B XMTR module. If a failure occurs, data on that channel is lost.

In the RCV direction, the A Eth Out port uses data only from the farend A XMTR and the B Eth Out port uses data only from the farend B XMTR. If a failure occurs, data on that channel is lost.

3.5.10.1.4 A & B Summed

This mode can be used to provide Ethernet link protection for hops with one RF link.

In the XMT direction, both the A and B ETH/T1 I/O modules receive data on the Eth In port. When there is only one RF link, the data from both the A and B ETH/T1 I/O Eth In ports are combined into a single data stream and the composite signal is applied to the active XMTR module. Frames are tagged to indicate the data source. When there are two RF links, this mode functions the same as A and B Separate with A and B operating as separate, independent channels. In this scenario, data from the A ETH/T1 I/O Eth In port is applied to the A XMTR module and data from the B ETH/T1 I/O Eth In port is applied to the B XMTR module.

In the RCV direction, the A Eth Out port uses data only from the farend A XMTR and the B Eth Out port uses data only from the farend B XMTR. If a failure occurs, data on that channel is lost.

3.5.10.2 Ethernet Switching

See Figure 3-36. In the A and B Switched mode, when an I/O switch is initiated by an alarm or a manual switch (refer to Table 3-6), the A ETH R/RT (Ethernet In) and A RR/ETH T (Ethernet Out) signals are switched simultaneously to B. B will remain in service until it alarms or a manual switch to A is initiated.

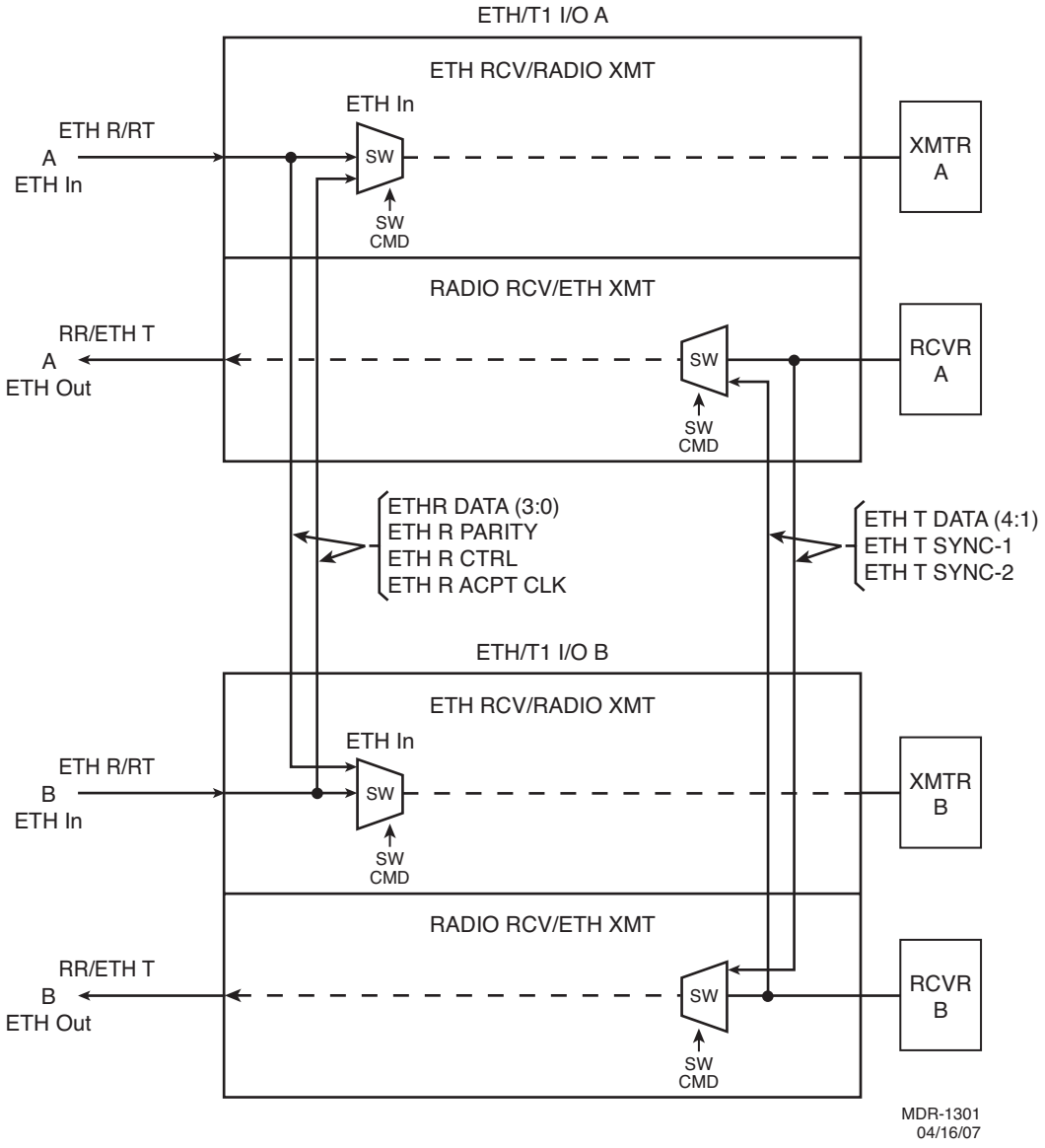


Figure 3-44 ETH/T1 I/O Crossover Function Simplified Functional Block Diagram

Table 3-6 Ethernet In/Ethernet Out Switching Priorities

Priority	Function
5 Highest	Card Not Valid (the card is being stored in the B side, but is not provisioned and not being used)
4	Card Not Equipped
3	Override (using either the controls on the controller module front panel or the USI Control screen)
2	No Link or No Signal on Ethernet Data
1 Lowest	Manual Switch (using either the controls on the controller module front panel or the USI Control screen)

3.5.10.3 DS1 Switching

See Figure 3-45. DS1 and AUX channel switching is independent of the Ethernet data switching. In hot-standby, space-diversity, and frequency-diversity radios, in the radio XMT direction, DS1 data is applied to both the A and B ETH/T1 I/O modules, multiplexed with Ethernet data and AUX channel data, and applied to the A and B XMTRs.

In the radio RCV direction, DS1 data out of the A RCVR is applied to both the A and B ETH/T1 I/O modules. When a DS1 switch is initiated by an alarm or a manual switch (refer to Table 3-7), the A DS1 TX outputs from the A RCVR are switched to the B ETH/T1 I/O module.

DS1 switching is not revertive. DS1 RCV circuits on the B ETH/T1 I/O will remain in service until either B alarms or a manual switch to A is initiated.

Table 3-7 DS1 Switching Priorities

Priority	Function
4 Highest	Card not valid (the ETH/T1 I/O card is being stored on the B side, but is not provisioned and not being used).
3	I/O Card not present
2	Override
1 Lowest	Manual switch

3.5.10.4 10/100BASE-T Operation

The 10BASE-T and 100BASE-T radios employ half-duplex and full duplex baseband transmission over two pairs of category 5/5E (CAT5/5E) balanced cabling. The aggregate data rate of 10/100 Mb/s is achieved by transmission at a data rate of 10/100 Mb/s over each wire pair. The data is transmitted over the RF path in burst of up to 10 Mb/s and 100 Mb/s, respectively.

3.5.10.5 1000BASE-T Operation

The 1000BASE-T (sometimes referred to in the industry as GigE) radio employs full duplex baseband transmission over four pairs of category 5/5E balanced cabling. The aggregate data rate of 1000 Mb/s is achieved by transmission at a data rate of 250 Mb/s over each wire pair. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pair at the same time. Data from the link partner is received in bursts of up to 1000 Mb/s and is transmitted over the RF path in bursts of up to 150 Mb/s.

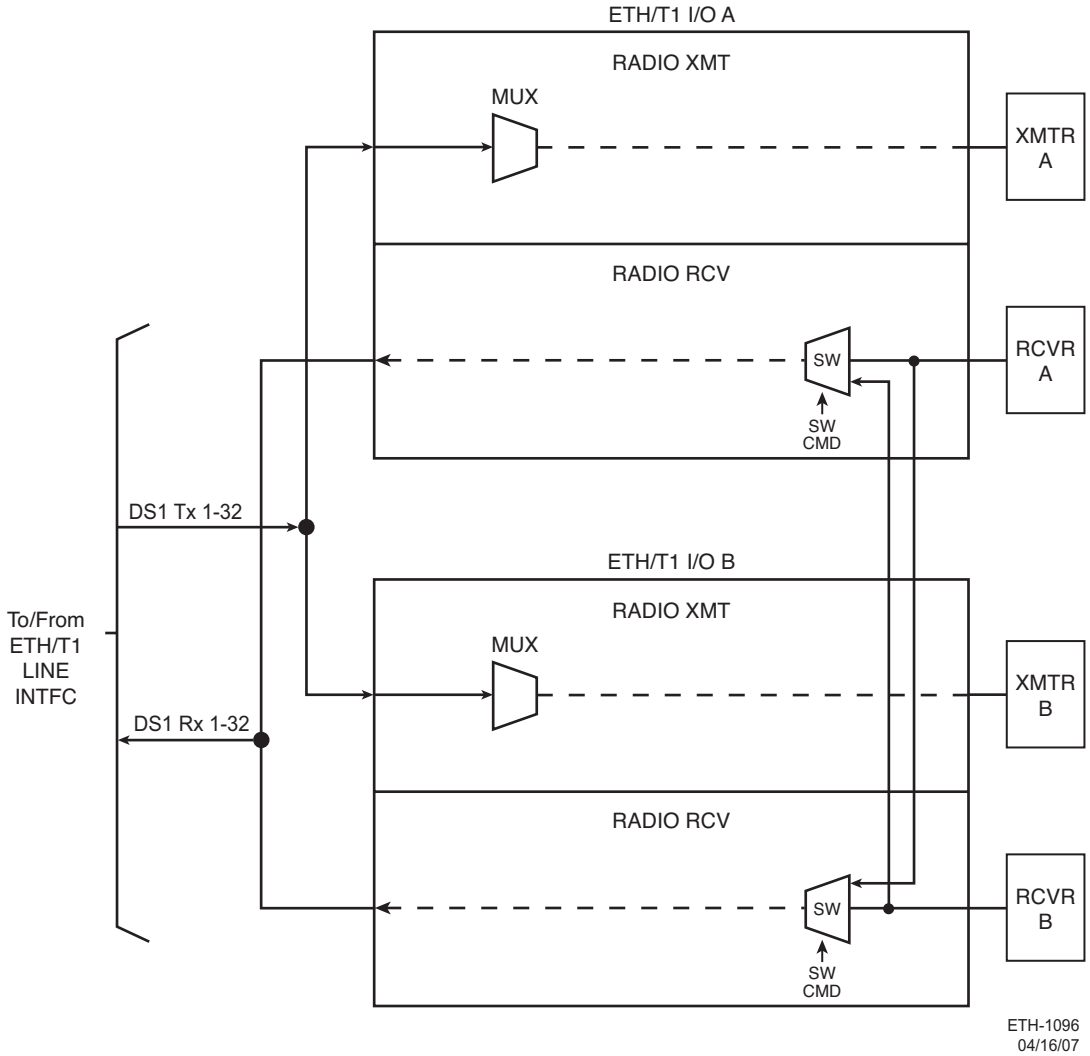


Figure 3-45 DS1 Switching

3.5.10.6 Ethernet Data Flow

See Figure 3-46. The DX-35S ETH/T1 I/O consists of the RJ45 connector, the Input/Output transformer, the Ethernet PHY, the ETHRA FPGA, and the T1/E1 Line Interface. A description of each follows.

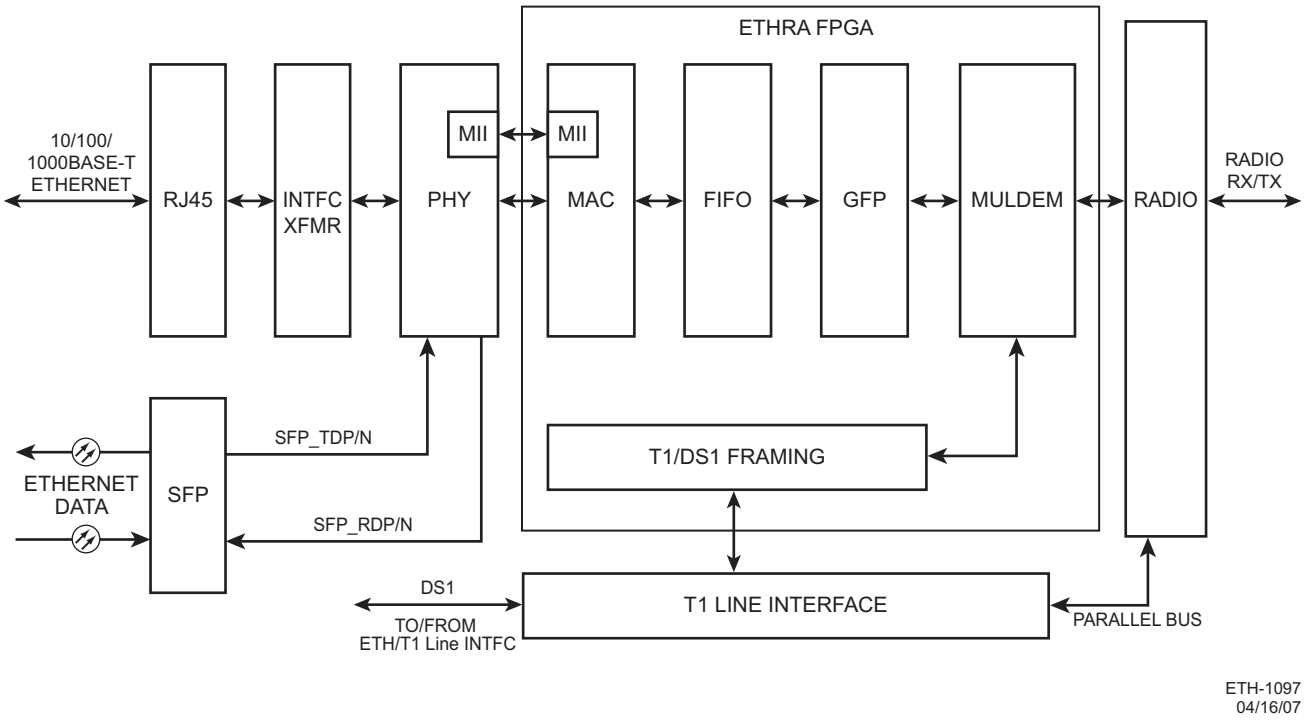


Figure 3-46 ETH/T1 I/O Data Flow Block Diagram

3.5.10.6.1 RJ45 Connector

The RJ45 connector is the Ethernet cable connection to/from the interface transformer on the ETH/T1 I/O module.

3.5.10.6.2 Interface Transformer

The transformer is used for signal coupling between the RJ45 connector and the Ethernet PHY block. Transformer coupling provides spike filtering and termination.

3.5.10.6.3 SFP

The Small Form-factor Pluggable (SFP) is used for signal coupling between the fiber optic cable and the Ethernet PHY block. The SFP is a compact optical transceiver.

3.5.10.6.4 Ethernet PHY

The PHY connects Ethernet media to the ETHRA FPGA (through Media Access Control) and defines the electrical signaling, line states, clocking guidelines, data encoding, and circuitry needed for data transmission and reception.

The PHY also performs auto-negotiation (detects the rate of incoming and/or outgoing data; 10BASE-T, 100BASE-T, 1000BASE-T) and selects the highest common input rate.

3.5.10.6.5 ETHRA FPGA (Ethernet Field Programmable Gate Array)

The main internal components of the FPGA are: MAC, FIFO, GFP, Muldem and T1/DS1 Framing block.

3.5.10.6.5.1 MAC (Media Access Control)

The MAC interfaces between Physical Layer (PHY) and the FIFO and primarily performs Ethernet Framing to wit:

- When receiving Ethernet data from the PHY (for Radio XMT), this component recognizes where frames begin and end in the bit-streams received.
- When transmitting data to the PHY (during Radio RX), the MAC delimits the frame by inserting some extra bits into or among the frames being sent to enable the receiver(s) to recognize the beginning and ending of the frames.
- The MAC employs cyclical redundancy checks (CRC) by the use of checksums to ensure the integrity of the bits in the frame to verify the frame is intact.
- The MAC implements SMMA/CD during half-duplex Ethernet RX mode.

3.5.10.6.5.2 FIFO Buffer (First Frame In - First Frame Out)

The First In First Out buffer (FIFO) connects between the MAC and the GFP processor. Its purpose is to transfer Ethernet data to the GFP for framing encapsulation prior to insertion in the service channel for radio XMT, and to receive decapsulated framed data from the GFP for transfer to the MAC and further transmission over the Ethernet.

In the Ethernet RCV/Radio XMT direction the three modules are: System Receive module (receives data from the MAC), the Fabric receive module (sends data to the GFP), and the Water Mark module. In the radio RCV/Ethernet XMT direction there are three sub-modules in the data path: the Fabric TX module (receives RF from the GFP), the System TX module (sends data to the MAC), and the Water Mark module (data flow control during data transfer). In both directions data is written to and read from the Generic Synchronous 2-port SRAM buffer.

During half-duplex operation, CSMA/CD mode is operational and collision effects are evaluated during data transfer. Excessive collisions will cause a cessation of transfer and removal of collision corrupted transferred data. During full-duplex operation, CAMA/CD is off and there are no collision effects to interrupt data flow.

In the Ethernet RCV/Radio XMT direction, Ethernet data is clocked into the egress FIFO eight bits at a time from the MAC through the System Receive module, written into FIFO memory in the sequence of arrival, read out of memory into the Fabric Transmit module, and

then, four bytes at a time, sent to the GFP. To begin transfer of data, the MAC sends the FIFO a Ready-To-Send signal and awaits the FIFO reply Ready-To-Receive. As the MAC sends its Ethernet data to the FIFO, it runs data validity checks. If the data is invalid because of corruption, or excessive collision effects, FIFO is notified to abort reception. When data transmission resumes, the data is written into memory by the System receive module. The data at the same time is being read out of memory by the fabric receive module. This module hand shakes with the GFP (Ready to Send/Ready to Receive). When GFP acknowledgement is received, the data is sent to the GFP four bytes at a time. In the GFP the data frame is encapsulated for insertion into the radio service channel.

In the Radio RCV/Ethernet XMT direction, RF data is clocked into the ingress FIFO four bites at a time through the Fabric Transmit module, written to FIFO memory in the sequence of arrival, read out of memory into the System Receive module and then transferred eight bits at a time to the MAC. During reception from the GFP to the FIFO the data undergoes validity checking by the Fabric Transmit module. If data is invalid, the Fabric Transmit module notifies the GFP to quit sending the present data and restart a new frame sequence. A Water Mark module in the FIFO is used to control data flow and assure that data threshold levels at all points of transmission and reception are within limits. In the case of under-run, the FIFO holds data in the buffer until more is received from the GFP module. In the Radio RCV/Ethernet XMT direction, a short frame (less than 64 byte frame length) is considered an error frame and is discarded.

3.5.10.6.5.3 GFP (Generic Framing Procedure)

The Generic Framing Processor (GFP) processes received Ethernet signals for transport over the radio network and processes received radio signals for transport over the Ethernet network. The processor preserves original control information and incurs very short transmission delay. The framing process incurs very short transmission delay. The framing process includes encapsulation (for radio transmission) and decapsulation (for Ethernet transmission), header processing, digital encoding/decoding, performance monitoring and more. The processor contains a simplified FIFO interface to connect to the ingress/egress FIFO.

During Ethernet RCV/Radio XMT, the processor receives the Ethernet signals from the FIFO via the FIFO Interface. It aligns character and control code, and maps consecutive characters into block code. Eight block codes are grouped into a superblock with core and payload headers. There is also a CRC-16 error check code added which calculates and inserts core and payload header error control into each transmitting GFP frame. The superblocks are then encapsulated as payload into periodic, fixed length GFP frames and inserted in the radio service channel for RF transmission.

During Radio RCV/Ethernet XMT, the processor receives the radio frames from the service channel, performs frame delineation and validation (core/payload header error control) for each received GPF frame, and decapsulates the data into a set of superblocks. The superblocks are then decoded into 8-bit characters (data and control codes) and sent to the egress FIFO via the FIFO interface.

3.5.10.6.5.4 Muldem

The muldem contains the circuitry to perform framing, to insert Ethernet, Service Channel, and data into the frames for radio transmitting, and in the case of radio receiving, remove data from the overhead and transfer it to the PHY for feed to the Ethernet cable. In the case of DS1, the data is DS1 framed in the T1/DS1 ETHRA circuitry and directed through the T1/E1 Line Interface to the Aux Interface.

3.5.10.6.5.5 T1/DS1 Framing

Frames the DS1 data for transmission to the T1 Line Interface.

3.5.10.6.5.6 T1 Line Interface

The T1 Line Interface interfaces between the ETHRA and the AUX card for WS DS1 signals and also connects to the backplane parallel bus for handling radio controller bi-directional data.

3.5.10.7 Ethernet RCV/Radio XMT Data Flow

See Figure 3-47. The ETH/T1 I/O data flow follows from board input at the RJ45 connector to the Coupling Transformer to the Physical Layer Device (PHY) and into the ethernet Regenerator Array (ETHRA). From there it leaves the Ethernet I/O Interface board and enters the radio path.

The PHY chip on the I/O board serves as the controlling influence for Ethernet data flow. When enabled for Auto-Negotiation, the PHY establishes a communication link with the far end PHY on the other end of the Ethernet cable (if it, too, has Auto-Negotiate capability) and between them they compare their abilities and connect at the highest common data transfer rate or mode (10BASE-T, 100BASE-T, or 1000BASE-T). Auto-Negotiation makes automatic connection of the highest data rate available without intervention from the user or from management software and ensures data integrity. If Auto-Negotiation is not enabled, the transfer will occur at a pre-configured rate.

The coupling transformer filters and terminates the incoming Ethernet signal and from there the data is picked off by the PHY for application to the ETHRA. Connecting the PHY and the ETHRA is the Medium Independent Interface (MII) circuitry. Since the MII circuits interface between the PHY and the ETHRA, identical circuits are located in the PHY and also in the Media Access Control (MAC) circuitry within the ETHRA. The MII circuits convert the line signals received by the PHY into digital format signals and provide them to the ETHRA via the MAC. the ETHRA multiplexes the Ethernet data with data from the serial service channel interface and wayside interface and converts the final multiplexed data into two X/Y data rail pairs. The X/Y data pairs are then applied to a serial scrambler. The scrambled X/Y data is applied to a Forward Error Correction (FEC) encoder circuit which uses Trellis Coded Modulation and Reed-Solomon coding. The encoded X/Y data steams are converted to I and Q data steams and clocked out of the ETHRA by the T CLK B input from the XMTR module BAUD VCXO. The TX1 1-4 and TX Q 1-4 data are applied to the transmitter module via connector J3A.

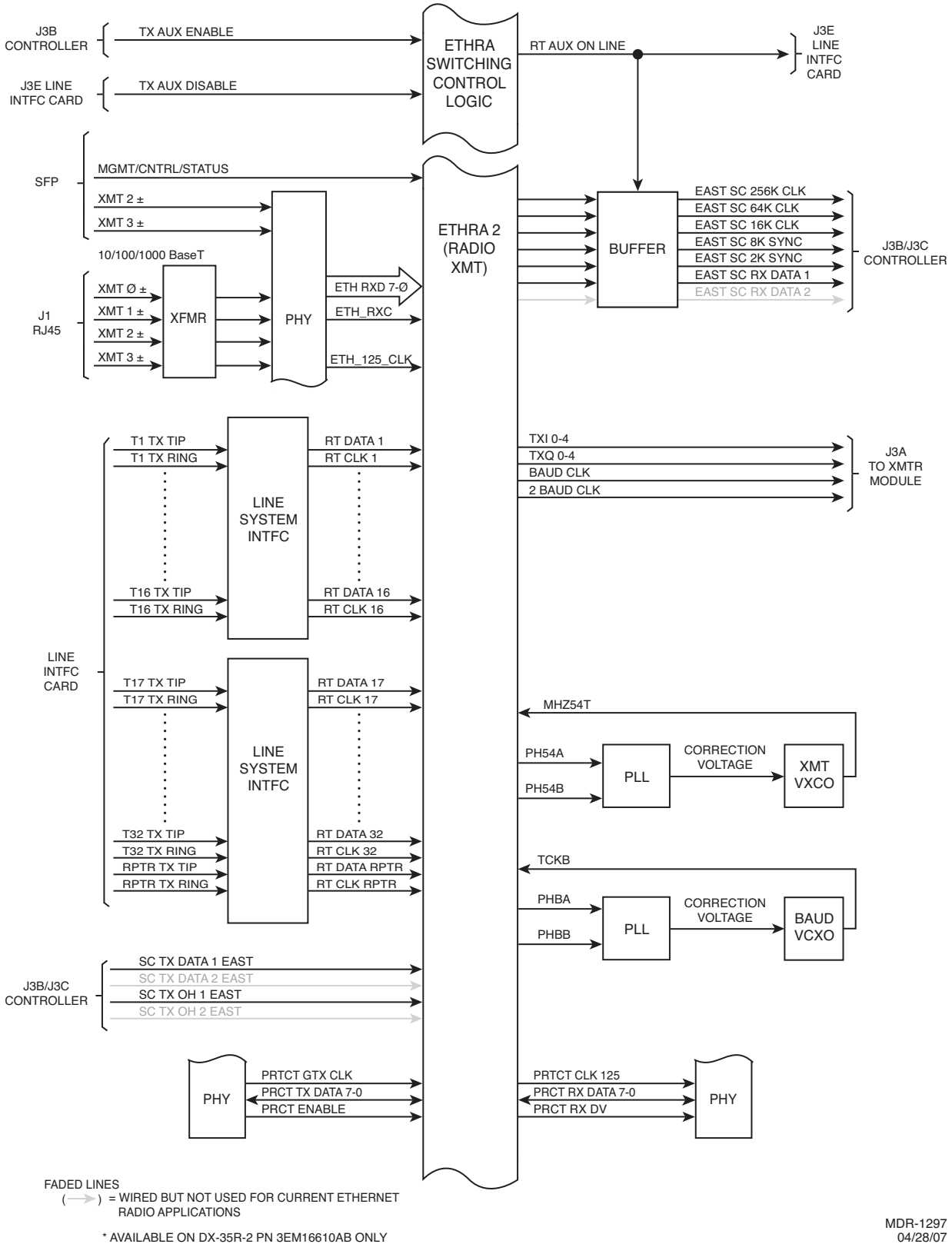


Figure 3-47 DX-35S ETH/T1 I/O Functional Block Diagram (Sheet 1 of 3)

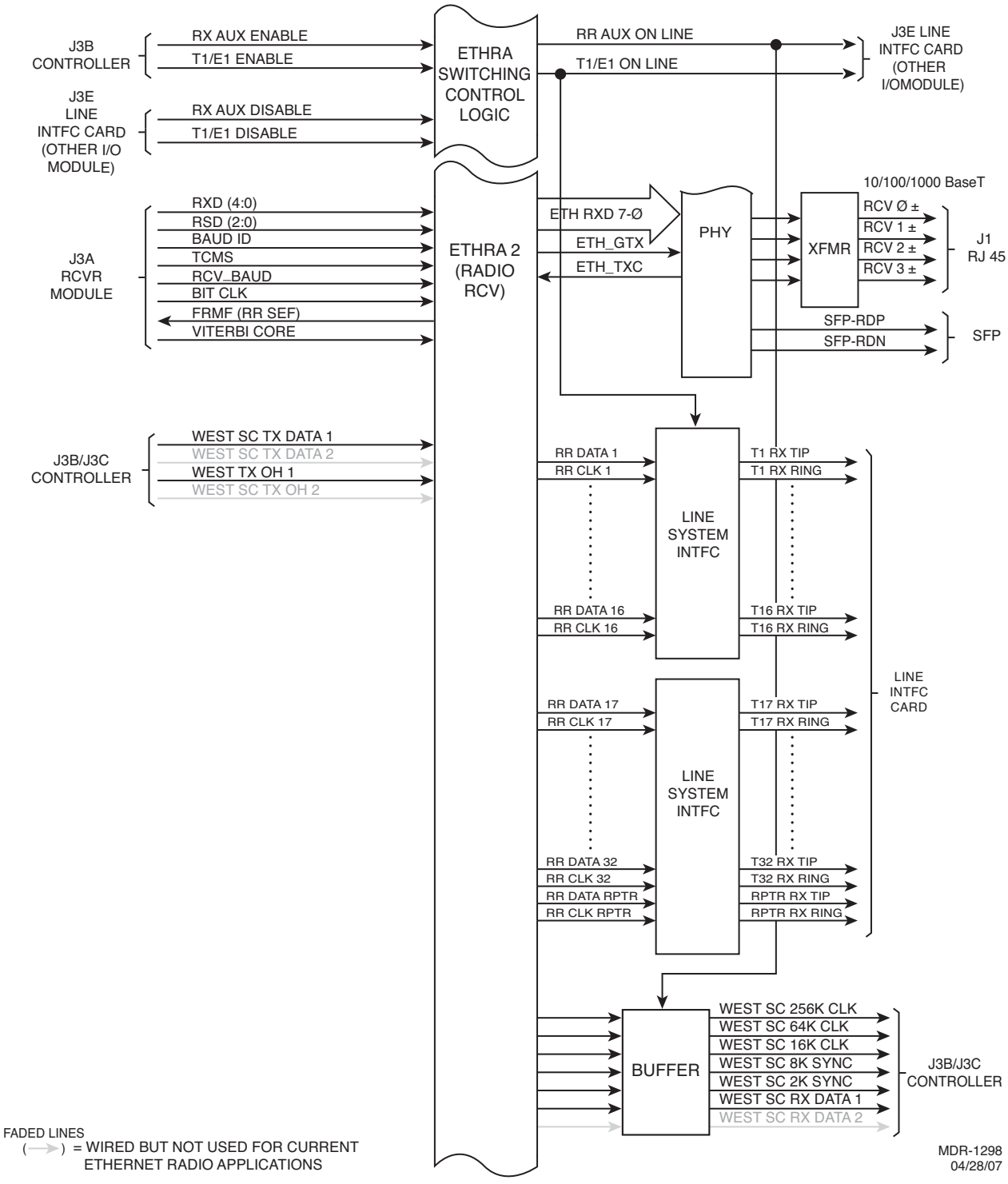


Figure 3-47 DX-35S ETH/T1 I/O Functional Block Diagram (Sheet 2 of 3)

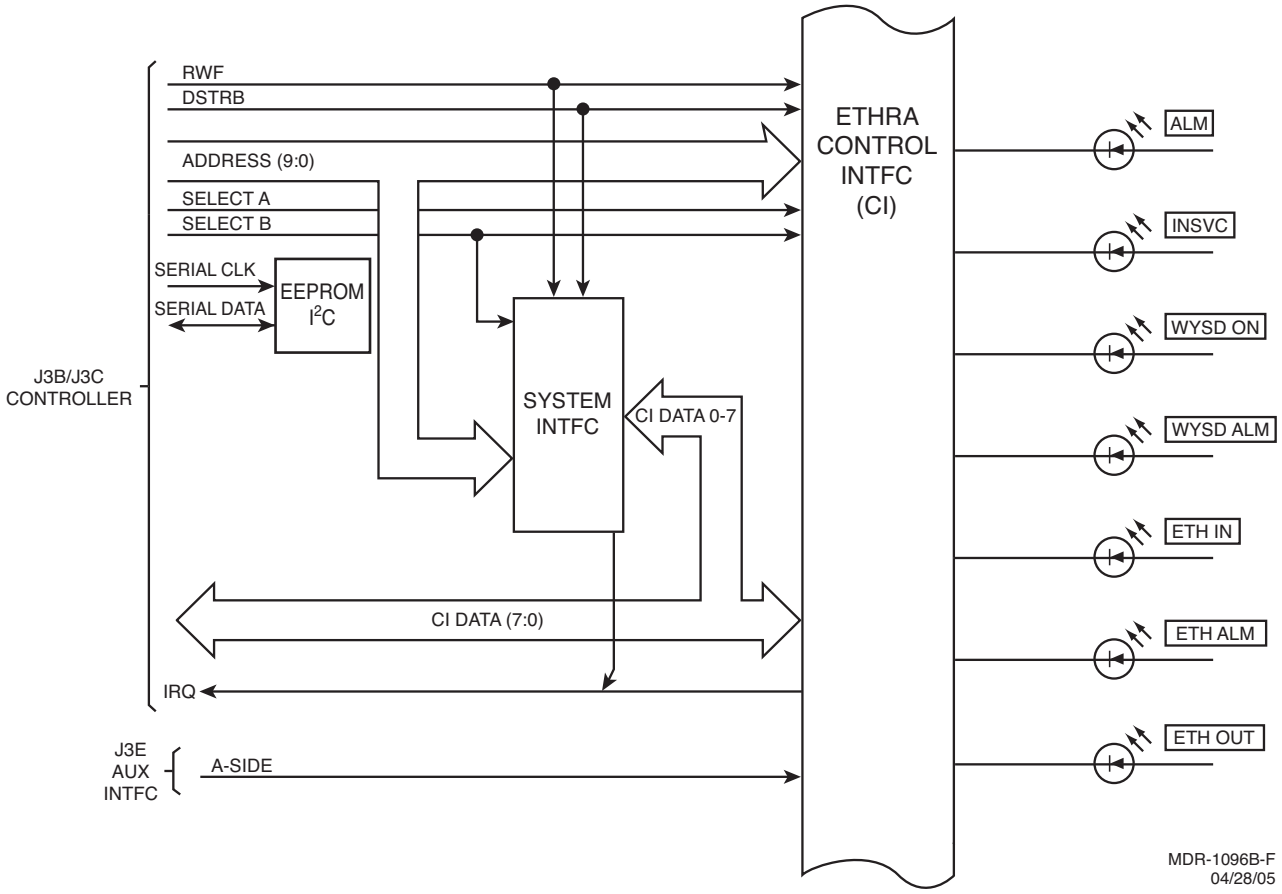


Figure 3-47 DX-35S ETH/T1 I/O Functional Block Diagram (Sheet 3 of 3)

3.5.10.7.1 XMTR Module Interface

The XMTR module interface at connector J3A receives Transmit Data (TX1 1-4 and TXQ 1-4), BAUD CLK, and 2 BAUD CLK (twice the frequency of BAUD CLK) from the ETHRA.

3.5.10.7.2 T1 Interface

The line system interface circuit provides clock recovery, clock smoothing, elastic buffering and line encoding for each T1 channel.

The T1 tip and ring signals are applied to the line system interface circuits via connector J3E. The balanced tip and ring signals consist of pulsed square waves at 1.544 Mb/s. The line system interface circuit bridges the RZ data onto one channel, converts the balanced tip and ring signals to NRZ data, B3ZS encodes the data, and using the recovered clock, writes the data into an elastic buffer. In the elastic buffer, the recovered clock is compared to the low-speed clock created by the ETHRA and if a mismatch is detected, stuffing bits are inserted. The RT DATA 1-32 outputs of the line system interface circuits are clocked into the ETHRA by the respective output clocks.

3.5.10.7.3 Service Channel Interface

Refer to service channel demultiplex description later in this section for RCV details. The DX-35S ETHRA receives inserted service channel 1 data from the AE-37Y-1 controller module via connector J3B. Service channel 2 data from the controller is wired (J3C) but not used for the Ethernet radio applications.

Overhead MUX circuitry in the ETHRA receives local insert-service channel data (SC TX DATA 1 EAST, SC TX DATA 2 EAST, SC TX OH 1 E, and SC TX OH 2 E) from the service channel muldem in the controller module. The EAST SC TX DATA is clocked into the ETHRA by the controller using the EAST SC CLOCKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST C 8K SYNC, and EAST SC 2K SYNC) provided by the ETHRA. In the ETHRA, the service channel insert data (EAST SC TX DATA) is inserted into the radio frame overhead.

3.5.10.8 Radio RCV/Ethernet XMT Signal Flow

See Figure 3-47. The DX-35S ETH/T1 I/O RCV circuits receive parallel RX and RS data signals; an BAUD CLK from the RCVR module. The ETHRA demultiplexes/decodes these inputs to form Ethernet data, auxiliary (overhead data), and a reference sync signal. The overhead data contains a 262 kb/s service channel, a 1.544 Mb/s WDS1 per each DS1, and two 16 kb/s command path channels.

3.5.10.8.1 RCVR Module Interface

The RCVR module interface at connector J3A consists of Receive Data (RXD), Receive Subset data (RSD), BAUD Identification (ID), Trellis Code Modulation Sync (TCMS), Receive BAUD clock (RCV BAUD), Bit Clock (CLK), Frame False (FRMF) and Viterbi Correcting Errors (VITERBI CORE).

RCVR module interface circuits consist of a retime circuit and Forward Error Correcting (FEC) circuit. RXD and RSD signals from the RCVR are clocked into the retime circuit by the BAUD CLK. The retime circuit retimes these to the baud clock and the signals are then applied to the ETHRA FEC circuit. The FEC circuit removes the FEC encoding placed on the data stream by the MDR-8000 XMTR at the other end of the hop.

3.5.10.8.1.1 ETHRA Functions

The ETHRA performs Reed-Solomon decoding, descrambling, radio frame detection and alignment, extracting service channel and DS1 overhead channels, elastic buffering, frame detection, PVMR, data rate adjustment to interface with FEC array, phase/frequency detection, and alignment signal generation.

3.5.10.8.1.2 Parity Byte

Parity bits are continuously monitored and a parity error pulse is generated when a mismatch is detected.

3.5.10.8.2 T1 Interface

The DX-35S uses a line system interface ASIC for T1 signal processing. The demultiplex section of each line system interface ASIC receives 16 channels of T1 data and clocks. The 16 channels of data are clocked into an elastic buffer. The data is then converted to a quasi-RZ format and encoded, according to the modulation mode. The encoded data is sampled in an AIS detector for loss of signal, demultiplexed onto two (T&R) channels, and converted to RZ

data. TEO (trailing edge overshoot) pulses are added to the RZ data so that the pulses conform to cross-connect requirements without the need for an external equalizer. Tip and ring outputs for each channel are applied to the MDR-8000 interface via connector J3E.

3.5.10.8.3 Service Channel Interface

Refer to service channel multiplex description previously described in this section for XMT details. The DX-35S sends service channel 1 data to the AE37Y-1 controller module via connector J3B. Service channel 2 data from the controller is wired (J3C) but not used for the Ethernet radio applications.

See Figure 3-48. The service channel interface at the ETHRA in the Ethernet I/O interface consists of the WEST SC RX DATA, WEST SC CLKS (WEST SC 256K CLK, WEST SC 64K CLK, WEST SC 16K), and WEST SC SYNC (WEST SC 8K SYNC, WEST SC 2K SYNC) outputs. In the ETHRA, the service channel data (WEST SC RCV DT) is removed from the radio frame overhead and is sent to the service channel muldem in the controller module. The WEST SC RX DATA is clocked into the controller by the ETHRA using the WEST SC CLOCKS provided by the ETHRA.

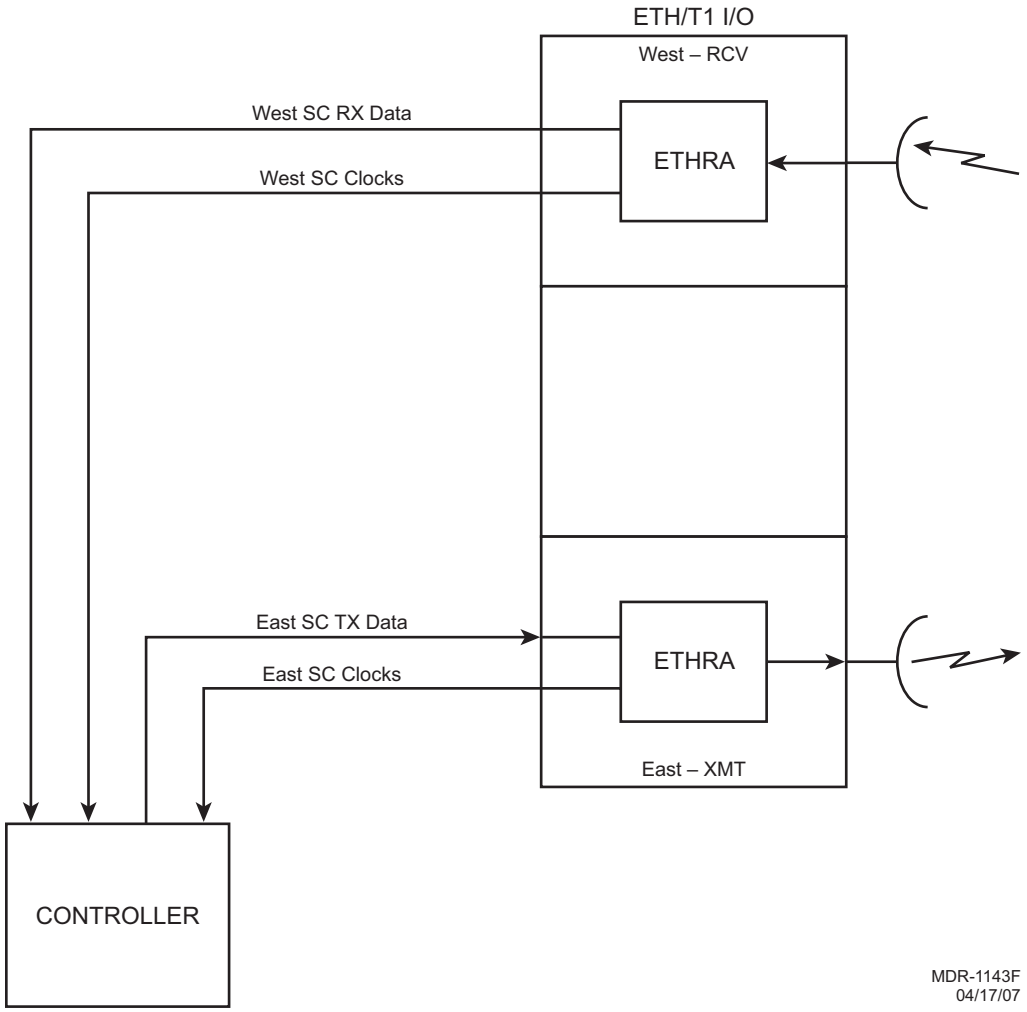


Figure 3-48 ETHRA Service Channel Interface Functional Block Diagram

3.5.10.9 Control and Monitor Functions

3.5.10.9.1 Controller Interface

See Figure 3-47. The controller interface is used to transfer alarm and status information to the AE-37( ) Controller.

Alarms generated in the ETHRA are latched in the controller interface until they are acknowledged by the system controller. Ethernet receive/radio transmit alarms generated by the ETHRA include: Severely Errored Frame (SEF), Loss of Frame (LOF), Parity Error, and Loss of Signal (LOS).

3.5.10.9.2 SEF

SEF is declared when a minimum of four consecutive errored framing patterns has been received. SEF is cleared when a minimum of two consecutive error-free framing patterns have been received.

3.5.10.9.3 LOF

LOF is declared if the SEF state persists for a count comparable to 23 frames. LOF is cleared when the signal remains in-frame for a minimum of one millisecond.

3.5.10.9.4 Parity Error

The parity checker calculates CRC-8 parity over all the bytes of the STSn frame and checks this calculated parity against the RCV parity (B1 byte) in the next frame. An error is declared if a mismatch or error is detected.

3.5.10.9.5 LOS

LOS is declared when an all zeros pattern is received on all four bits of nibble data (a minimum of 100 microseconds).

Data is sent and received during a two-byte transfer. The first byte is a pull byte that selects the device ID and register address. It also controls whether a read or write operation is taking place. The second byte contains data from the selected register.

3.5.10.9.6 Provisioning Inputs

The I/O interface receives the following provisioning inputs (PROV 1-8) from capacity keys on the XMTR and RCVR modules:

- modulation scheme
- local oscillator control source (pedestal voltage or PLL)
- STS1 operation and umber of STS1 lines enabled
- data scrambled or passed data through unmodified

- stuff rate source for stuffing DS1/E1 signals in radio frame (average stuff rate or stuff request signals from DS1 interface ASIC)
- enables or disables data scrambler stuck pattern (all 1's, all 0's, or alternating 1's and 0's).

3.5.10.9.7 I^2C Bus

The I^2C (Inter-Integrated Circuit) bus is for inventory control and communicates module part number, serial number, and revision history information to the AE-37( ) Controller.

3.5.10.9.8 Loopback Controls

Refer to loopback information on the Control screen for details. To access the Control screen:

1. Click here to enter Controls guide. Main screen will open.
2. On the Main screen, on dropdown for type of radio, click on ETH. ETH Status Alarm screen will open.
3. On ETH Status Alarm screen, on tool bar, click on User Control. User control screen will open.
4. On User Control screen, click on loopback function.

3.5.10.9.9 Alarms

- ALM – red LED, indicates I/O interface module failure
- ETH ALM – yellow LED, indicates ETHERNET receive circuit failure.

3.5.10.9.10 Status

INSVC – green LED, indicates XMT and/or RCV circuits are passing data

ETH IN – green LED. This activity monitor indicates data on input to ETHERNET RCV/ RADIO XMT circuits.

ETH OUT – green LED. This activity monitor indicates data on output from RADIO RX/ETH-ERNET XMT circuits.

3.6 TRANSMITTER SUBSYSTEM FUNCTIONAL DESCRIPTION

See Figure 3-49. The transmitter subsystem consists of a QAM transmitter, and a power amplifier (optional). The purpose of the transmitter is to convert digital baseband signals to a QAM RF signal and transmit the signal. The following paragraphs describe the operation of the transmitter subsystem.

The digital baseband signals are converted to analog baseband signals that are then converted to an RF QAM signal by mixing the analog baseband with a multiplied crystal oscillator. The 2GHz I/Q modulator output is up-converted to the desired RF frequency and amplified to a medium power RF signal. If higher power is required the signal is sent to the UD-51( ) Power Amplifier before being sent to the antenna. The RF QAM signal is amplified and applied to the antenna via a transmit filter.

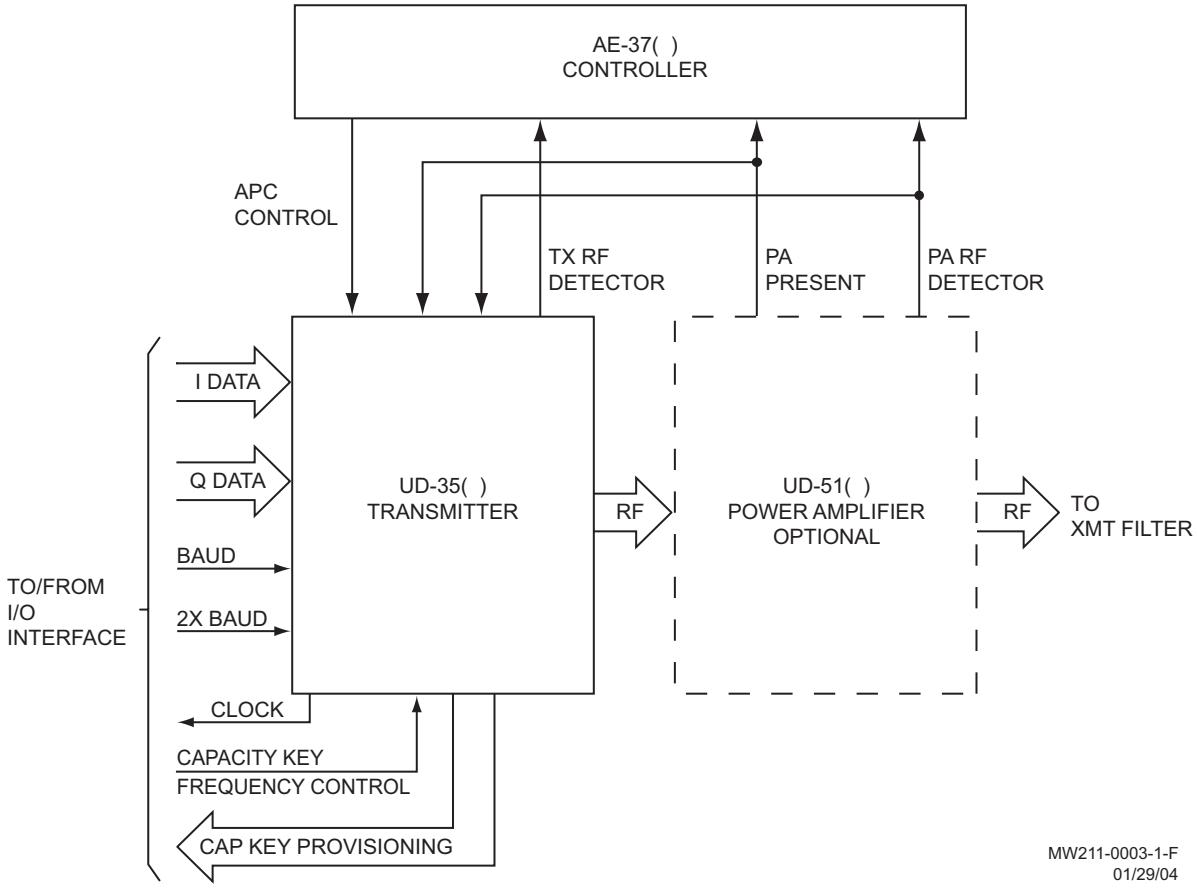


Figure 3-49 Transmit Function Block Diagram

3.6.1 XMT Monitor Points Vs USI

XMT power is referenced at the antenna output of the diplexer/filter or at the top of the stack for waveguide stacking configuration. Transmitter and Power Amplifier module monitor voltages and USI monitor voltages are relative values. The values can be recorded as reference voltages at initialization and then checked periodically for degradation.

See Figure 3-50. There is no correlation between the DC MON test point on the PA front panel, the PA RF MON input to the controller, and the PA (DC MON) reading on the USI. The PWR Mon test point on the XMTR front panel is not designed to match the XMTR RF MON voltage at the input on the controller and the TX (PWR MON) voltage on the USI; however, it is common to find less than 1% difference.

If the shelf is not equipped with a PA, the RF monitor voltage from the RF coupler/detector on the XMTR output is switched to the XMTR AGC circuits. The detected RF monitor voltage from the PA is switched to the AGC circuits on the XMTR module by the PA Present control signal from the PA when equipped. The AGC circuit controls the gain of the XMTR output amplifier.

3.6.1.1 XMTR PWR Mon

The voltage on the PWR MON test point on the XMTR front panel is not adjustable. The output monitor is driven by the unity gain buffer. This reference voltage on this test point and/or the voltage displayed on the TX (PWR MON) display on the USI Analog screen are useful as a troubleshooting aid when the shelf does not have a PA. If the shelf is equipped with a PA, the PA voltages should be used.

3.6.1.2 PA DC Mon

The voltage on the DC MON test point on the PA front panel is adjustable on earlier versions of the PA and is normally only factory adjustable on later versions (the control is covered by the output level label). The output monitor circuit is driven by the level shifter. The reference voltage on this test point and/or the voltage displayed on the PA (DC MON) display on the USI Analog screen are useful troubleshooting aids.

At the factory, the DC MON test point on the PA front panel is set for 0.1 volts per dB output power (e.g. 2.9v = 29dB output power).

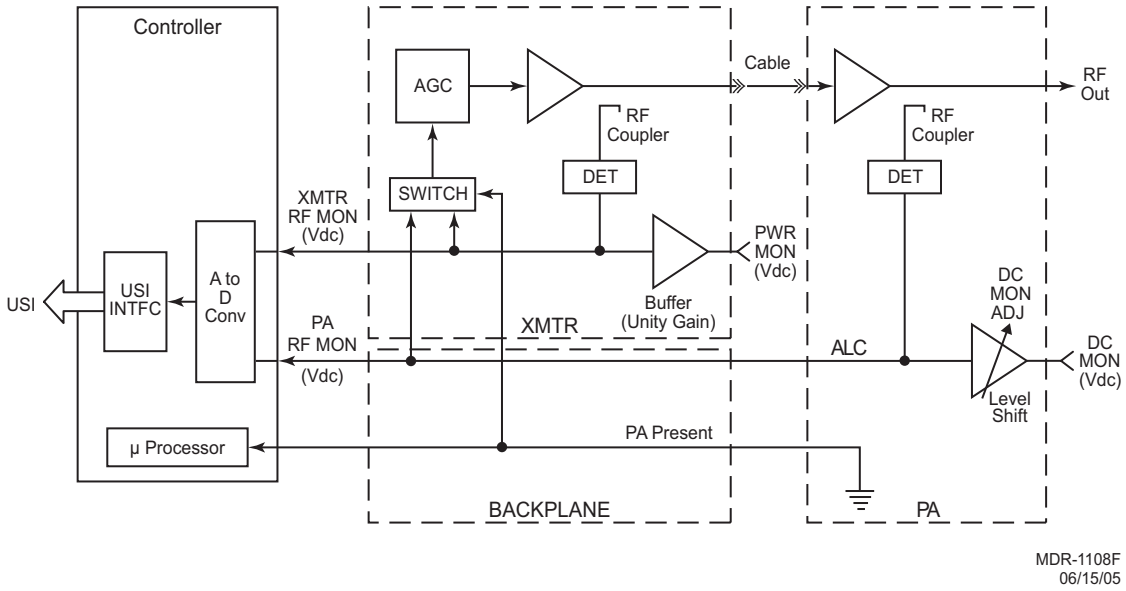


Figure 3-50 XMTR/PA Test Points Functional Block Diagram

3.6.1.3 Controller

The XMTR RF MON and PA RF MON voltages are applied to the analog to digital (A to D) converter circuits on the controller. The digital outputs are read by the USI in the USI interface circuits.

3.6.2 Automatic Level Control (ALC)

When ATPC is disabled, ALC analog circuits control the output power level of the XMTR module or the PA (if equipped). The ALC loop function is disabled if ATPC is enabled.

3.6.2.1 XMTR ALC Loop (Analog)

See Figure 3-51 for the XMTR ALC loop signal flow. When the radio is not equipped with a PA, the RF output of the XMTR module is detected and looped back to control the level of the IF input to the up-converter. Lack of a ground on the PA PRESENT signal causes the PA/XMTR select switch to switch the XMTR RF DETECTOR VOLTAGE from the RF detector to the integrator circuit in the XMTR module. Integrator circuit gain is controlled by the front panel XMT LVL control. The control voltage developed in the integrator circuit is switched to the voltage controlled variable attenuator that controls the level of the IF signal to the upconverter.

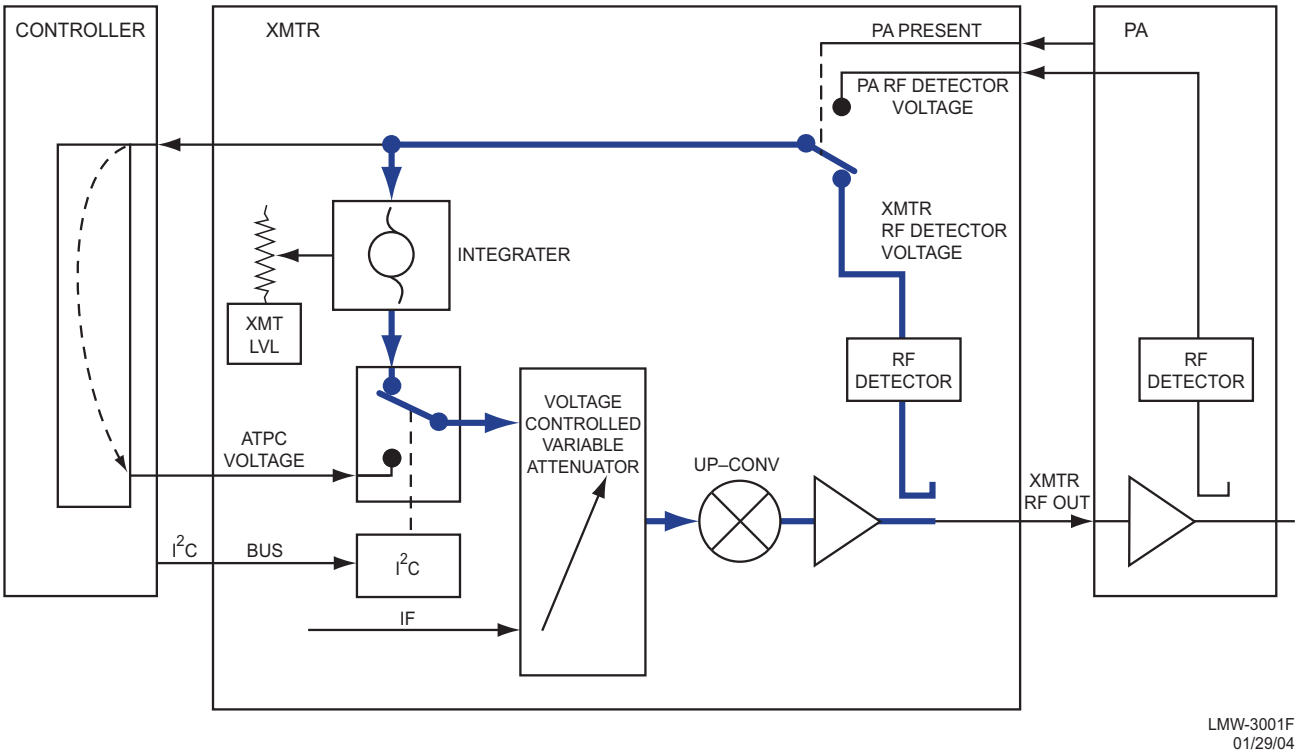


Figure 3-51 XMTR ALC Loop (Analog) Signal Flow

3.6.2.2 PA ALC Loop (Analog)

See Figure 3-52 for the PA ALC loop signal flow. When the radio is equipped with a PA, the RF output of the PA module is detected and looped back to control the level of the IF input to the up-converter on the XMTR module. The PA PRESENT signal causes the PA/XMTR select switch to switch the PA RF DETECTOR VOLTAGE from the RF detector to the integrator circuit in the

XMTR module. The control voltage developed in the integrator circuit is switched to the voltage controlled variable attenuator that controls the level of the IF signal to the upconverter. The output of the up-converter is amplified and applied to the fixed-gain amplifier in the PA.

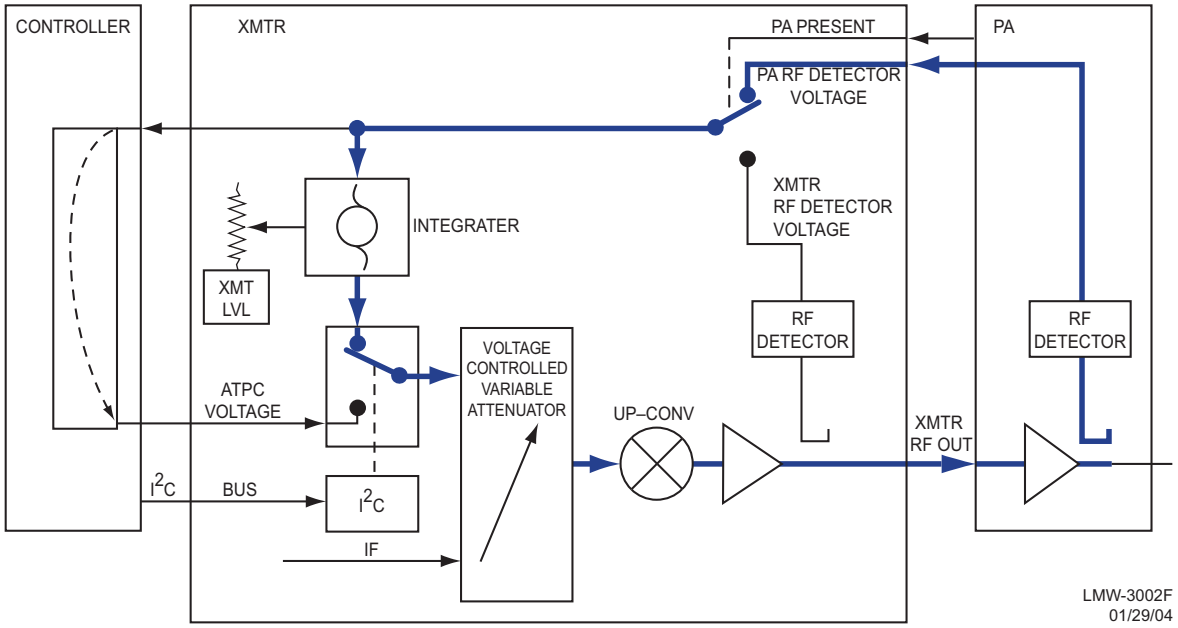


Figure 3-52 PA ALC Loop (Analog) Signal Flow

3.6.3 Automatic Transmit Power Control (ATPC)

When the radio is equipped with the optional PA, ATPC is a provisioning option and can be used to reduce the transmit power to approximately 10 dB below maximum under normal path conditions. ATPC loop functions depend on the output power level. There are two loop modes of operation; high and low power digital ALC loop and end-to-end digital ALC loop.

3.6.3.1 High and Low Power Digital ALC Loop

See Figure 3-53 for the XMTR ATPC loop signal flow. In this loop mode of operation, the ATPC power is at the high or low rail and the level is maintained by the controller module. The RF output of the XMTR module is detected and looped back to control the level of the IF input to the up-converter. Lack of a ground on the PA PRESENT signal causes the PA/XMTR select switch to switch the XMTR RF DETECTOR VOLTAGE from the RF detector to the controller module. The control voltage developed in the controller modules switched to the voltage controlled variable attenuator that controls the level of the IF signal to the upconverter. The output of the up-converter is amplified and applied to the XMT filter.

See Figure 3-54 for the PA ATPC loop signal flow. In this loop mode of operation, the ATPC power is at the high or low rail and the level is maintained by the controller module. The RF output of the PA module is detected and looped back to control the level of the IF input to the up-converter on the XMTR module. The PA PRESENT signal causes the PA/XMTR select switch to switch the PA RF DETECTOR VOLTAGE from the RF detector to the controller module. The control voltage developed in the controller modules switched to the voltage controlled variable attenuator that controls the level of the IF signal to the upconverter. The output of the up-converter is amplified and applied to the fixed-gain amplifier in the PA.

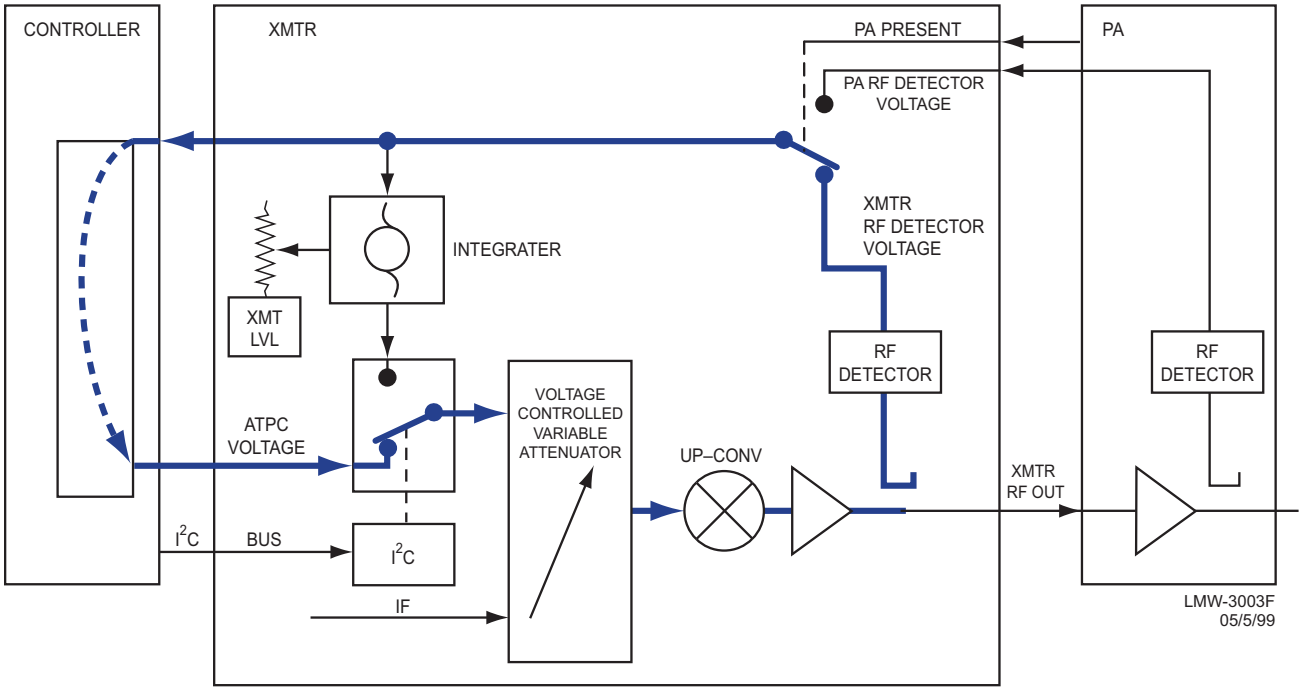


Figure 3-53 XMTR ATPC Loop (Digital) Signal Flow

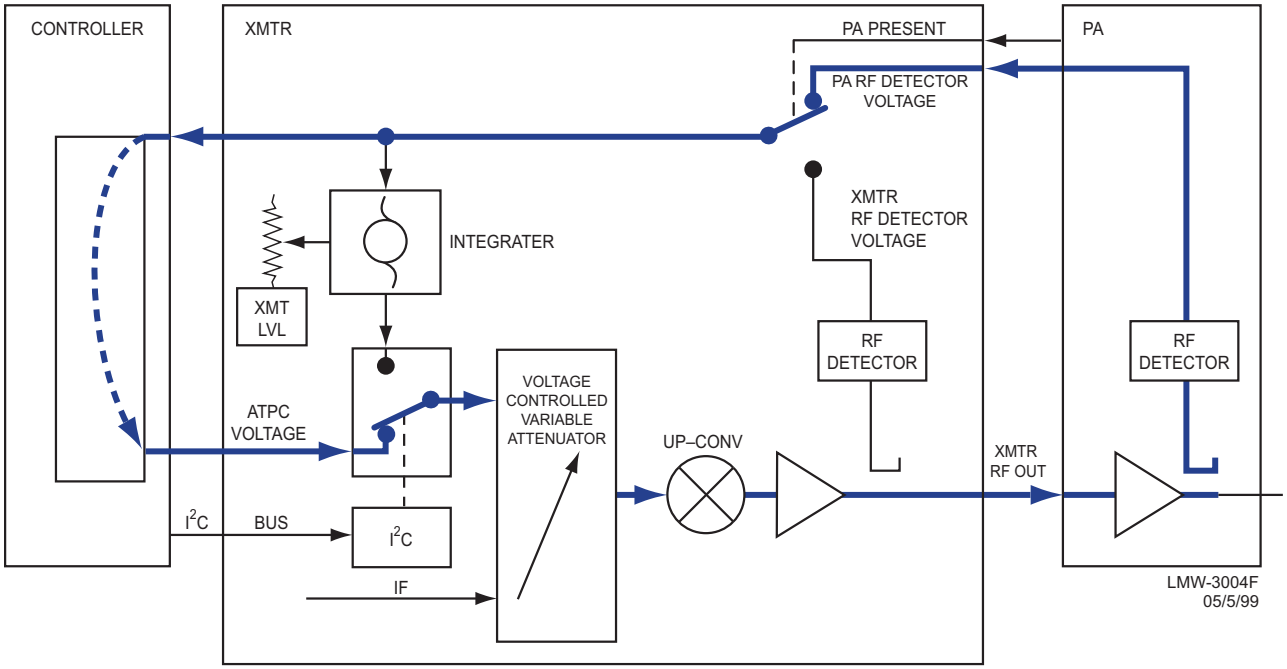


Figure 3-54 PA ATPC Loop (Digital) Signal Flow

3.6.3.2 End-to-End Digital ALC Loop

See Figure 3-55 for the active region ATPC loop signal flow. In this loop mode of operation, the ATPC power is in the active region (level is between low and high power rails) and the far end receiver controls the transmitter via the return command path. During faded path conditions, low RSL detected in the far end receiver causes an increase in transmit power at the upstream transmitter.

The radio can be operated with the ATPC disabled, enabled, or enabled with timeout. Select ATPC disable for maximum power out of the PA at all times. Select ATPC enabled with timeout to force ATPC to low power when the high power alarm is activated. An ATPC high power alarm is generated if the ATPC is active for more than five minutes without returning to low power. ATPC remains at low power until the far end receiver requests an ATPC power reduction.

In normal ATPC operation, the transmitter gain and PA bias control are under software supervision. The transmitter is set for low gain (10 dB below full gain) and the PA is set for low bias. The low bias reduces the current consumption in the output stage of the PA to save power and reduce heat dissipation. When ATPC is provisioned disabled, the PA operates at full output power. In hot-standby transmitters, the bias control of the off-line PA is set to low bias with the transmitter gain set at full.

The near end transmitter sends status information to the far end to indicate if the ATPC is able to go up or down. The far end receiver monitors the RSL voltage from the on-line receiver and compares this voltage to a preset threshold voltage (representative of approximately -65dBm RSL). If the RSL voltage is higher than the threshold voltage and the near end transmitter status indicates the ATPC can go down, a down request is sent to the near end transmitter. If the RSL voltage is lower than the threshold voltage and the near end transmitter status indicates the ATPC can go up, an up request is sent to the near end transmitter. The down and up messages are sent from the far end transmitter over the return path in an internal 16 kb/s command channel in the radio overhead. The near end controller module receives the messages from the near end receiver and moves the ATPC one step (approximately 0.5 to 1.0 dB) down or up.

Any time ATPC is not at low gain, the PA bias is enabled so that maximum PA linearity is available. In hot-standby transmitters, the off-line transmitter gain is set to track the on-line gain. In frequency diversity systems, the A and B ATPC operate independently.

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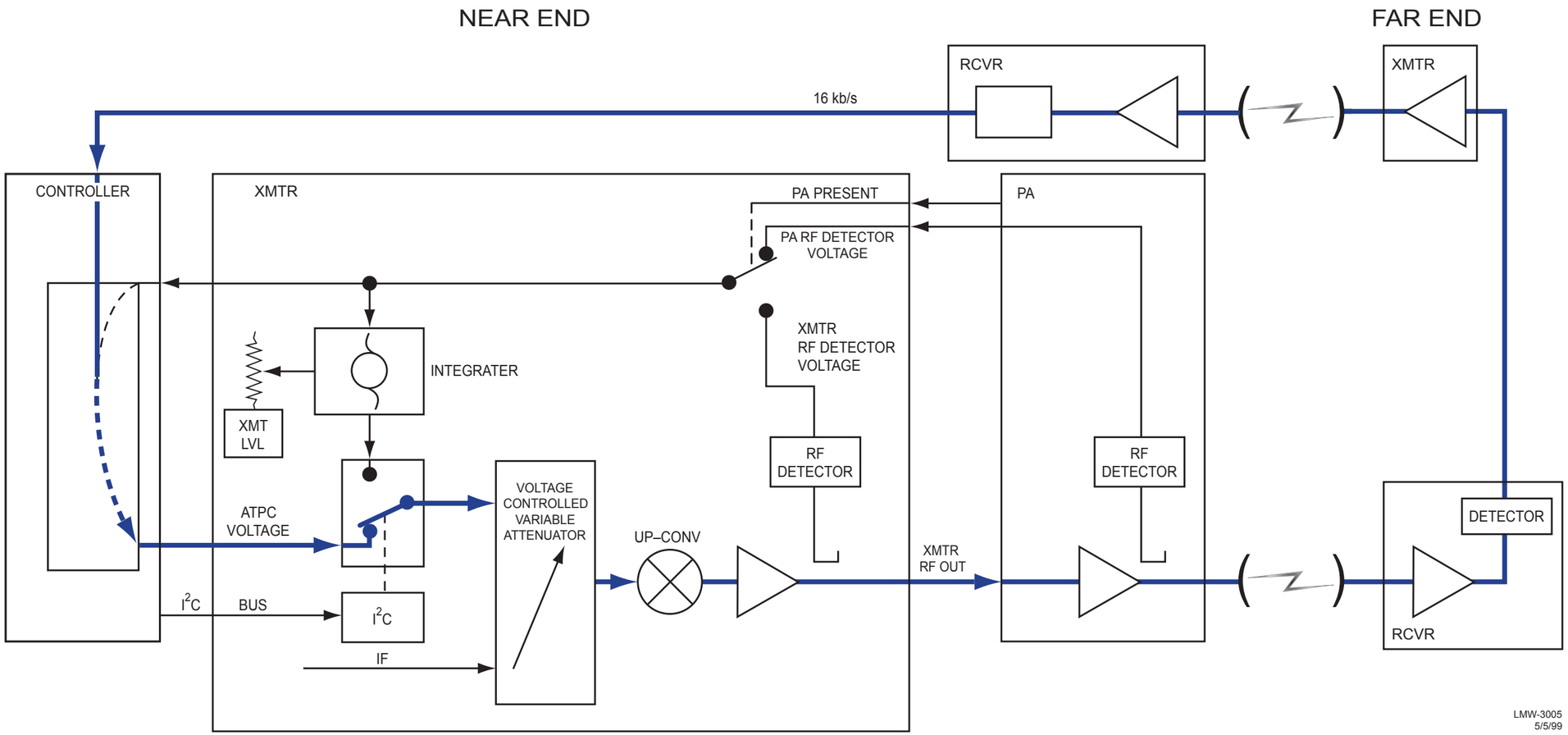

Figure 3-55 Active Region ATPC Loop Signal Flow

3.6.4 Transmitter Switching

Manual switches are provided on the AE-37Y Controller module to manually switch the transmitters. Under normal operation, the manual switches will be in the AUTO position, which allows the switching decisions to be made by the controller module based on alarm information.

3.7 TRANSMITTER SUBSYSTEM MODULES

Modules are described to the functional block diagram level in the following paragraphs. Modules are described in transmit signal flow order.

3.7.1 UD-35( ) Transmitter

See Figure 3-56, Figure 3-57, Figure 3-58, and Figure 3-59. The UD-35( ) Transmitter consists of the baseband modulator board, capacity key subboard, and a RF modulator subboard with accompanying crystal oscillator subboard. The transmitter converts I and Q baseband signals into an IF spectrum in the 1.5-2.5 GHz range depending on the RF frequency desired.

3.7.1.1 BB Modulator Board

See Figure 3-57. On the BB modulator board, the digital I/Q data rails are digitally filtered and converted to an analog I/Q baseband. The aliases are removed and the signal is amplified.

3.7.1.2 Oscillator FREQ CONT

This front panel control fine tunes the crystal oscillator resonant frequency.

3.7.1.3 XMT Enable/Disable and Online Controls

In a protected system, the controller enables the online XMTR via the A/B XMT ENABLE signal. The enable signal causes the control logic to turn on the IN SERVICE LED and an XMT ON LINE output signal is sent to the other XMTR module as a XMT DISABLE input. On the other XMTR, the XMT DISABLE signal is applied to the control logic and turns off the XMTR. In a protected system with the RF switch, when the selected XMTR is on line, the SWITCH signal from the control logic circuit is applied to the RF switch and switches the XMTRs.

3.7.1.4 XMT LVL Control

This front panel control adjusts the RF output power of the XMTR by changing the correction voltage applied to the output variable attenuator. Refer to the description of the ALC loop for details.

3.7.1.5 Capacity Key

The capacity key (PN 967-1609-001 through 020) consists of an I^2C (Inter-Integrated Circuit) EEPROM, I and Q low-pass filters, VCXO, and pull-down resistor array. The I^2C EEPROM communicates part number, serial number, and revision history to the I^2C select circuit on the BB MOD board. The I and Q filters are baud clock frequency dependent. The filtered I and Q outputs are applied to the RF MOD subboard. The VCXO is frequency dependent and derives the CAPACITY CLOCK output (baud clock) from the CAPACITY KEY FREQ CONTROL input. The pull-down resistor array uses a 6-bit word (PROV 1-8) to communicate to the controller how the radio is configured. The PROV 1-8 outputs select the type of radio and provision the trellis coded modulation scheme (32/128 TCM).

3.7.1.6 Crystal Oscillator Subboard

See Figure 3-58. The crystal oscillator board operates in the 105-150 MHz range depending on the RF requirements. The oscillator is a low phase noise oscillator. The output is interfaced to the RF modulator board at 50 ohms at a +10dBm level.

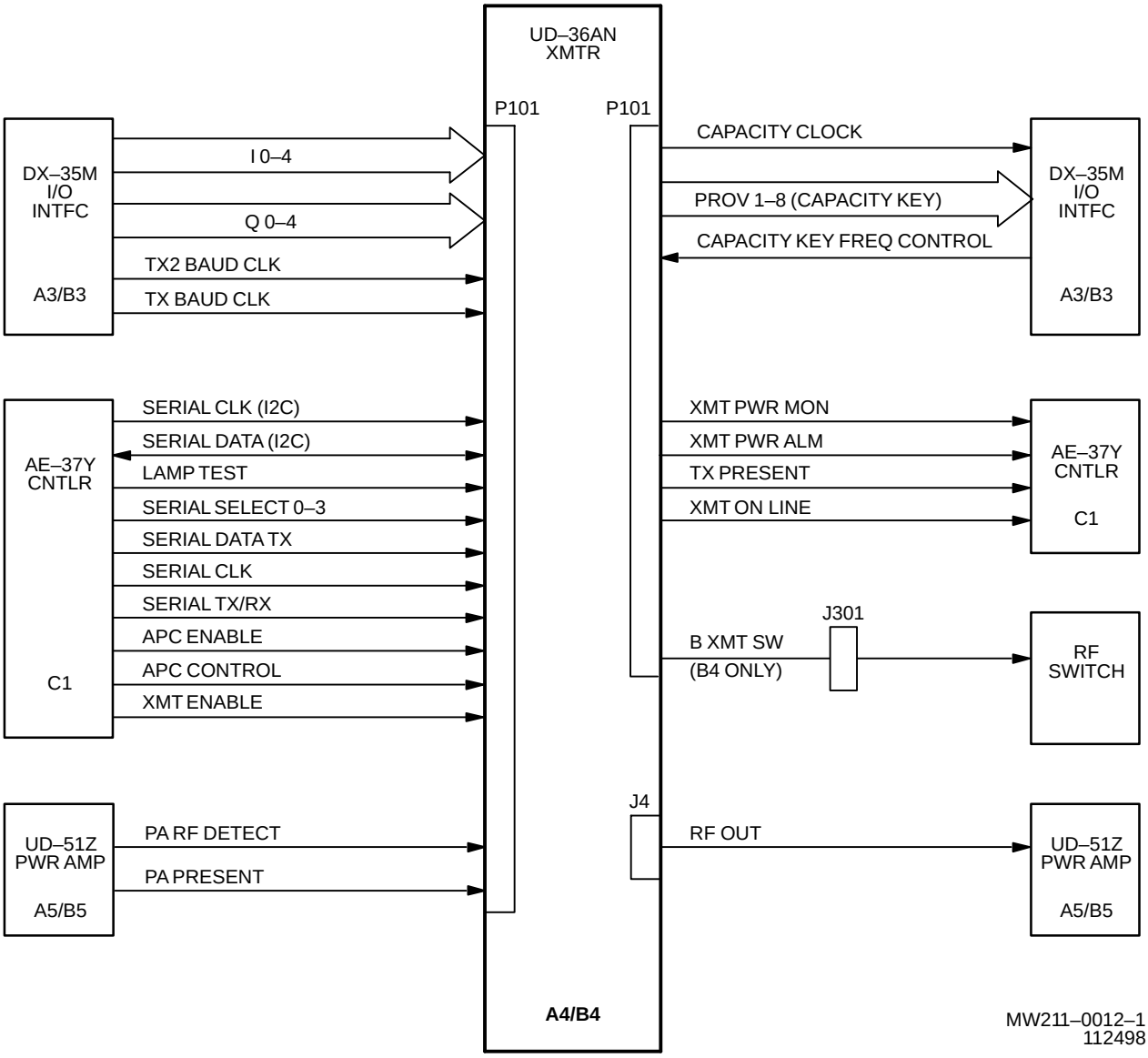

Figure 3-56 UD-35( ) Transmitter Interconnect Diagram

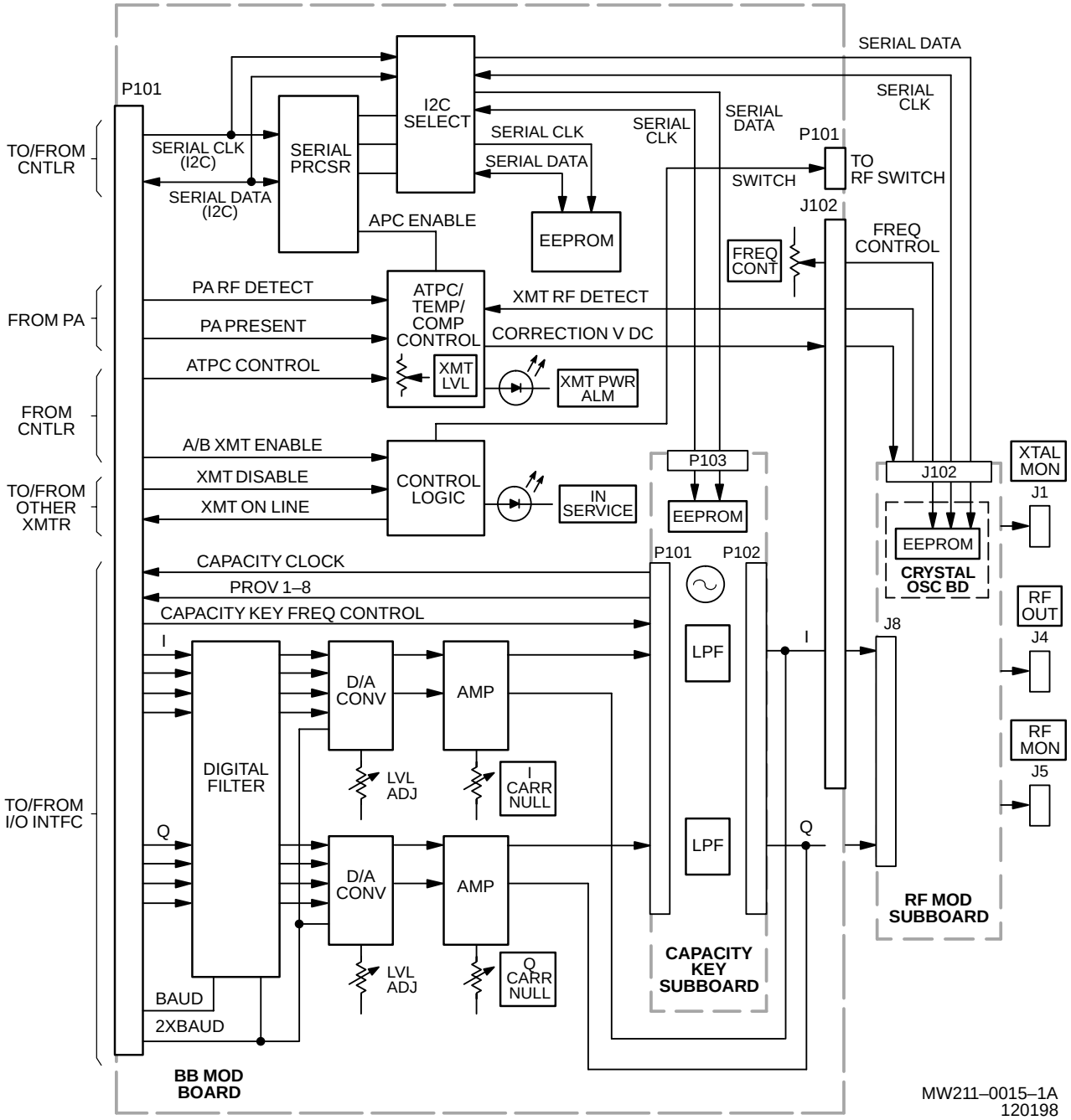

Figure 3-57 UD-35( ) Transmitter Functional Block Diagram

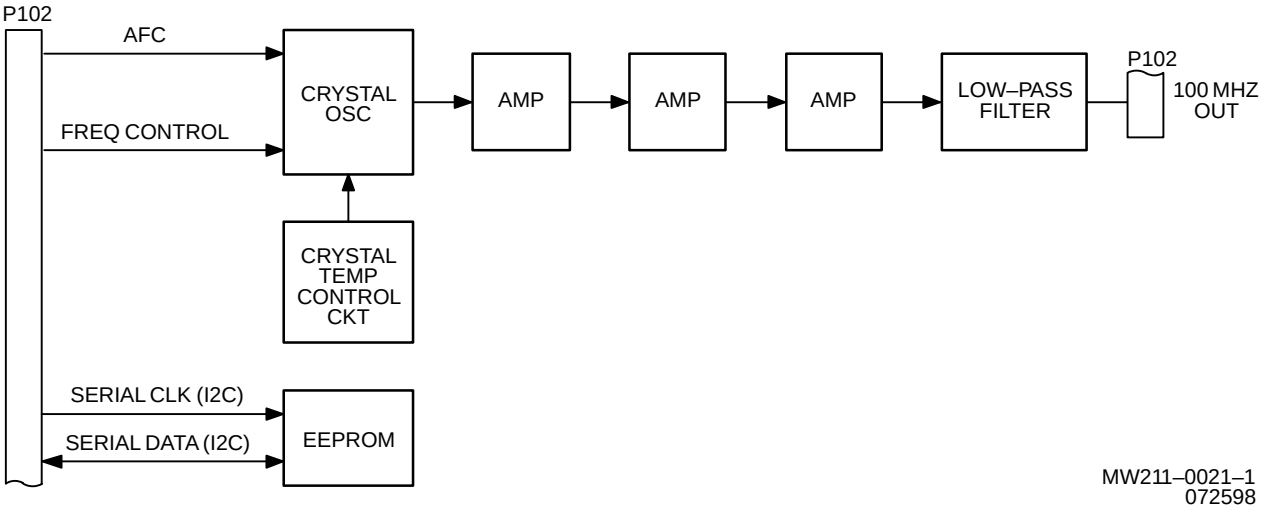

Figure 3-58 UD-35( ) Crystal Oscillator Subboard Functional Block Diagram

3.7.1.7 RF Modulator Subboard

See Figure 3-59. The RF modulator subboard receives the crystal oscillator input and splits the signal to a monitor and a frequency multiplier. The multiplier is usually a low order (2, 3 or 4) and the output is heavily filtered to remove all unwanted harmonics. The signal is multiplied once or twice more to reach a 2GHz frequency, each time filtered to remove unwanted harmonics. This LO signal is split, one side to the I/Q modulator the other to a higher frequency multiplier.

The LO feeding the I/Q modulator is split into two quadrature vectors each driving a double balanced mixer. These mixers up-convert the analog baseband signal to a 2GHz QAM signal. This signal is combined and amplified and fed to a voltage variable attenuator (VVA) where ATPC and temperature compensation level correction occurs.

The LO feeding the higher frequency multiplier is multiplied as required to drive an upconverter mixer to shift the 2GHz QAM signal to the desired RF frequency. The output of the mixer is amplified to a usable RF level so some short distance applications can be satisfied without the optional UD-51( ) Power Amplifier.

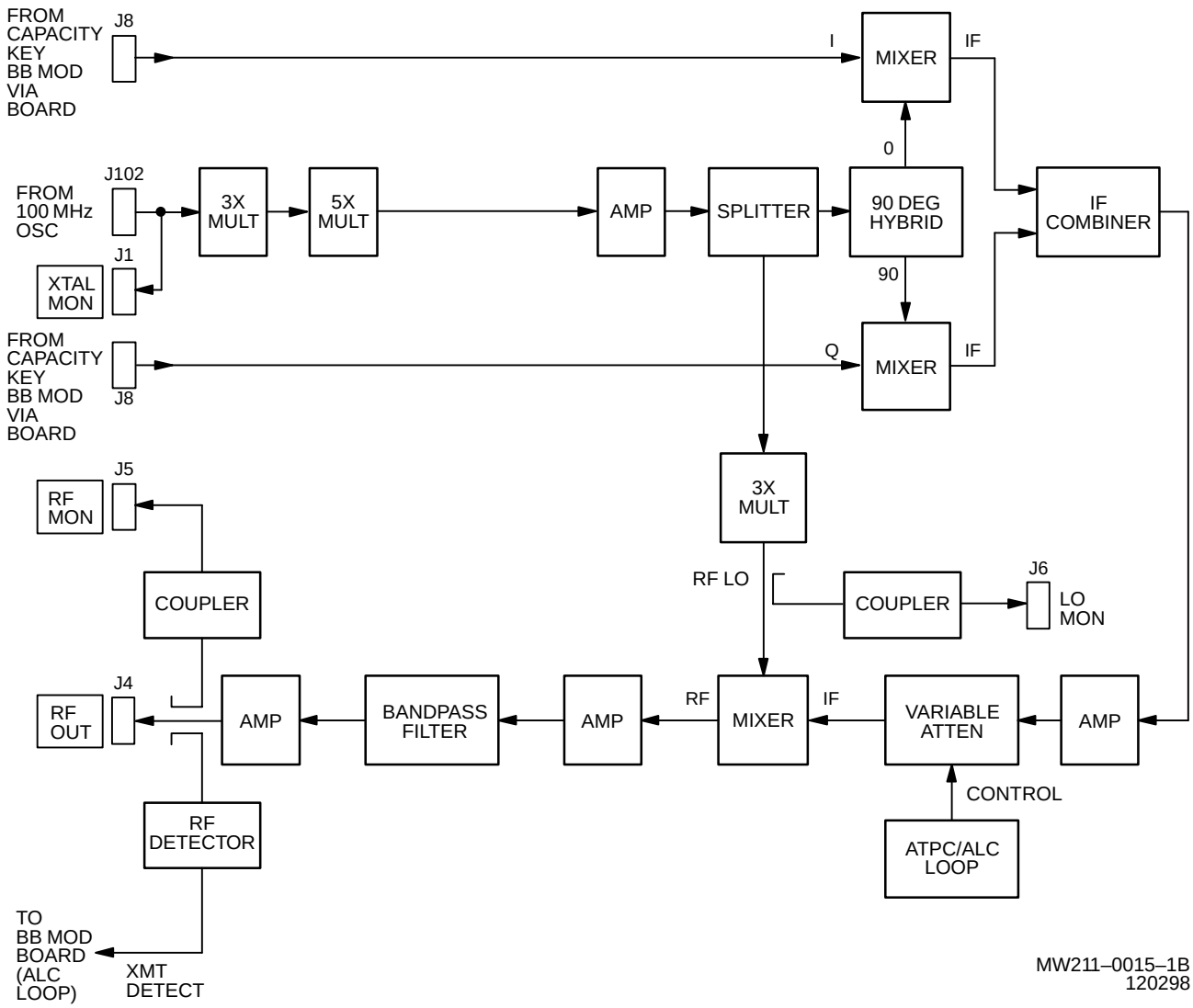

Figure 3-59 UD-35( ) RF Modulator Subboard Functional Block Diagram

3.7.1.7.1 Monitor Circuits

Two crystal oscillator monitor circuits are provided, one at the input to the RF MOD subboard (J1 XTAL MON), that is a direct connection, and the second (J6 LO MON) at the input to the RF/IF mixer, through a coupler. The RF output is monitored via an RF coupler (J5 RF MON). The XTAL MON and RF MON test points are accessible via front panel connectors.

3.7.1.7.2 ALC Loop Output

The RF output is coupled to a detector to produce a dc voltage (XMT RF DETECT) that is applied to the BB MOD board and used in the ALC loop.

3.7.1.8 ALC Loop

The Automatic Level Control (ALC) loop automatically maintains the RF output level of the transmitter. Refer to Automatic Level Control (ALC) under Transmitter Subsystem Functional Description in this section for details.

3.7.1.9 Monitor and Control

The output signal is fed either to the UD-51( ) Power Amplifier (if equipped) or directly to the antenna. The signal is also coupled to a monitor with a nominal level of 0dBm. The signal is coupled to a level detector as well which generates a DC level proportional to the RF output level. This detector voltage is fed back to the controller which uses the signal to determine failure and to correct for gain changes over temperature.

The transmitter sends provisioning data and a frequency control signal to the DX-35( ) I/O Interface module. The provisioning data communicates the type of radio (DS1/E1) and the TCM modulation scheme (32 or 128 TCM) to the I/O interface. The frequency control input is the feedback loop from the phase-lock loop on the I/O interface module to automatically control the crystal oscillator frequency.

3.7.1.9.1 I^2C Bus

EEPROMs to interface the I^2C bus are provided on the BB MOD board, crystal oscillator subboard, and capacity key subboard. The I^2C bus communicates module part number, serial number, and revision history information to the AE-37( ) Controller. The EEPROM on the crystal oscillator subboard also provides oscillator frequency to the controller.

3.7.2 UD-51( ) RF Power Amplifier (Optional)

See Figure 3-60 and Figure 3-61. The RF signal from the UD-35( ) Transmitter is amplified by the UD-51( ) Power Amplifier and routed through a bandpass filter to the antenna. The output of the power amplifier varies depending on the particular unit from +25 dBm to +33 dBm. It is a solid-state linear amplifier with a fixed gain of approximately 21 dB. The actual gain is a function of the radio type and output power.

3.7.2.1 ALC Loop

The Automatic Level Control (ALC) loop automatically maintains the RF output level of the fixed-gain PA by controlling the output level of the XMTR module. Refer to Automatic Level Control (ALC) under Transmitter Subsystem Functional Description in this section for details.

3.7.2.2 Monitor and Control

The power amplifier uses an active bias control stage that allows the unit to go to high bias only during high power operation when increased linearity is required. The RF MON test point is coupled off of the power amplifier output and is nominally 0 dBm. A low power alarm is provided to indicate when the RF output signal power is below a preset level. A detector diode is used to generate a dc voltage that is proportional to output power. This voltage is used to drive alarm circuits and a dc monitor and is also fed back to the XMTR module for ALC. The alarm and dc monitor are independently adjustable.

3.7.2.2.1 I^2C Bus

An EEPROM to interface the I^2C bus is provided on the bias board. The I^2C bus communicates module part number, serial number, and revision history information to the AE-37( ) Controller.

3.7.2.2.2 Temperature Differential Alarm

The power amplifier mounts to the heatsink on the backplane with three screws. If the mounting screws are not installed and tightened properly, after approximately ten minutes, the TEMP ALM LED will light and an alarm output is sent to the controller.

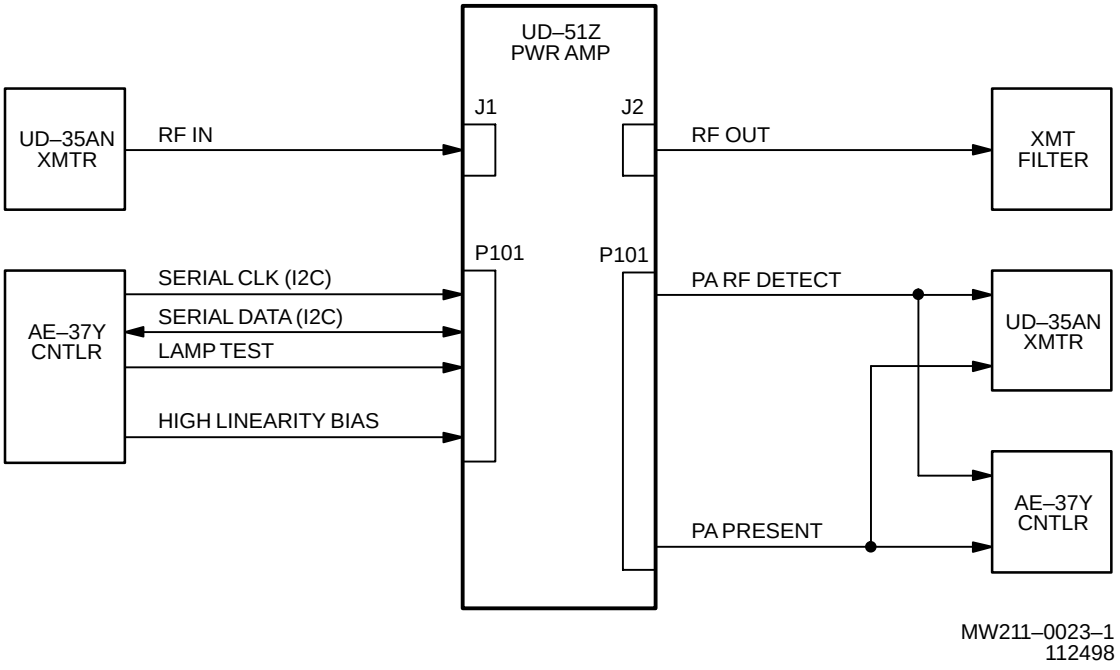

Figure 3-60 UD-51( ) Power Amplifier Interconnect Diagram

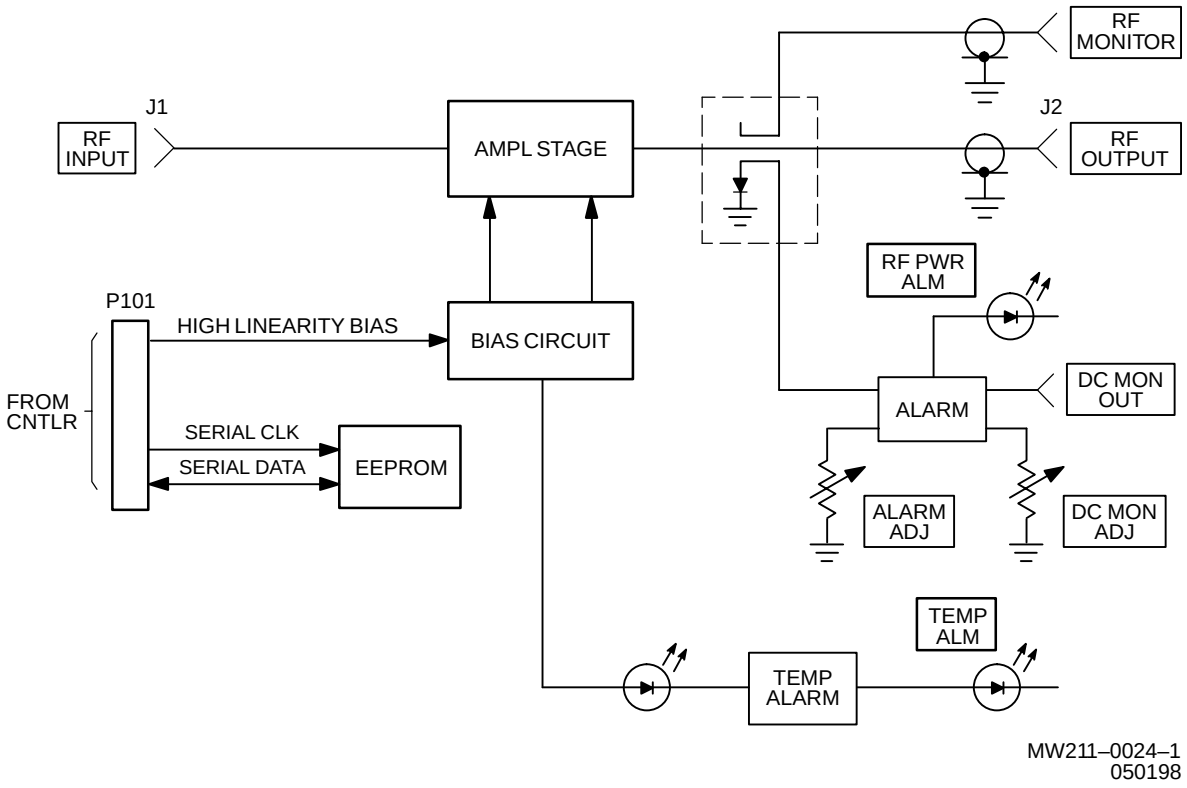

Figure 3-61 UD-51( ) Power Amplifier Functional Block Diagram

3.8 TRANSMIT FILTERS

The transmit filter removes unwanted spurious RF signals and provides a reflection point when stacking several transmitters on a common waveguide run.

3.9 RECEIVER SUBSYSTEM FUNCTIONAL DESCRIPTION

The receiver in the MDR-8000 radio demodulates a radio frequency (RF) signal into digital decoded data. The digital data from the receiver is fed to the input/output interface (I/O interface module) where it is further decoded and demultiplexed.

3.10 RECEIVER SUBSYSTEM MODULES

See Figure 3-62. The MDR-8000 receiver subsystem can have either one of two available receiver modules; the single receiver or the dual receiver.

The following paragraphs describe the operation of the receive subsystems. The single receive subsystem is described in the 3.9.1 series of paragraphs and the dual receive subsystem is described in the 3.9.2 series of paragraphs.

3.10.1 UD-36 ( ) Single Receiver

See Figure 3-62, Figure 3-63, and Figure 3-64. The UD-36( ) single receiver module consists of the main receiver unit, the capacity key to set the units capacity and modulation, and the local oscillator to set the units specific operating frequency

The receiver supports the following modulation formats and capacities:

- 128 TCM for DS1 and OC3/STM-1 applications
- 32 TCM for DS1 and 1-2 DS3 applications
- 64 TCM for 1-3 DS3 applications

The receiver supports a range of RF from 2 GHz to 11GHz.

The single receiver is typically used in the following radio configurations:

- Non-Standby
- Hot-Standby
- Hot-Standby with Space Diversity
- Frequency Diversity

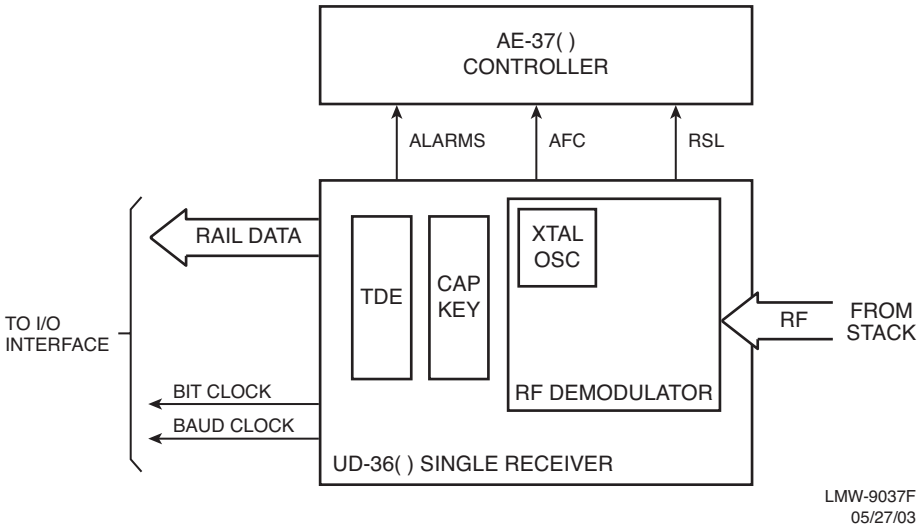

Figure 3-62 Single Receiver Functional Block Diagram

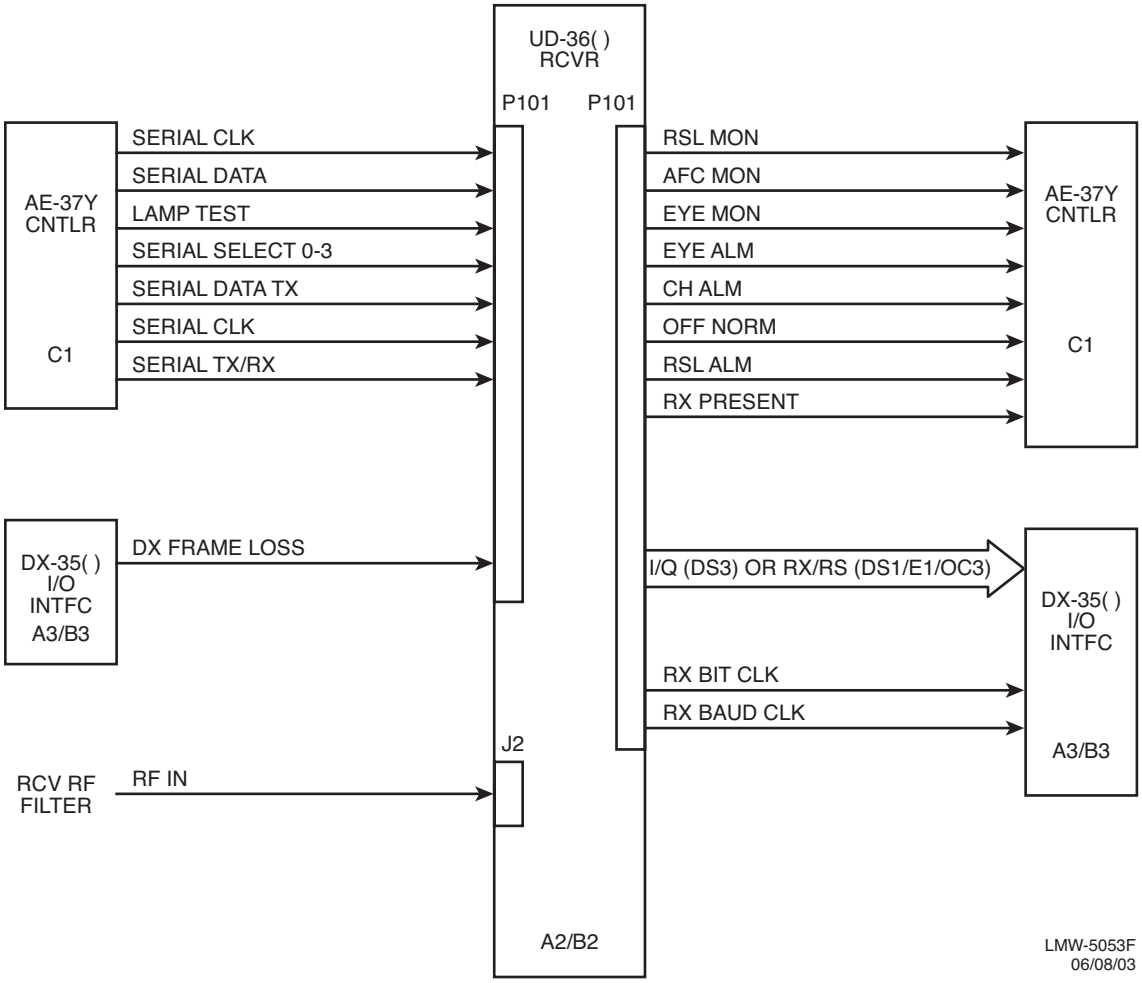

Figure 3-63 UD-36( ) Single Receiver Interconnect Diagram

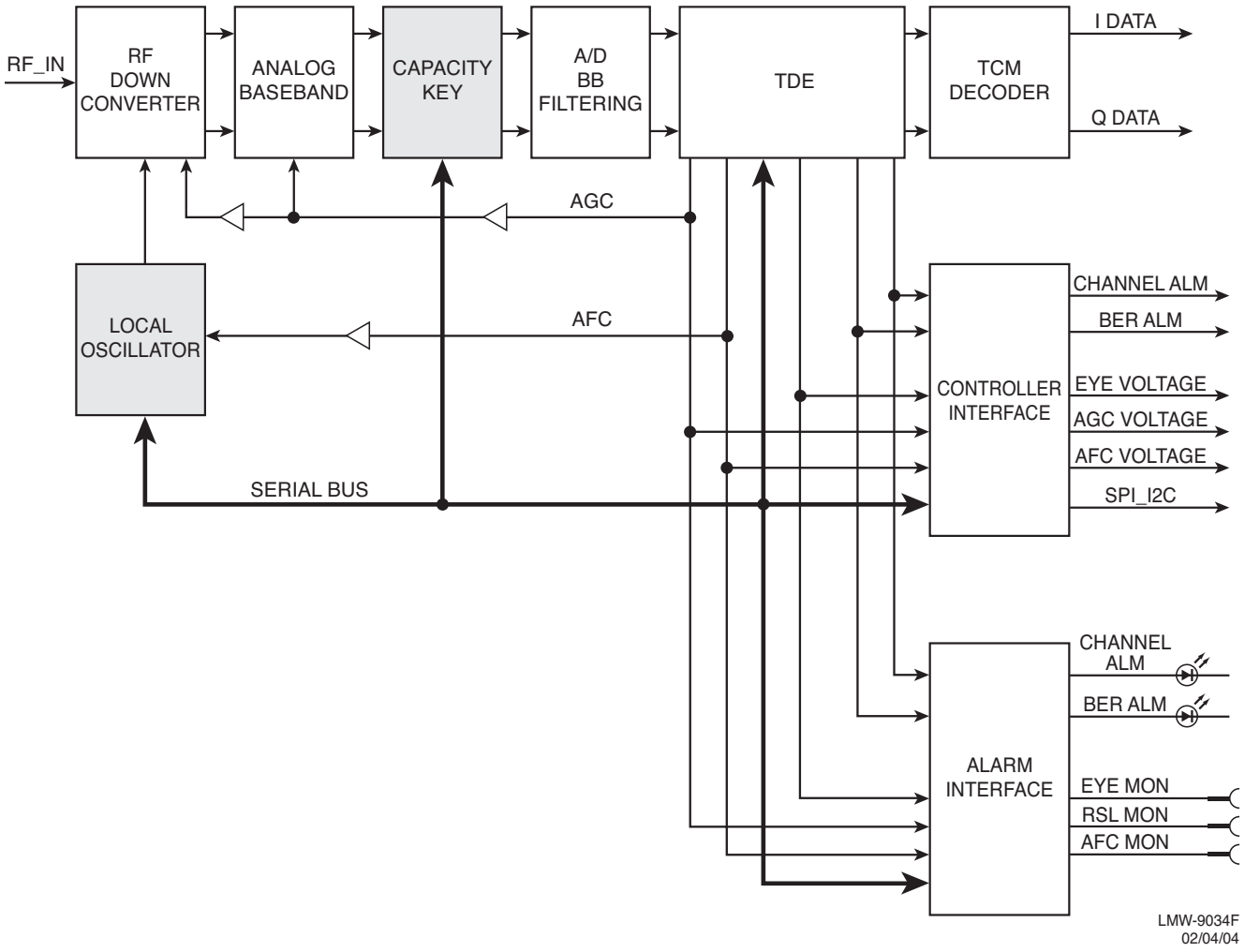

Figure 3-64 Single Receiver Block Diagram

3.10.1.1 External Interfaces

The incoming RF signal is fed to the receiver from the RF filter assembly. An SMA connector on the receiver front panel provides for connection of this interface.

Internal to the cardcage, the receiver feeds its digital outputs to the corresponding I/O interface. The unit communicates alarm status information to the controller. The controller provides the receiver with provisioning and control data. Power for the receiver comes from the corresponding power supply module.

3.10.1.2 Oscillator

The operating frequency of the receiver is set by the oscillator sub-assembly, part of the RF Down Converter. The oscillator sub-assembly contains a VCXO that operates in the 100 MHz to 150 MHz range depending on the desired channel frequency. The output of the oscillator is effectively multiplied up to the desired RF for demodulation in the RF portion of the receiver. The center operating frequency of the VCXO is set by an external potentiometer in earlier versions of the receiver. In later versions the center frequency is automatically controlled from the time domain equalizer (TDE). The receive oscillator is phase locked to the transmitter by the AFC and the associated control loop parameters. The phase detector is in the TDE functional block.

3.10.1.3 RF Demodulator

See Figure 3-65. The RF demodulator, part of the RF Down Converter, converts a suppressed carrier QAM RF signal into I and Q analog baseband signals. The demodulator has a low noise amplifier (LNA) section that sets the noise figure and the overload level of the unit. An AGC circuit is deployed to control the levels through the unit and is set to maximum gain at low signal levels to help achieve a good noise figure. Additionally, at normal to high RSL, the AGC limits the levels through the chain to prevent amplitude distortion. The control signal to the AGC circuit is generated in the TDE.

The down conversion function is performed in the RF demodulator and is generally done in two steps. The RF is first converted to an IF and then further demodulated into I and Q analog baseband signals by using a quadrature demodulator. The local oscillator (LO) used to perform the down conversion and demodulation is derived from the oscillator sub-assembly. The CW signal from the oscillator is multiplied appropriately and fed to the down conversion and demodulation circuits. The multiplication factor varies with RF bands. The oscillator generates a signal in the 100 MHz - 150 MHz range. The RF input signal to be demodulated is in the 2 GHz - 11 GHz range.

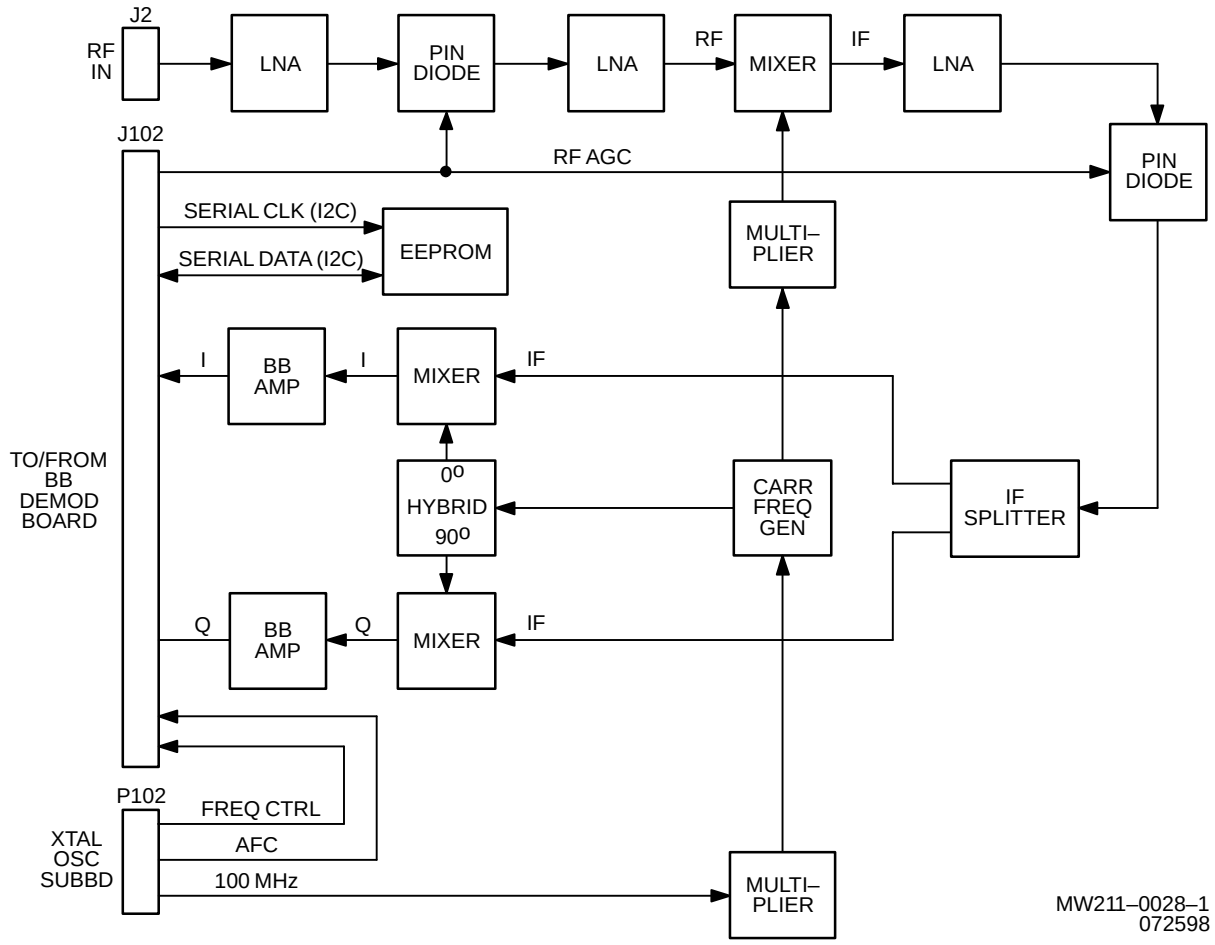

Figure 3-65 UD-36( ) Receiver, RF DEMOD Subboard Functional Block Diagram

3.10.1.4 Analog Baseband

The analog baseband section provides additional baseband gain and baseband AGC. The section is designed to maintain a constant baseband level into the A/D converter. The gain remains constant throughout the dynamic range of the receiver from threshold to overload. Independent gain stages are used for I and Q baseband.

3.10.1.5 Capacity Key

The capacity key, a field replaceable sub-unit, is used to configure the receiver for the proper modulation and baud rate operation. Configuration information resides on the capacity key and is read by the receiver, controller, and I/O interface to properly configure the receiver chain. The capacity key also contains the baud clocks and the anti-aliasing filters for the I and Q baseband signals. The anti-aliasing filter is used to prevent the distortion at the sampling frequency from folding back in-band.

3.10.1.6 Digital Baseband

The digital baseband section contains the A/D converters for the I and Q channels along with the digital pulse shaping filter. This function accepts the filtered analog baseband signal and generates the post equalized digital I and Q signals that are fed to the TDE. The digital filter is a 24-tap filter with a roll-off factor of 0.2.

3.10.1.7 TDE

The Time Domain Equalizer (TDE) is a countermeasure primarily for multipath impairments. The TDE consists of a 11-tap feed forward section and a 11-tap decision feedback section with a single center tap. The TDE uses least mean squared (LMS) and Zero forcing algorithms for tap adaptation. The TDE output symbols are also used in the decision directed recovery loops for AGC, AFC, and clock recovery.

3.10.1.8 TCM Decoder

The Trellis Coded Modulation (TCM) decoder for OC3/STM-1 uses the following codes:

Inner Code

4d Trellis rate 2/3 Convolutional Code providing 4.66 dB of coding gain over uncoded 128 QAM. Modulation used is 128 signal points with channel information density of 6.54 bits per channel symbol.

Outer Code

4-Way Byte Interleaved Reed Solomon Code with 856 bytes block size with 840 bytes of information. This is expected to provide between 0.5 and 1 dB of coding gain. An additional level of bit interleaving is employed outside the Reed Solomon code to distribute burst errors (105 max). Bit interleaving is performed in order to distribute errors in a manner in which every other symbol will have no more than 1 bit error.

3.10.1.9 Controller Interface

Communication to the system processor is over the SPI bus. The system processor is the master device in all cases and initiates all transfers. The controller interface function is used to download provisioning and control details from the radio controller to various devices on the receiver and also to send alarm and status information from the receiver to the radio controller. The SPI port is also used to set the adaptation parameters of the TDE during initialization.

3.10.1.10 Monitoring

Alarm and status information from the receiver is fed to the controller for reporting to the USI and the network management systems. The information is also brought to the receiver's front panel to test points and LEDs for local access. The LEDs indicate the Channel Alarm and the Eye Closure Alarm status and the On-Line condition.

A Channel Alarm is generated if the incoming signal is degraded by noise or other impairments to the point that clock or carrier recovery cannot be achieved. When the Channel Alarm is ON the LED indicator goes to red. During this time, receiver performance typically exceeds 10^{-6} BER. Under normal conditions the Channel Alarm indicator should be off.

The Eye Closure Alarm threshold is provisionable from 10^{-5} to 10^{-8} BER. An Eye Closure Alarm is generated when the receive signal degrades to these thresholds; the LED indicator goes to red. Under normal conditions the Eye Closure Alarm indicator should be off.

The On-Line condition indicator should be green when the receiver is in service and red when out of service.

3.10.2 UD-36 ( ) Dual Receiver

See Figure 3-66, and Figure 3-67. The UD-36( ) dual receiver module consists of the main receiver unit, the capacity key to set the units capacity and modulation, and the local oscillator to set the units specific operating frequency. This module also contains a diversity channel that is functionally the same as the main channel. The two channels (main and diversity) are on the same PC board but physically on opposite sides. The diversity channel has its own independent capacity key and oscillator to set its mode of operation. The outputs of the two channels are fed to the switching circuit which monitors the condition of the channels and selects the better signal for transmission to the I/O. The switching circuit is physically located on the main channel side of the PC board.

The receiver supports 128 TCM for OC3/STM-1 applications only and supports an RF range from 6 GHz to 8 GHz. The dual receiver is used where Quad Diversity operation is needed but can also be used to provide space diversity protection in non-standby systems.

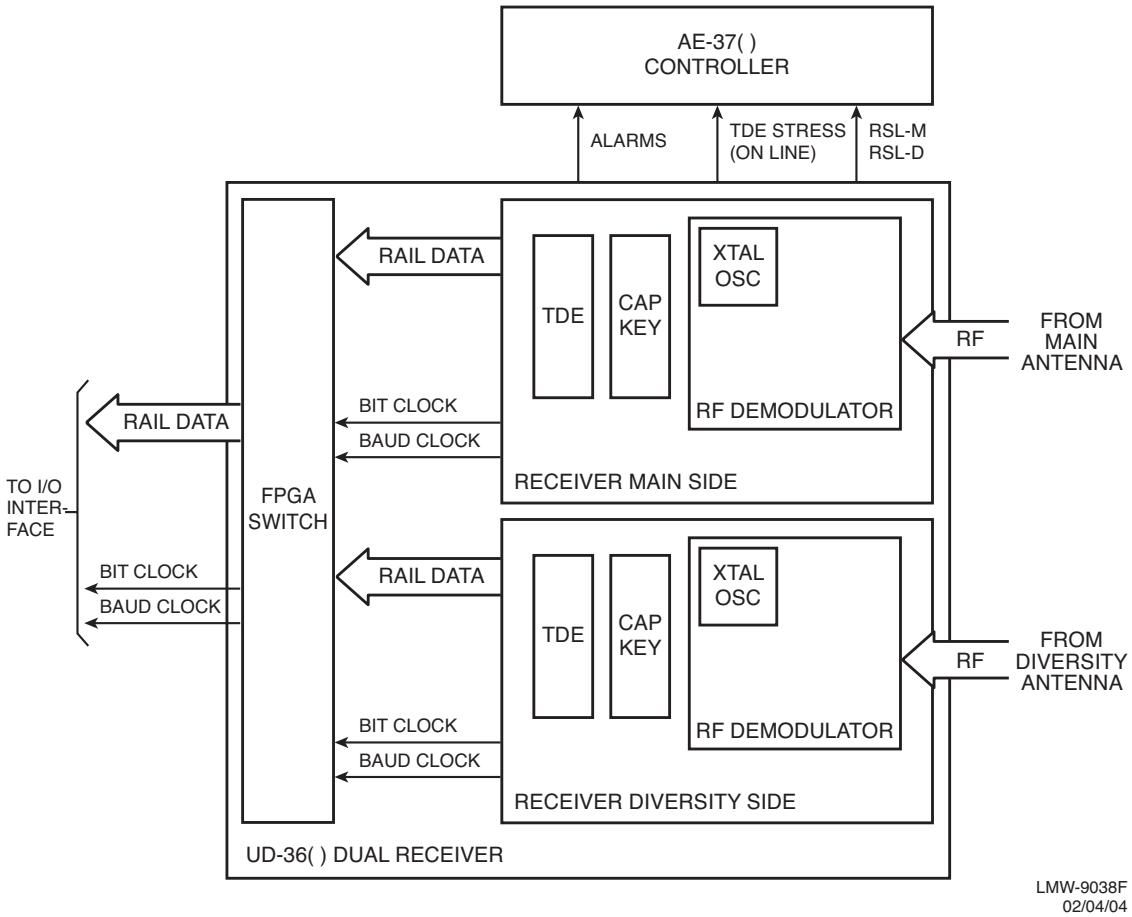

Figure 3-66 Dual Receiver Functional Block Diagram

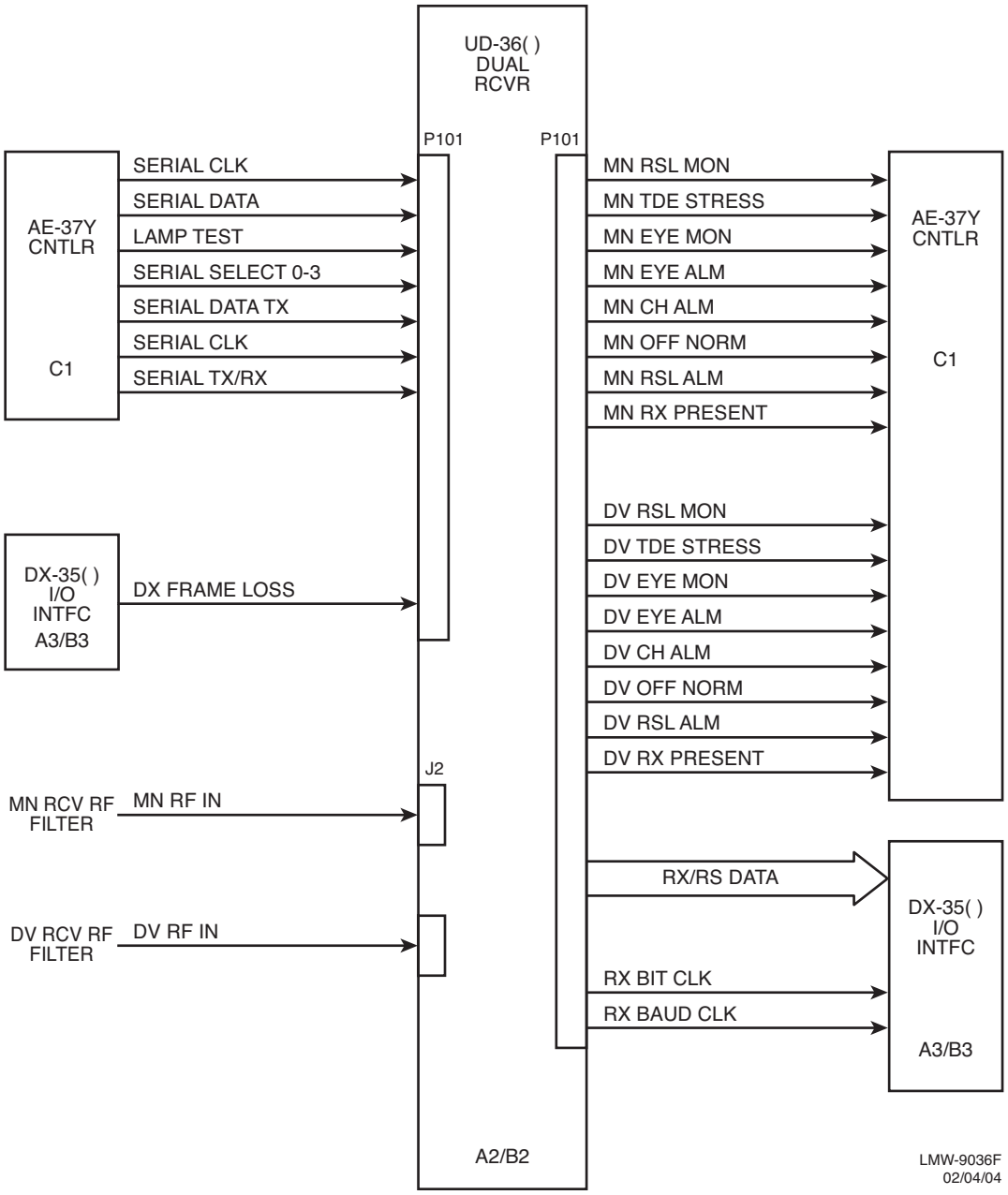

Figure 3-67 Dual Receiver Interconnect Diagram

3.10.2.1 External Interfaces

The dual receiver has two RF input signals; one for the main channel and one for the diversity channel. Internal to the card cage the unit feeds its digital outputs to the corresponding I/O interface module. The unit communicates alarm status information to the controller which provides the receiver with provisioning and control data. Power for the dual receiver comes from the corresponding power supply module.

3.10.2.2 Oscillator

The oscillators of the dual receiver are physically and functionally identical to the oscillator used for the single receiver. A separate oscillator is provided for the main channel and the diversity channel. The main and diversity oscillators typically operate at the same frequency.

3.10.2.3 Capacity Key

The capacity key for the dual receiver is the same as that used for the single receiver. Two capacity keys are used in the dual receiver; one for the main channel and one for the diversity channel. The capacity keys used in each of these channels are typically identical.

3.10.2.4 Main Channel

The main channel is functionally the same as the single receiver. It is dedicated to processing the RF input signal from the main antenna and generating the digital data status and information that are fed to the switching circuit.

3.10.2.5 Diversity Channel

The diversity channel is functionally the same as the single receiver. It is dedicated to processing the RF input signal from the diversity antenna and generating the digital data status and information that are fed to the switching circuit.

3.10.2.6 Switching

The switching circuit is physically located on the main channel side of the receiver PC board. Data and status information from both the main and diversity channels are fed to the switching circuit. This circuit performs two major functions; data alignment and switching.

Data alignment is required for errorless switching between the two channels. The radio frame markers are found on each channel and are aligned by using data buffers. The alignment circuit can tolerate a maximum of 300 nsec of delay offset.

Status information is fed to the switching circuit from the TDE. The TDE processes the status information from both sides and selects the data from the better channel for distribution to the I/O interface unit. The following parameters are used to make the switching decision:

- Channel Fail
- Frame Alarm
- Eye Closure Alarm
- AGC Alarm
- TCM Errors
- TDE Stress

The switching circuit constantly evaluates these parameters and selects the channel that has the best performance. The switching parameters from both the main and diversity channels are also fed to the controller. In protected systems the controller evaluates the status of the online channel to determine if a switch between the “A” and “B” dual receiver is required.

3.10.2.7 Monitoring

Alarms, indicators, and test points are the same as for the single receiver, except that the dual receiver has two sets of each. For details, refer to the single receiver section.

3.11 MONITOR AND CONTROL SUBSYSTEM FUNCTIONAL DESCRIPTION

3.11.1 Protection Switching

The radio can be configured for full 1:1 protection of the power supply, transmitter, power amplifier, I/O interface, and receiver modules. The AE-37( ) Controller constantly monitors the modules for fault conditions and controls the switching of protected subsystems.

3.11.2 Switchover Priority

Upon an alarm condition, a switchover to the other transmitter or receiver is based upon priority. Initially, both power up to the A-side; then switchover is determined according to the following hierarchy:

RECEIVER		
	Override (initiated from controller)	Highest priority
	Alarms	
	Manual switch (initiated from USI laptop computer or from controller front panel)	Lowest priority
TRANSMITTER	Override (initiated from controller)	Highest priority
	CLA Switch	
	Alarms	
I/O	Manual switch (initiated from USI laptop computer or controller)	Lowest priority
	Override (initiated from controller)	Highest priority
	Alarms	
	CLA Switch Manual switch (initiated from USI laptop computer or controller).	Lowest priority

Parallel or serial receive/transmit alarms are activated by any module. Manual switching is from the USI laptop computer local or far-end controls menu. Manual switchover cannot occur from an alarm-free condition to the other side with an alarm. Alarms causing switchover are as follows:

RECEIVER ALARMS	TRANSMITTER ALARMS	I/O ALARMS
No report	No report	No report
Channel fail	PA power	DS1/E1 clock recovery
Radio frame	Common/loss	Input signal loss
Eye closure		Buffer spill
Radio errors		

3.11.2.1 Low Speed Protection

Low speed (I/O) protection for the line interface array hardware is provided by redundant I/O Interface modules. The on-line cards provide X/Y rail data to both cards. The controller will select the set of modules with the fewest alarms.

Any of the following conditions constitutes an I/O failure in the multiplex direction.

- Loss of MUX Signal – Excessive zeroes have been detected.
- MX Spill – Elastic buffer overflow.
- MUX Line Code Error – B8ZS or AMI encoding error detected.
- Loss of Clock Recovery Sync – Clock cannot be recovered from incoming data.

Any of the following conditions constitutes an I/O failure in the demultiplex direction.

- DX Spill – Elastic buffer overflow.
- Loss of Smooth clock – A smooth clock cannot be recovered from incoming data.
- Driver Failure – The on-line driver signals do not match the output data.

3.11.2.2 High-Speed Protection

The high-speed portion of the system consists of the I/O interface, the receiver and transmitter modules. One-for-one protection of the high-speed modules is available for hot-standby, space diversity. or frequency diversity applications by adding a second set of modules.

3.11.3 Transmit Protection

In the transmit path, each I/O Interface generates digital baseband signals from the shared X/Y rail data. The baseband output of each I/O interface module is fed to the corresponding A and B transmitter and power amplifiers. In hot-standby transmitters, the RF data from each power amplifier is fed to the RF switch where either A or B data is selected for transmission. The controller selects which transmitter is on-line based on PA and common loss alarm indications. The relay switch control is provided by the B side Transmitter unit so that the switch state is maintained when the controller is removed from the shelf. In frequency diversity transmitters, both PA outputs are on-line at all times.

3.11.4 Common Loss Alarm (CLA)

In hot-standby transmitter applications, the far-end receiver is used as a check for silent failures in the transmitter. The far-end controller sends periodic status messages to the transmit end that contain information about which receiver is on line and its status. If the on-line receiver has been out of frame continuously for 30 seconds, a transmit switch will occur. If the receiver frame loss clears within 5 seconds of the switch, a common loss alarm will be latched for the transmitter that was previously on-line. This alarm will only be cleared by a controller reset, pressing the LAMPTEST switch on the front of the controller, or acknowledging the alarm from the local status screen of the USI computer.

If the receive frame alarm does not clear, the problem is assumed to not be caused by the transmitter. Switching will continue every 30 seconds until a receiver recovers but a common loss alarm will not be latched. After every fifth transmit switch, the I/O will be switched.

3.11.5 Receive Path Protection

Errorless receive switching is provided for protected applications. This is accomplished in the I/O interface modules by aligning the phase of the X/Y rail frames between the A and B-side modules. An internal digital delay line is used to adjust the absolute delay of off-line receiver to match the on-line receiver. When a switch command is received from the controller, the X/Y clock and data drivers from the off-line receiver are turned on, causing the on-line drivers to turn off (make before break). The switch is timed to occur when the clock and data signals are stable so that no glitches are created. The X/Y rail data from the on-line receiver is fed to both sets of demultiplex circuits.

The controller monitors each receiver for failures or degradations and selects the best one. The following criteria are used (in order of priority):

- I/O Prov – Loss of communication to I/O Interface or configuration mismatch.
- Radio frame – The I/O Interface array has lost radio frame.
- CRC error rate – The radio CRC (parity) rate exceeds $1x10^{-4}$.
- AGC – One side below and other above AGC (approx -65 dBm RSL). Switching can be disabled by provisioning.
- Eye Closure – user provisionable: 10^{-5}, 10^{-6}, 10^{-7}, 10^{-8}, or disabled.

3.11.6 DS1 Radio Receiver DADE

In order to provide errorless receiver switching, the receive A and B frames must be aligned. This is done automatically by the off-line receiver. The off-line receiver compares the frame sync from the on-line receiver with its own internal frame sync. The delay of an internal digital delay line is adjusted so that the sync phases match. The delay line has 12 step positions, each step adding a delay of one period of the capacity key oscillator. The delay position of the on-line receiver is set at a fixed position by the controller. The controller adjusts this position so that the off-line receiver is not at the end of its delay line. A DADE alarm is generated if the off-line receiver is at either end of the delay line.

The system differential delay may be caused by differences in antenna waveguide lengths. If this difference is excessive, the DADE circuits may run out of range.

Variations in counter phase relationships in the X/Y-I/Q MUX and DEMUX circuits may also create differential delay or cause the delay to vary when the receiver lock is disturbed. These variations are part of normal operation and do not affect the errorless switching performance.

3.11.7 Manual Switching

Manual switches are provided on the AE-37( ) Controller to manually switch the transmitters, receivers, and I/O interface drivers. Under normal operation, the manual switches will be in the AUTO position, which allows the switching decisions to be made by the controller based on alarm information. In the transmit and receive directions, both data paths have equal priority. This means that if either the A or B path is selected for transmission by the controller, it will then remain selected until a path failure occurs. If the manual switches are set to A or B, the controller will switch to the selected side if that side does not have a higher level of active alarms. By simultaneously pressing the OVRD switch, the manual requests are latched and switching will occur regardless of the alarm status. A switch will never be made to a non-equipped or non-powered side.

3.11.8 Automatic Transmit Power Control (ATPC)

Automatic Transmit Power Control (ATPC) is standard in the MDR-8000 radio, but a provisioning option allows the user to disable the function. When enabled, the user can select between two modes of operation: ATPC for normal ATPC functions or ATPC T/O for ATPC with timeout. The ATPC function allows the radio XMTR to operate at a level lower than maximum power output level during normal operating periods. A level detector in the associated RCVR at the far end monitors RSL and when a failure is detected (includes fading) the RCVR commands the associated XMTR to go to high power. Specific function details depend on the mode of operation provisioned and/or the failure as follows:

Provisioning: ATPC or ATPC T/O

- Normal Operation: ATPC tracks RCVR with highest RSL. XMTR output is 10 dB down from maximum power out. Normally the A-side has the highest RSL (B-side RSL is 10 dB down from A-side RSL).
- If one RCVR fails: XMTR goes to high power for 10 seconds, once every minute, until RCVR is restored.
- If both RCVRs fail: XMTR goes to high power and stays there (until RCVRs are restored).

Provisioning : ATPC T/O (only)

- If Command path fails: XMTR goes to high power for five minutes and then returns to low power. Then, if command path has not been restored, once every hour the XMTR goes high for 10 seconds and then returns to low power.

3.11.9 ALC Loop

The Automatic Level Control (ALC) loop automatically maintains the RF output level of the fixed-gain PA by controlling the output level of the XMTR module. Refer to Automatic Level Control (ALC) under Transmitter Subsystem Functional Description in this section for details.

3.11.10 Provisioning

- The AE-37( ) Controller uses a nonvolatile EEPROM to store configuration information for the system. This information is displayed and modified in the provisioning screen of the USI computer.

- The controller periodically examines the status from each module to ensure concurrence with the information stored in the EEPROM. If a mismatch is found, the OFF NORMAL alarm is activated.

3.11.11 Remote Inventory

See Figure 3-68. The 256 X 8 bit EEPROM stores inventory information that is read by the AE-37Y Controller over the I^2C bus when the remote inventory function on the USI is initiated. Inventory data, including part number, software revision, serial number, and hardware revision are stored in the non-volatile memory on each equipped module.

There is an I^2C bus for the A-side modules (I^2C A), B-side modules (I^2C B), and ancillary modules (I^2C C). Ancillary modules include the relay interface and controller modules.

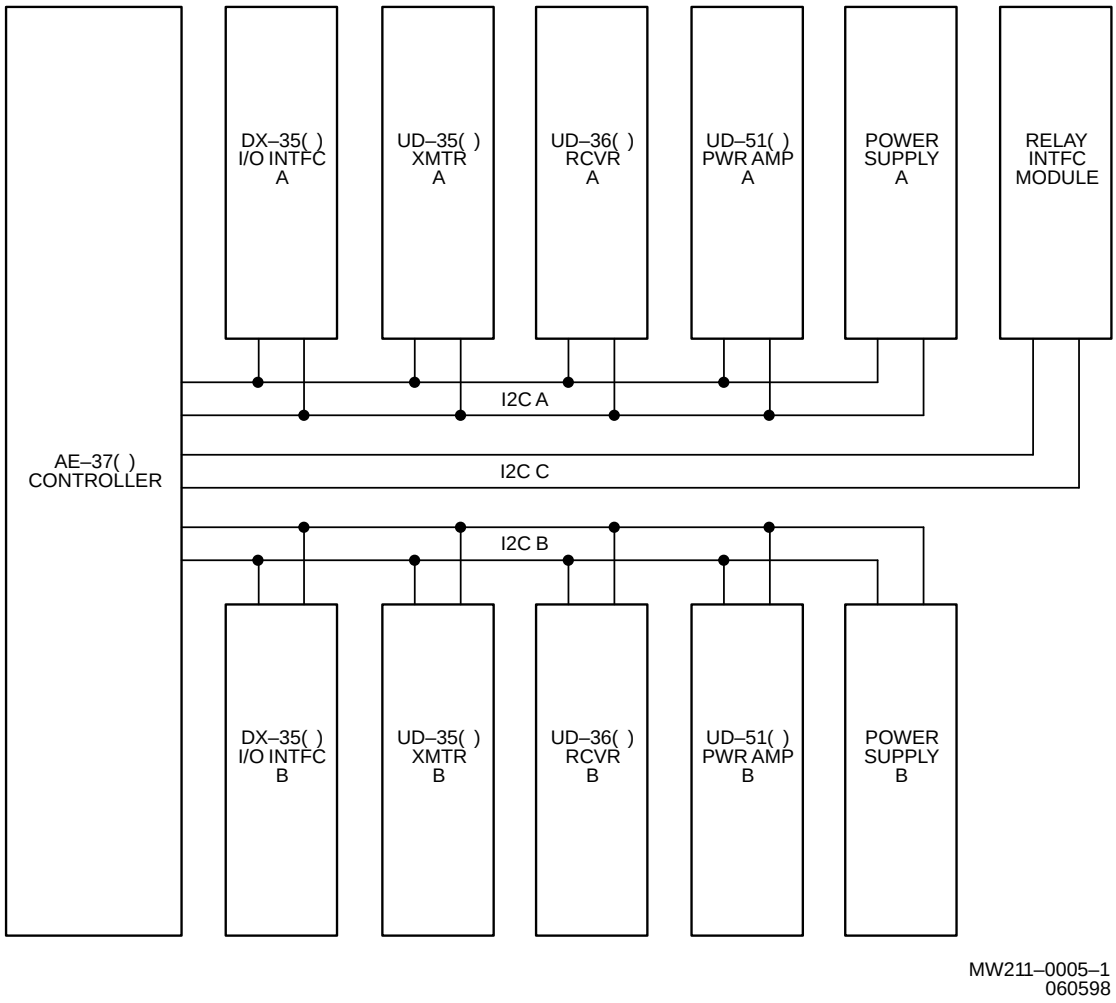

Figure 3-68 I^2C Communications Function Block Diagram

3.12 TMN SYSTEM FUNCTIONAL DESCRIPTION

See Figure 3-69 for a simplified block diagram showing Telecommunications Management Network (TMN) overhead access in the MDR-8000. Simple Network Management Protocol (SNMP) data for transport is transferred to the radio controller via the parallel bus on the backplane. The radio controller inserts the data into the provisioned service channel. The Service Channel controller inserts the data into the provisioned service channel. The Service Channel 1 SC1) output of the controller at 256 kb/s (four 64 kb/s channels combined) is applied to the XMT baseband (BB) circuits on the I/O interface module and output to the radio XMTR. SC1 data from the RCV BB circuits on the I/O interface are applied to the TMN interface module where the SNMP data is extracted and applied to the radio controller via the parallel bus.

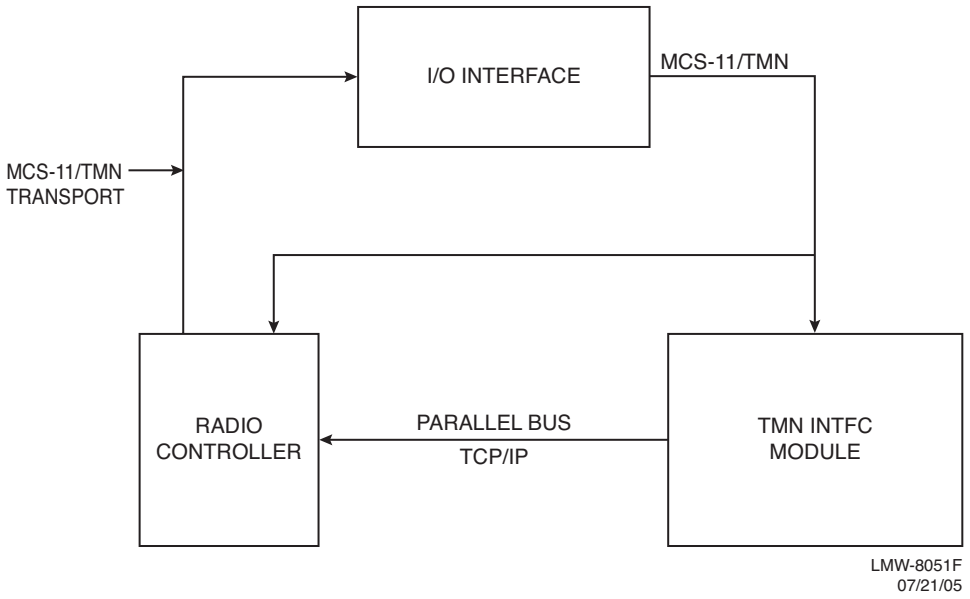

Figure 3-69 TMN Overhead Access Simplified Functional Block Diagram

3.12.1 Radio Terminal Service Channel Signal Flow

3.12.1.1 West SC

See Figure 3-70. At a terminal, the west service channel interface at the I/O interface module consists of the WEST SC RCV DT and WEST SC CLKS (WEST SC 256K CLK, WEST SC 64K CLK, WEST SC 16K SYNC, WEST 8K SYNC, and WEST SC 2K SYNC) outputs. The WEST SC XMT DT output is a single 256 kb/s multiplex signal that contains four 64 kb/s channels. In the I/O interface, the service channel data (WEST SC RCV DT) is removed from the radio frame overhead and is sent to the service channel muldem in the controller module. The WEST SC RCV DT is clocked into the controller by the WEST SC CLOCKS.

3.12.1.2 East SC

At a terminal, the east service channel interface at the I/O interface consists of the EAST SC XMT DT input and EAST SC CLKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST SC 8K SYNC, and EAST SC 2K SYNC) outputs. The EAST SC XMT DT input consists of fur 64 kb/s channels multiplexed into a single 256 kb/s signal. Overhead MUX circuitry in the I/O interface receives local insert-service channel data (EAST SC XMT DT) from the service channel muldem in the controller module. The EAST SC XMT DT is clocked into the controller using the EAST SC CLOCKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST SC 8K SYNC, and EAST SC 2K SYNC). In the I/O interface, the service channel insert data (EAST SC XMT DT) is inserted into the radio frame overhead.

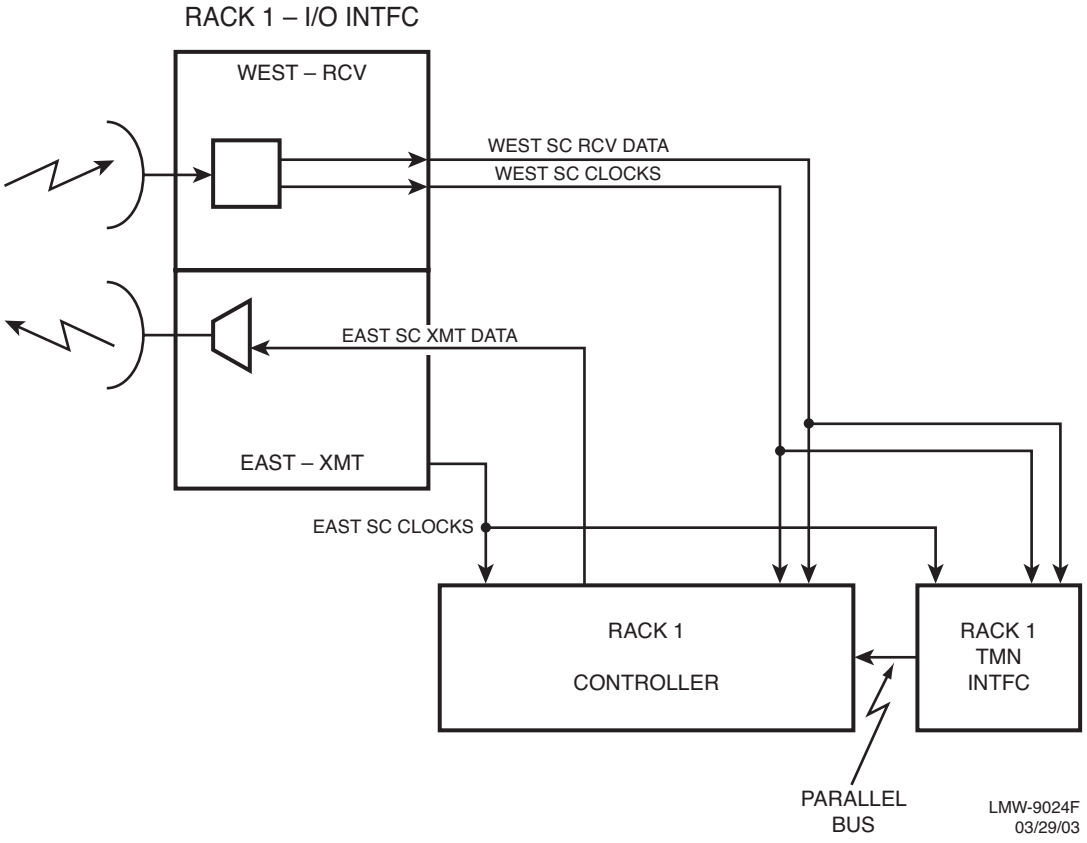

Figure 3-70 Terminal Service Channel Signal Flow

3.12.2 Radio Repeater Service Channel Signal Flow

3.12.2.1 West SC

See Figure 3-71. The service channel interface rack 1 I/O interface consists of the WEST SC XMT DATA and WEST SC XMT OFF HOOK inputs and WEST SC CLKS (WEST SC 256K CLK and WEST SC 2K SYNC) outputs. The WEST SC XMT DATA input consists of four 64 kb/s channels multiplexed into a single 256 kb/s signal.

The rack 1 controller module and TMN interface module always receive WEST SC RCV DATA and WEST SC RCV CLOCKS, regardless of the state of the WEST SC OFF HOOK SIGNAL from the controller. The WEST SC OFF HOOK signal from the controller controls only the WEST SC RCV DATA output of the MUX to the repeater port.

When WEST SC XMT OFF HOOK is low, (no off hook from rack 1 controller) data received over the RF path (WEST SC RCV DATA) is passed through the MUX and put on the repeater cable to rack 2. When WEST SC SMT OFF HOOK is high (off hook), WEST SC RCV DATA is clocked into the rack 1 controller by the WEST SC CLKS. The rack 1 controller multiplexes the WEST SC RCV DATA with local insert-data and the combined signal is passed through the MUX and put on the repeater cable to rack 2.

3.12.2.2 East SC

The service channel interface in rack 2 I/O interface consists of the EAST SC XMT DATA and EAST SC XMT OFF HOOK inputs and EAST SC CLKS (EAST SC 256K CLK, EAST SC 64K CLK, EAST SC 16K SYNC, EAST SC 8K SYNC, and EAST C 2K SYNC) outputs, and rack 1 data input via the RPTR cable. Each data (DT) input and output consists of four 64 kb/s channels multiplexed into a single 256 kb/s signal.

The rack 1 controller module and TMN interface module always receive EAST SC RCV DATA and EAST SC RCV CLOCKS, regardless of the state of the EAST SC OFF HOOK signal from the controller. The EAST SC OFF HOOK signal from the controller controls only the EAST SC RCV DATA output of the MUX to the RF port.

When EAST SC XMT OH is low (no off hook from rack 2 controller) data received over the repeater cable by the frame in/frame out (FIFO) circuit (EAST SC RCV DT) is passed through the MUX and inserted into the radio frame overhead. When EAST SC XMT OH is high (off hook), EAST SC RCV DT is clocked into the rack 2 controller by the EAST SC CLKS. The rack 2 controller multiplexes the EAST SC RCV DT with local insert-data and the combined signal (EAST SC XMT DT) is passed through the MUX and inserted into the radio frame overhead.

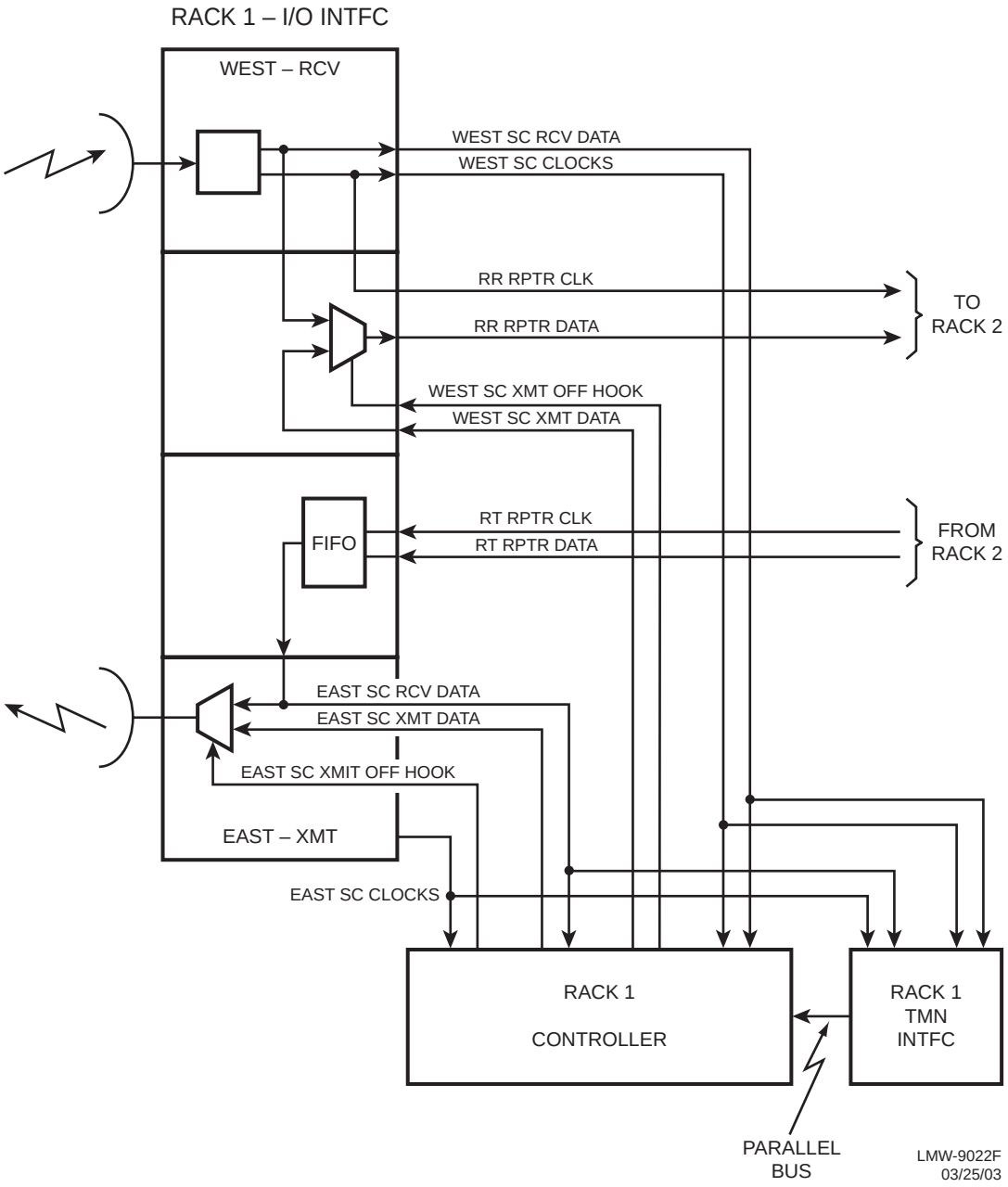

Figure 3-71 Repeater Service Channel Signal Flow

3.12.2.3 Operation

The SC XMT is always off hook and there is no direct through path in the radio. Packets are either buffered through the TMN interface or dropped and reinserted using a forwarding buffer in the radio controller.

See Figure 3-72 and Figure 3-73. The TMN Interface monitors the Service Channel for packets. It also sends packets to the Radio Controller to be inserted into the Service Channel via the TMN_E and TMN_W ports.

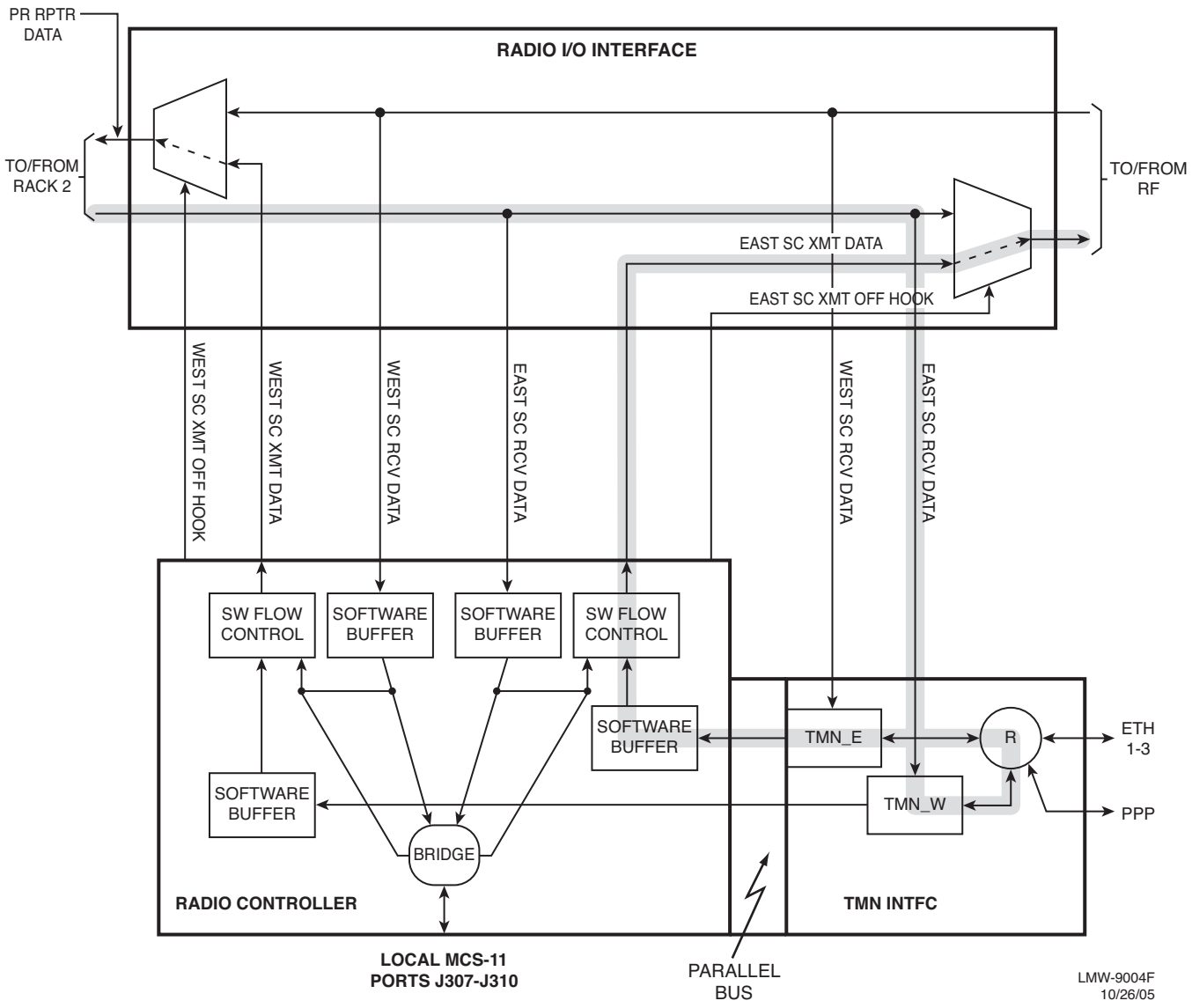

Figure 3-72 East Transport Message Flow

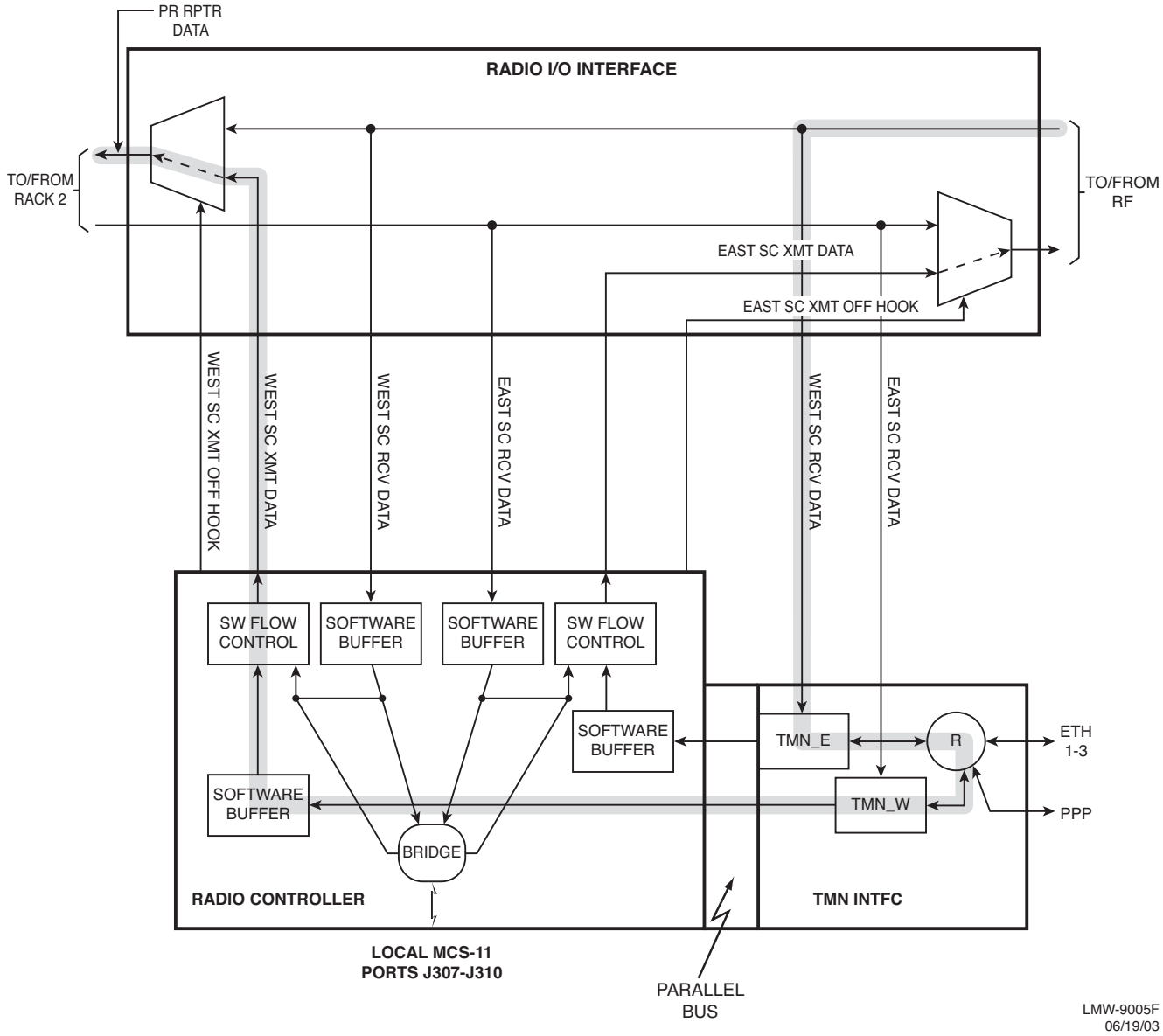

Figure 3-73 West Transport Message Flow

3.12.3 Packet Transport

See Figure 3-74 for a typical framing structure. The TMN Service Channel is operated in Full Duplex mode. It transports MCS-11 packets and Ethernet IP packets wrapped in an HDLC frame.

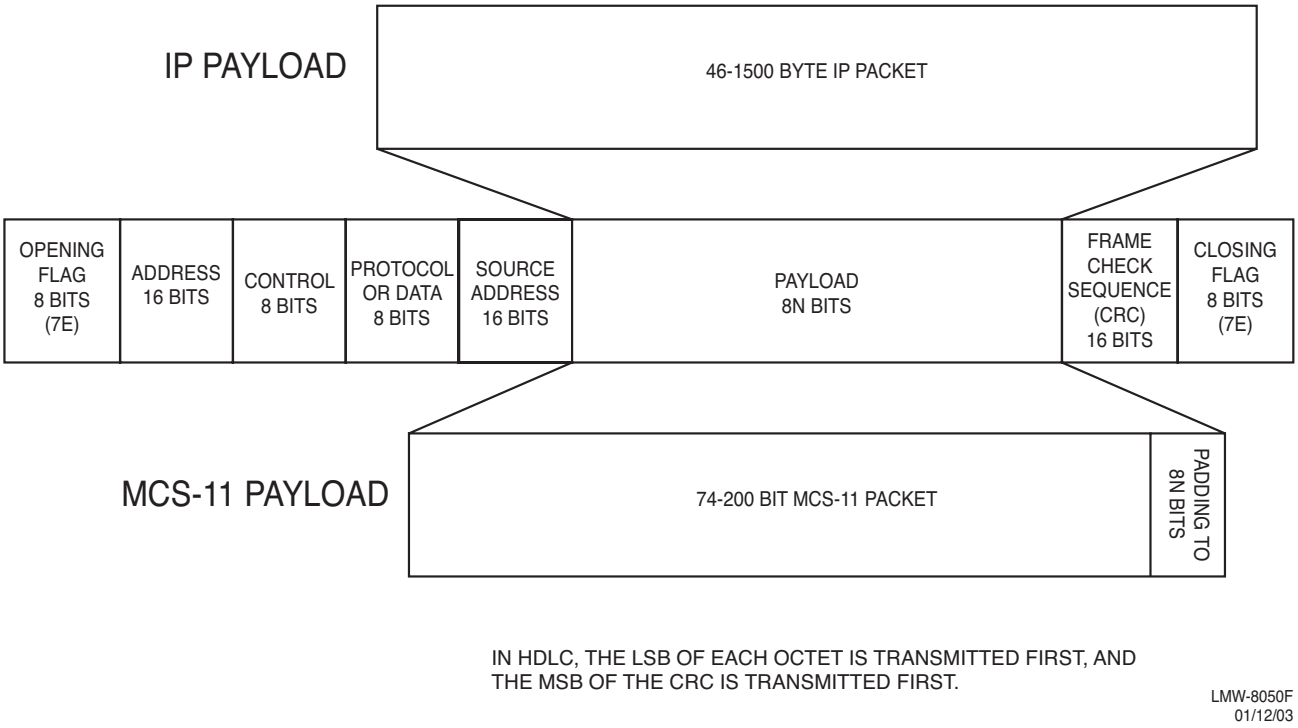

Figure 3-74 Typical Framing Structure

3.12.4 External Alarm, Status, and Control Interface Options

Alarm capacity/availability for the MDR-8000 series radio is summarized as follows:

Office alarms – Standard radio controller module relay outputs (Rack Alarm, Major, and Minor Alarms). Customer must wire to appropriate pins on connector J305.

MCS-11 – Standard provisioning option, enabling function on controller module. MCS-11 software is required but not supplied and must be installed on customer's laptop. Except for repeaters, customer must wire multiple radios to appropriate pins on connector J307, J308, J309, J310, and/or J311 in accordance with the application requirements. Refer to MCS-11 functional description in this section and MCS-11 connections in the Interconnect section for details. Customer must also dedicate (provision) one service channel to carry MCS-11 data. The TSM-2500/8000 series (Transmission Status Monitor) are used to monitor and control the MCS-11.

TBOS – Standard provisioning option, enabling function on controller module. TBOS software is required but not supplied and must be installed on customers' laptop.

SNMP – Optional AE-37AA TMN Interface module and TMN software must be installed. Customer must also dedicate (provision) one service channel to carry the SNMP IP data (can be carried on same service channel as MCS-11 data).

Relay Interface – Optional AE-27A Relay Interface module must be installed. Customer must wire foreign alarm interface to appropriate pins on connector J305. Refer to AE-27A Relay Interface module functional description in this section and relay interface connections in the Interconnect section for details.

3.12.4.1 Relay Interface

The AE-27( ) Relay Interface card provides SPST relays for alarm and status interface between the radio and customer circuits. The relays can be provisioned normally open or normally closed to ground. It also provides an additional 12 inputs for station alarm/status monitoring. Alarm and status interface is provided by connector J305. See interconnect drawing 3DH 03177-EJZZA in the Diagrams Section for connector pinout.

3.12.4.2 MCS-11 Monitor and Control System

Communication between the controller and the MCS-11 master station is based on a polling and response sequence. Alarms, status, and controls for the MCS-11 system include station summary alarms, detail alarms and status, and controls. The MCS-11 system uses a 2-level polling/reporting feature.

Station summary alarm is the level-1 alarm, and is polled on an automatic basis. It is defined as the remote station scanner (RSS) polling word. Detail alarms and status and controls are level-2 alarms polled on a manual (demand) basis. They are defined as the remote detail scanner (RDS) polling word and the remote control decoder (RCD) polling word.

The reporting feature is also 2-level. Level-1 station and summary reporting response is on an automatic basis and is defined as the remote substation data word (RSS). Level-2 detailed alarms and status, analog functions, and controls responses are on a manual (demand) basis, and are defined as follows: the remote subsystem detail data word (RDS), and the remote subsystem control data word (RCD).

3.12.4.3 Service Channels

See Figure 3-75 for typical service channel configurations. There are five functions of which three may be provisioned for the three service channels. The controller inserts and drops the provisioned function for each of the three service channels. Service channel 1 may use RS-232-1, MCS, AUDIO 1 (orderwire), or AUDIO 2. Service channel 2 may use RS-232-2, MCS, AUDIO 1 (orderwire), or AUDIO 2. Service channel 3 may use MCS, AUDIO 1 (orderwire), or AUDIO 2. A function may only be used in one service channel at a time.

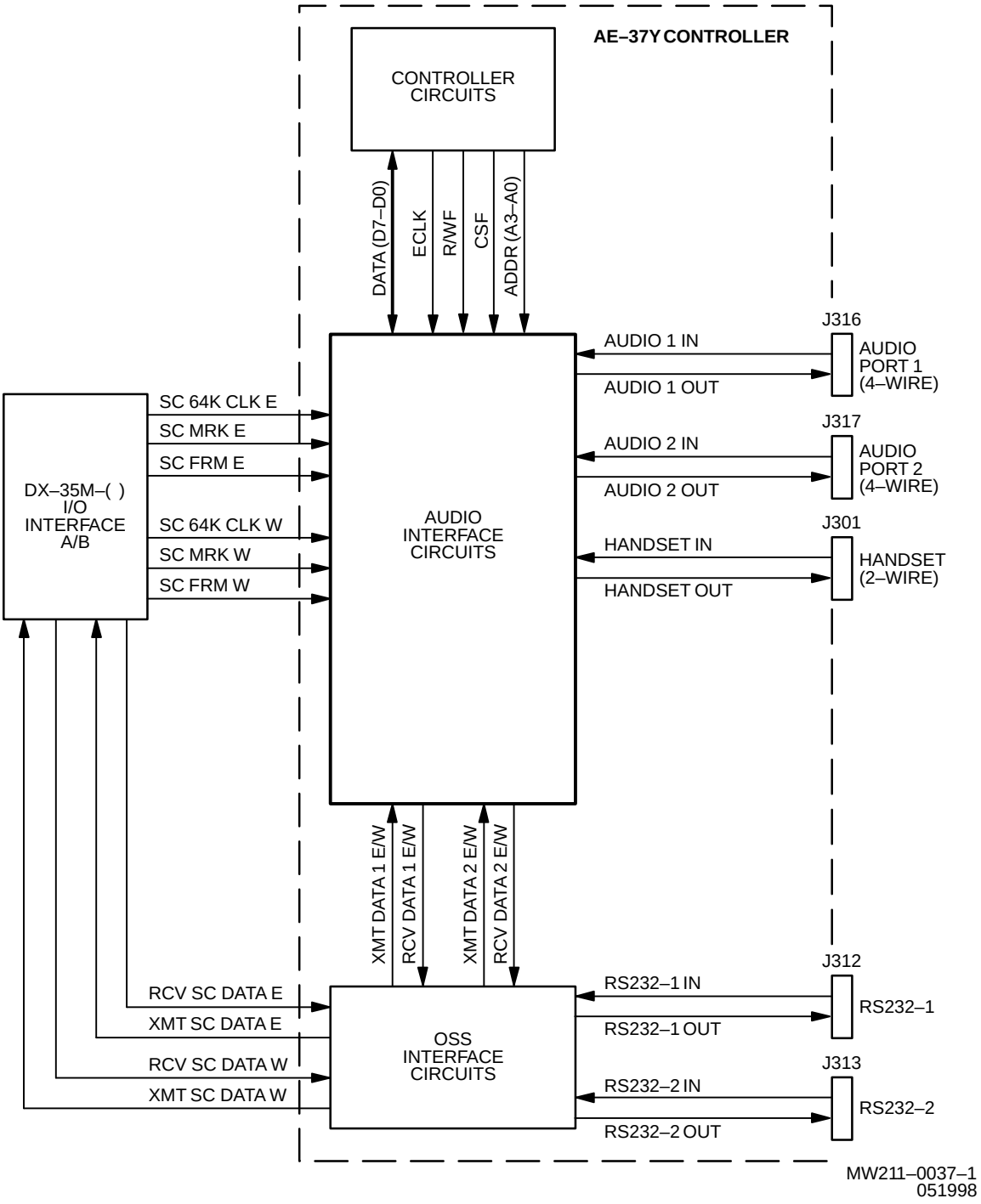

Figure 3-75 Typical Service Channel Configuration

3.12.4.4 Audio Interface

The audio interface converts PCM data to audio for two separate channels. This is done for both the radio and repeater data. Three-way bridging for each channel is provided to combine the radio and repeater audio with the local 4-wire audio. A 2-wire handset interface is provided for the first channel along with DTMF signaling.

3.13 MONITOR AND CONTROL SUBSYSTEM MODULES

Modules are described to the functional block diagram level in the following paragraphs.

3.13.1 AE-37( ) Controller

See Figure 3-76 and Figure 3-77. The AE-37( ) Controller provides alarm collection, alarm reporting, radio control, fault alarm and orderwire functions.

- Provides two independent audio channels
- Converts audio signals into 64 kb/s digital data
- Converts 64 kb/s digital data into audio signals
- Multiplexes and demultiplexes up to two 64 kb/s channels of audio PCM data
- Provides 2-to-4-wire audio conversion
- Provides RS-232 serial data communication port for USI computer interface
- Provides one synchronous MCS-11 interface port
- Provides one asynchronous MCS-11 interface port
- Provides HDLC (16 kb/s) command path interface

The AE-37( ) performs these functions using three main circuits: controller circuit, Operation Support System (OSS) circuit, and audio circuit. The circuit functions are described in the following paragraphs.

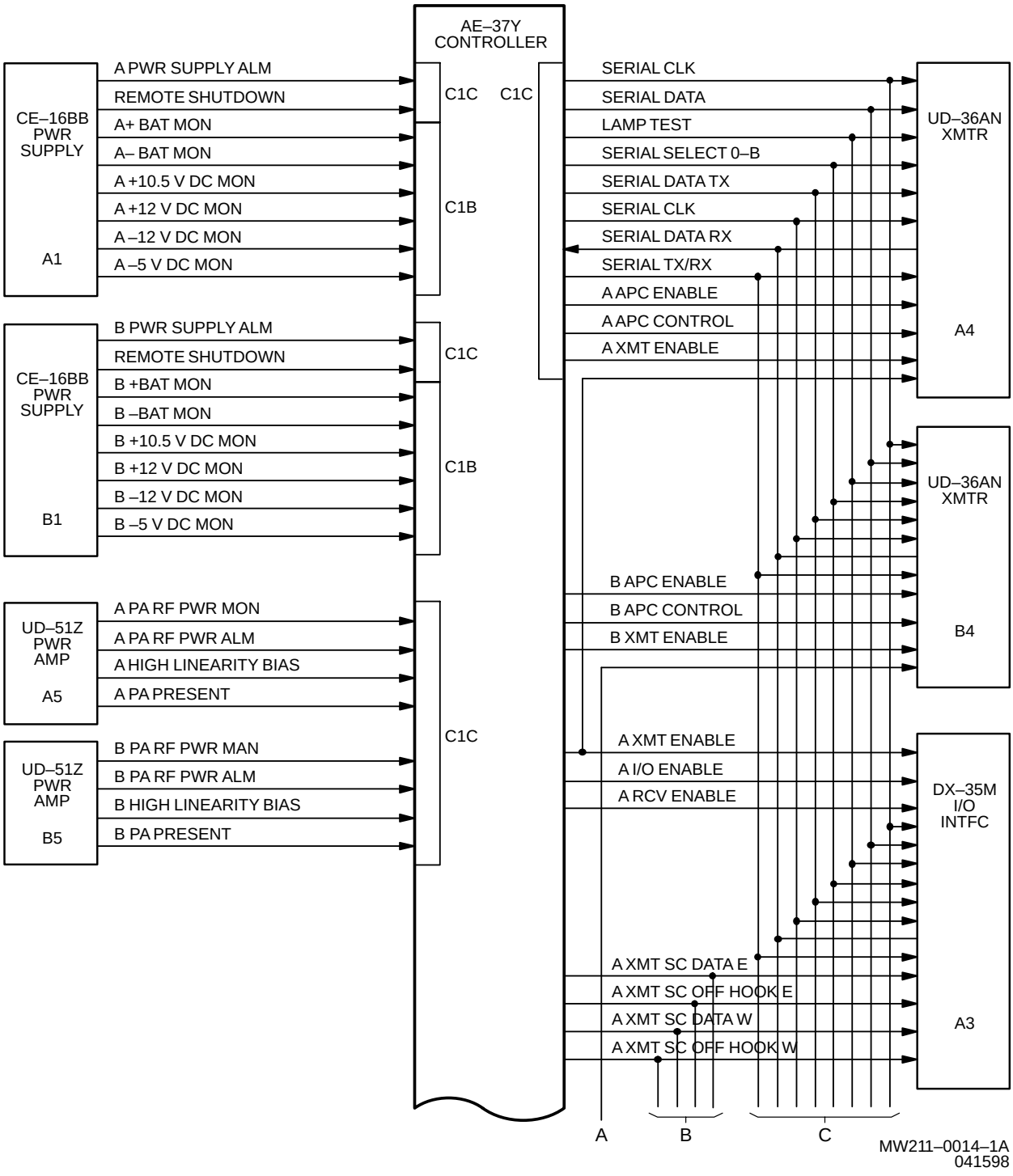

Figure 3-76 Controller Interconnect Diagram (Sheet 1 of 4)

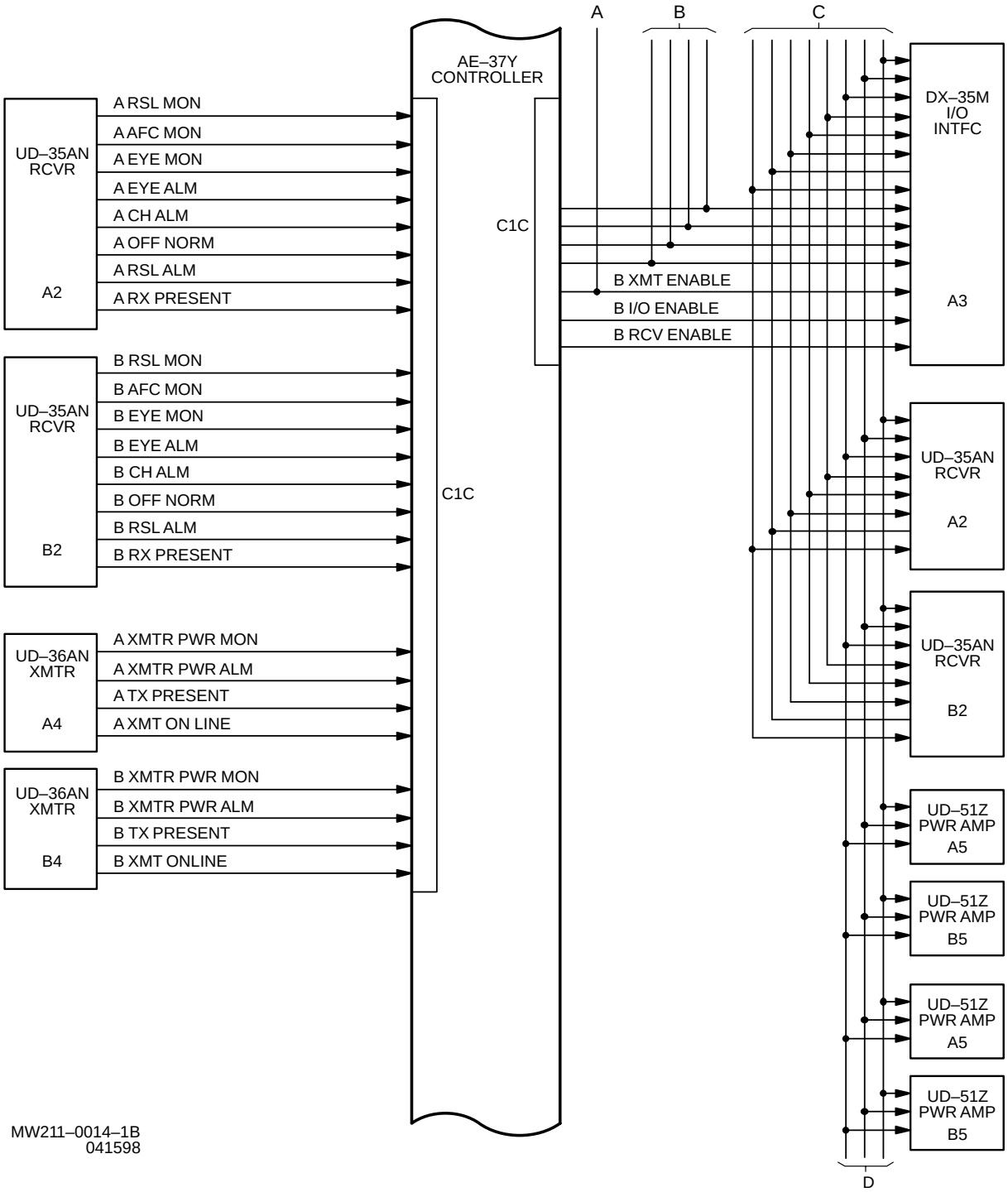

Figure 3-76 AE-37( ) Controller Interconnect Diagram (Sheet 2 of 4)

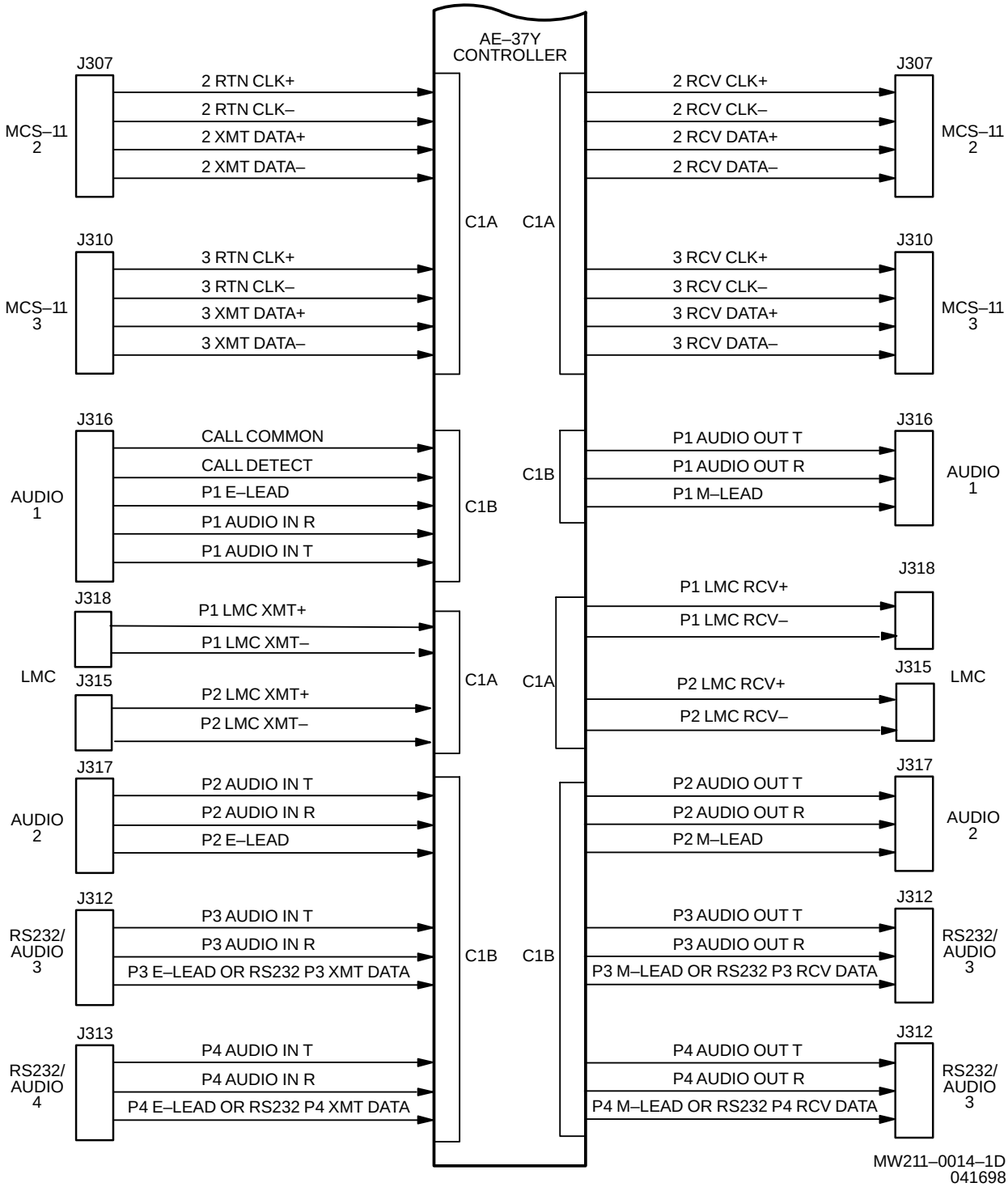

Figure 3-76 AE-37( ) Controller Interconnect Diagram (Sheet 3 of 4)

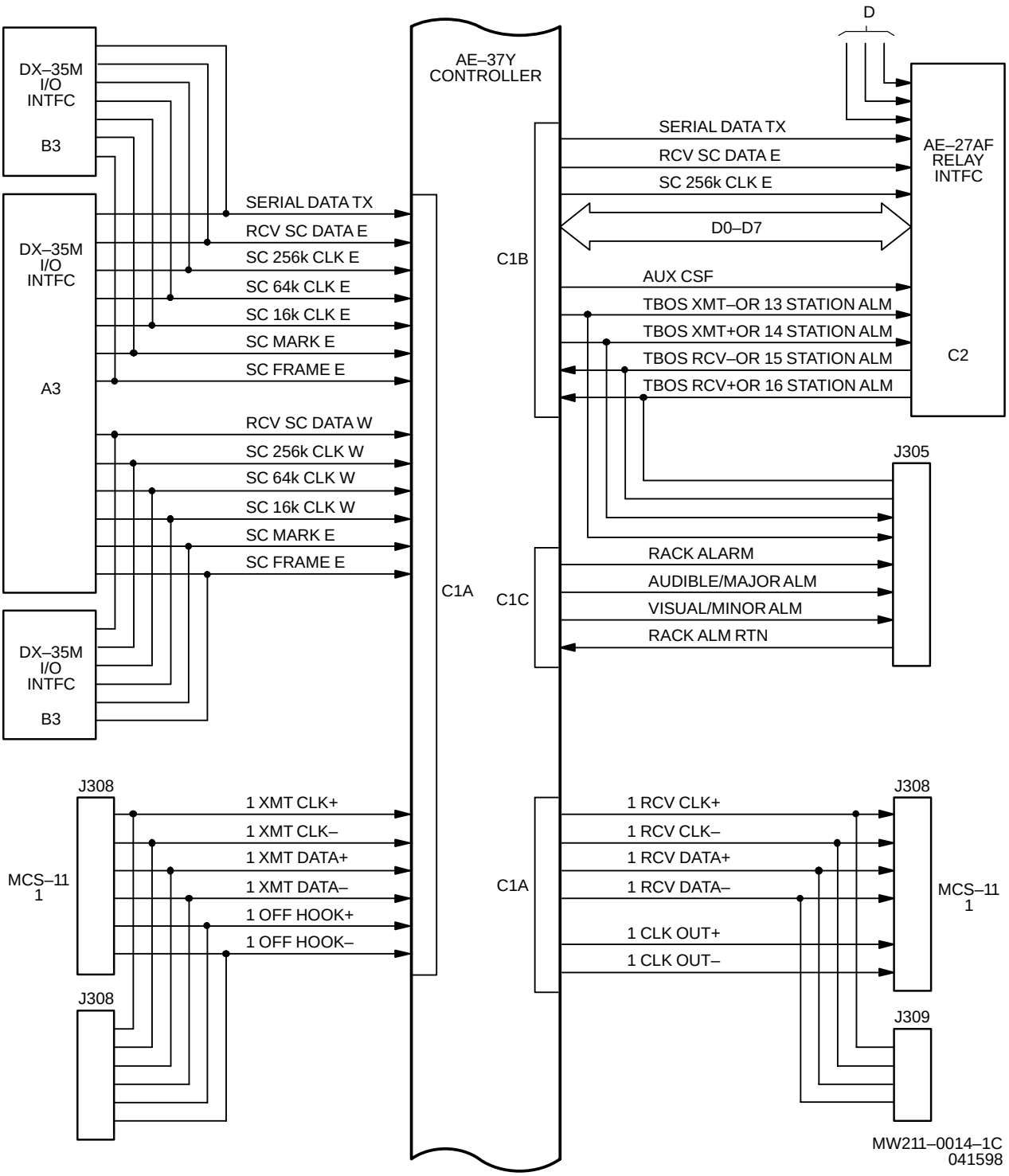

Figure 3-76 AE-37( ) Controller Interconnect Diagram (Sheet 4 of 4)

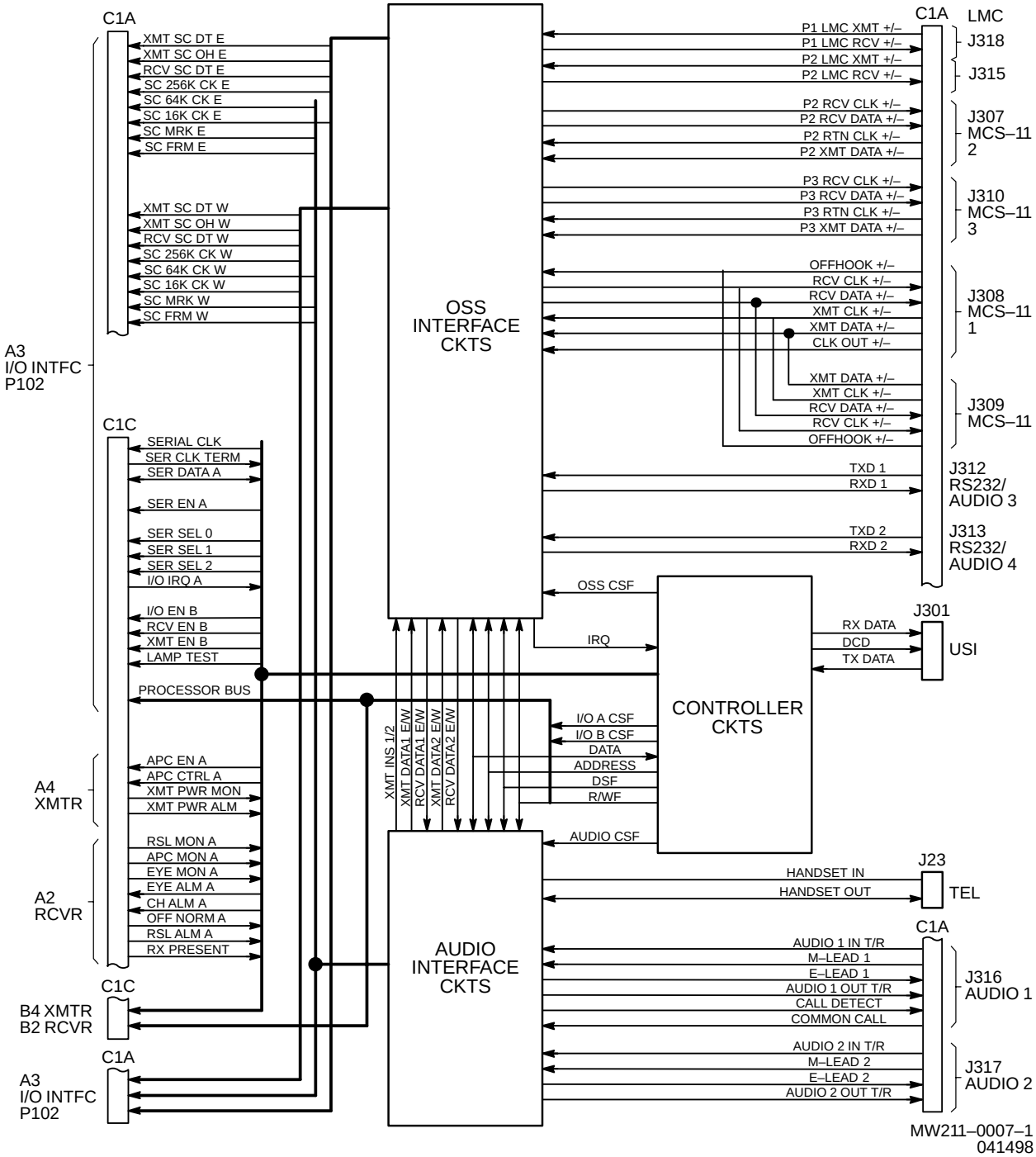

Figure 3-77 AE-37( ) Controller Functional Block Diagram

3.13.1.1 Controller Circuit Functions

See Figure 3-78. The controller circuits manage command path communications, status and alarm interfaces, and switching. The microprocessor collects and distributes switching and alarm information and provides/processes the serial link to the farend controller, the A- and B-side serial communications, the ATPC commands, and the analog status voltages. The microprocessor reads the remaining analog status voltages, communicates between the USI laptop computer, and services the fault interface, relay interface, and station control/monitor circuit functions. Farend input/output functions interface through the farend 16 kb/s low-speed data stream between the controller and DX-35( ) I/O Interface. The local 16 kb/s command path is the back-to-back repeater-to-controller interface in adjacent racks.

3.13.1.1.1 MC68360 Microprocessor

The MC68360 is a one chip integrated microprocessor and peripheral combination with general purpose timers, two serial I/O subsystems, programmable chip selects, a watchdog timer, and test and debug support.

3.13.1.1.2 Memory

Program memory is 256k x 32-bit flash EPROM. Variables are stored in 128k x 32-bit RAM. Provisioning information is stored in a 8 kbyte EEPROM. The provisioning information in the EEPROM is protected by a low voltage detector that resets the microprocessor whenever a low voltage condition is detected on the +5 V power supply.

3.13.1.1.3 Switch Control

The switch control function monitors and displays system alarms and switches between the A- and B-sides of the radio on hot-standby protected systems. All system alarms for the A- and B-sides of the radio are displayed on the USI laptop computer and/or receiver and transmitter fail alarms are displayed on the I/O interface.

Transmit, receive, and I/O enable outputs for both the A and B side are provided to software and can be overridden by hardware via the front panel switches. For example, selecting the RCV A and OVRD sets the RCV ENABLE A bit and resets the RCV ENABLE B bit. Logic is in place that will not allow both receivers or both I/O sections to be placed on line at the same time. The driving of an enable bit is under the control of software except when an override of that function is requested.

3.13.1.1.4 USI

See Figure 3-78, Sheet 2. Communication to the User System Interface (USI) is via controller front panel connector J301 and the Serial Communications Interface (SCI), internal to the MC68360 peripheral section.

3.13.1.2 Operation Support System (OSS) Circuit

See Figure 3-78. The OSS circuit provides serial communication port interfaces to the system controller and interfaces with the I/O interface module to multiplex and demultiplex the service channel data. It provides two synchronous 64 kb/s MCS interfaces (one for the radio path and one between repeaters) and one asynchronous interface for local drop and insert. It provides multiplexing and demultiplexing for up to two 64 kb/s of audio PCM data. It also provides a 16 kb/s interface for controller command path data over the radio

path and between repeaters. The OSS circuits consist of two service channel muldems, address and register data busses, serial communication ports, and RS-232 ports.

3.13.1.2.1 Front Panel Controls and Indicators

See Figure 3-78 Sheet 1. Twenty two LEDs and four switches are mounted on the front panel. Fifteen front panel LEDs light/flash to indicate status of controller/system. One alarm LED lights to indicate controller failure and one LED lights to indicate a shelf alarm. The LEDs are controlled/driven by the Enhanced Serial Communication Controller (ESCC). Refer to the Operations section for control and indicator details.

3.13.1.2.2 SPI Bus

See Figure 3-78 Sheet 2. The Serial Processor Interface (SPI) bus interfaces the MC68360 peripheral section with the EPLD that controls bus operations. Serial data is transmitted to and received from the MDR-8000 modules via the SPI bus. The SPI bus is controlled by the SER TX/RX and SERIAL SELECT 0-3 outputs of the transceiver. The SER TX/RX logic determines the mode of operation. The SERIAL SELECT 0-3 lines select the module. The SPI CLK clocks the SERIAL SELECT 0-3 into the transceiver.

3.13.1.2.3 I^2C Bus

The I^2C bus consists of one bidirectional data line and a clock. Serial data received over the I^2C bus includes part numbers and revision history (all modules and the backplane) and also capacity key information and crystal frequency from the transmitter and receiver.

3.13.1.2.4 Register Data Bus

See Figure 3-78 Sheet 4. The register data bus interfaces the MC68360 processor with the peripherals and other controller circuits, the OSS circuits, and the audio circuits. Individual chips are addressed via the address bus and enabled by the chip select lines (CS0 - CS6).

Three I^2C master bus controllers interface the I^2C bus with all MDR-8000 modules.

Analog-to-digital converters interface the register data bus and analog signals from the MDR-8000 modules. The analog signals consists of voltages from the power supplies (+10.5, +12, -12 and -5 Vdc) , RF power monitor voltage (PA RF PWR MON) from the power amplifiers (if equipped), RF power monitor voltage (XMT PWR MON) from the transmitter modules, and receive level monitor voltage (RSL MON), AFC voltage (AFC MON), and a voltage representative of the signal quality (EYE MON) from the receivers.

Transceivers interface the register data bus and digital alarm and status data from the MDR-8000 modules. Configuration status signals (TX PRESENT, RX PRESENT, and PA PRESENT) are used to inform the processor of current configuration which is then used by the processor logic to control functions, such as switching and the transmit ALC loop. Alarms applied to the register data bus include PA power supply (PA PS) alarm and PA power alarm (PA PWR ALM) from the power amplifiers (if equipped), combiner alarm (COMBINER ALM, if equipped with combiner), XMT PWR ALM from transmitter modules, power supply alarm (PS ALM) from power supplies, and channel fail alarm (CH FAIL), EYE CLOSURE, and RSL alarms from the receiver modules. Refer to functional description of relay interface module in this section for alarm descriptions.

A digital-to-analog converter for each side of the radio sends a dc voltage (ATPC CONTROL) to the A and B power amplifier.

3.13.1.2.5 Power Amplifier Control Circuits

See Figure 3-78 Sheet 2. The EPLD controls operating power to the power amplifiers and high biases the power amplifiers during high power operation when increased linearity is required. The EPLD sends a REMOTE KILL PWR signal through a TTL switch (KILL 10.5 V TO PA) that disables the 10.5 volt output of the power supplies to the power amplifiers. The HIGH LINEARITY BIAS signal high biases the power amplifiers.

3.13.1.2.6 MCS-11 Interface

See Figure 3-78 Sheet 1. When MCS is properly provisioned, four ports on the EPLD and microprocessor on the controller module are enabled, allowing the user to interface external MCS-11 Monitor and Control System equipment at four connectors on the backplane (J307, J308, J309, and J310). Two connectors (J308 and J309) are synchronous, parallel, data ports and provide CLK outputs. Connectors J307 and J310 are asynchronous ports.

For proper operation, MCS-11 must be provisioned using the following guidelines:

a. **MCS-11** must be selected as one of the service channels.

b. MCS must be assigned a valid address.

c. **MCS RSS** must be **ON** to allow controller to respond when polled.

Note

*MCS-11 must be provisioned **MCS-11 J310 Master/Junction** to enable XMT, RCV, and OUTPUT clocks. If an external modem is being used, provision MCS-11 for **MCS-11 J310 Modem**. This selection disables XMT, RCV, and OUTPUT clocks and all MCS-11 clocks must now be provided by the external modem.*

d. **MCS-11 J310 Master/Junction** must be selected unless an external modem is connected to the radio. If an external modem is used it must provide all MCS-11 clocks and the radio must be provisioned **MCS-11 J310 Modem.**

Note

*When provisioned **J308 Input Clock**, J308 and J309 RCV CLK and XMT CLK and J308 OUTPUT CLK are disabled. Select* **J308 Output Clock** *to send a 64 kb/s clock to external equipment (OUTPUT CLK J308-4/12) and also enable RCV CLK and XMT CLK.*

e. **MCS-11 J308 Output Clock** must be selected unless an external clock source is provided that will supply all MCS-11 clocks. If an external clock source is used, the radio must be provisioned MCS-11 J308 Input Clock.

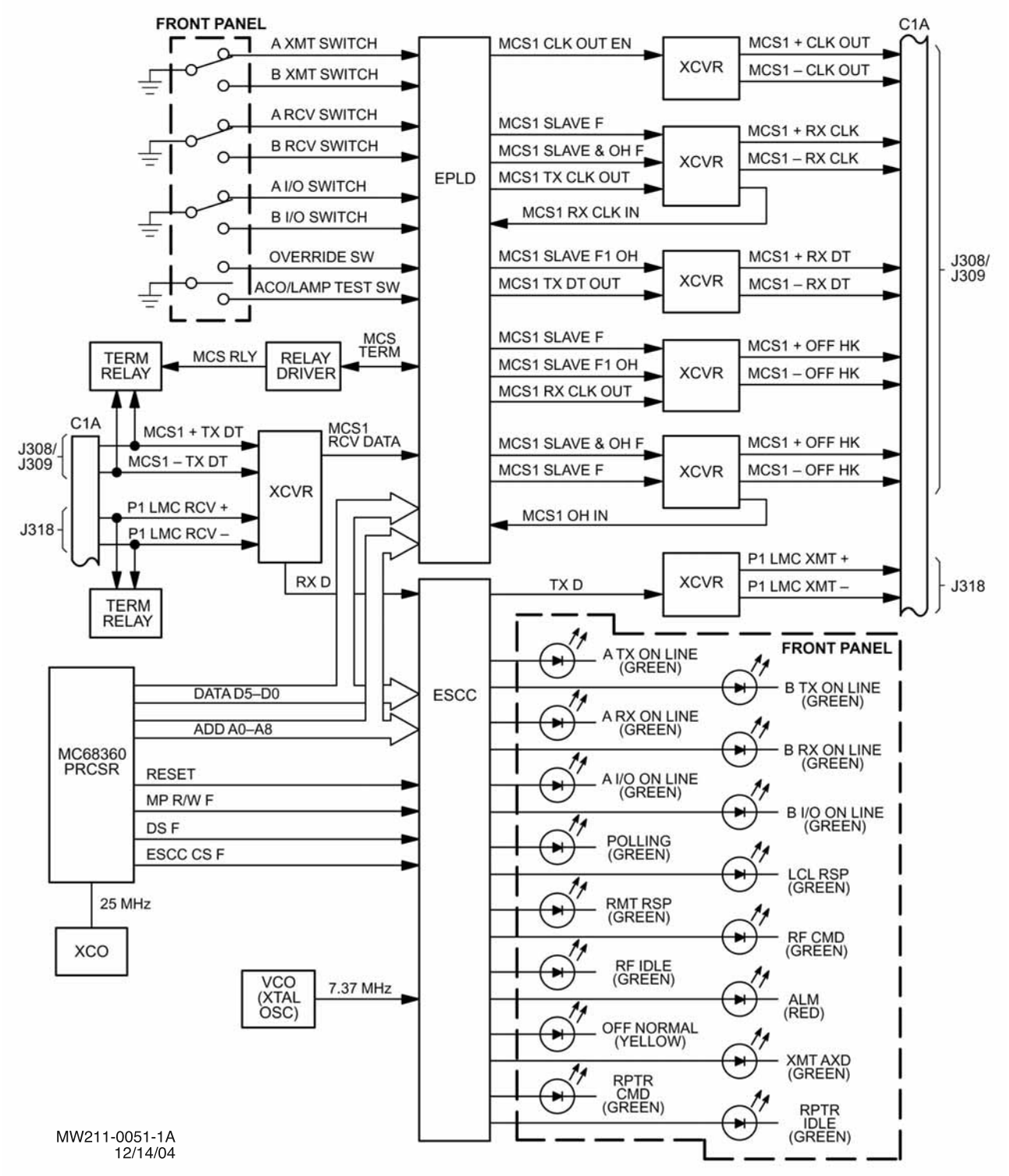

Figure 3-78 Controller/OSS Circuits Functional Block Diagram (Sheet 1 of 4)

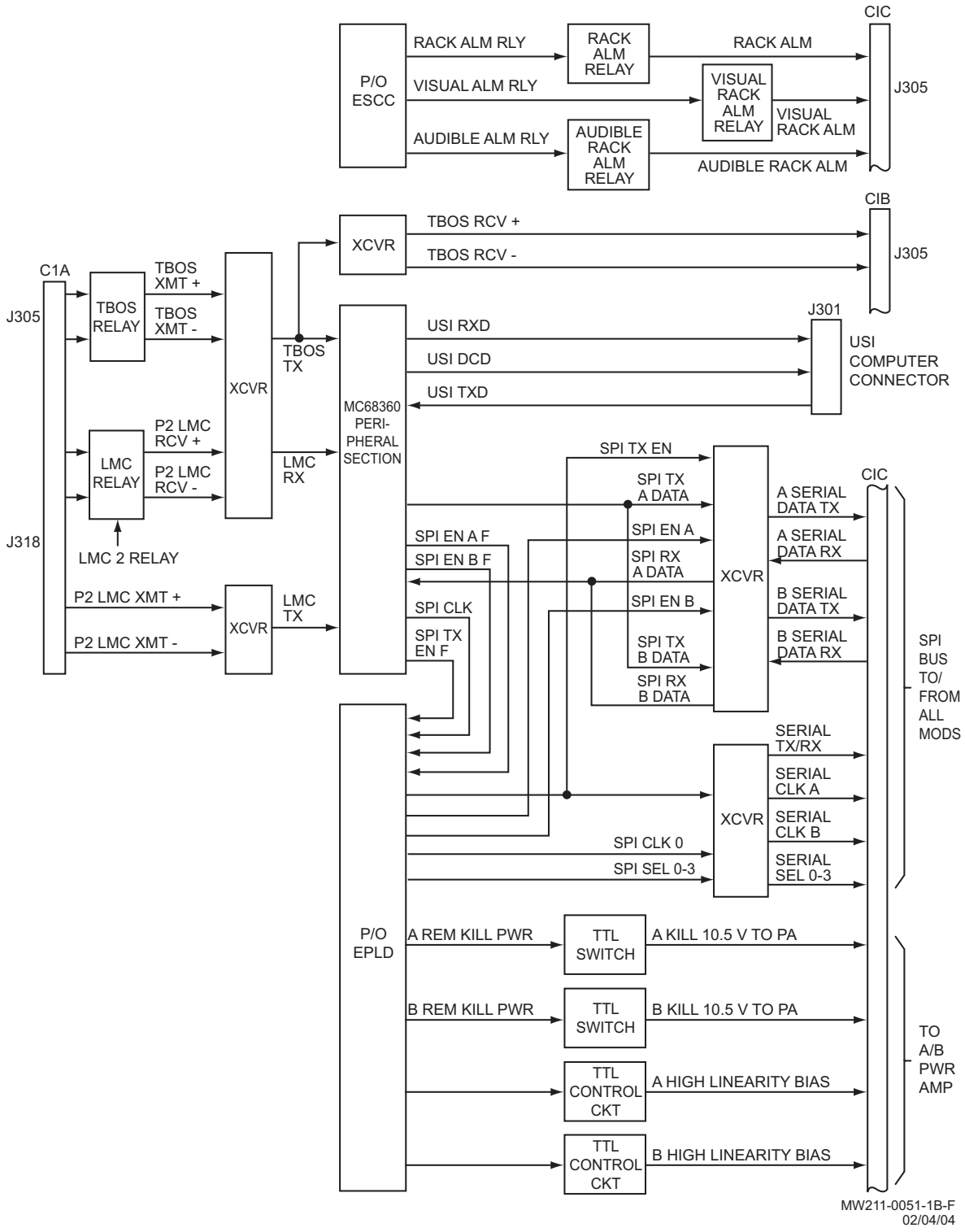

Figure 3-78 Controller/OSS Circuits Functional Block Diagram (Sheet 2 of 4)

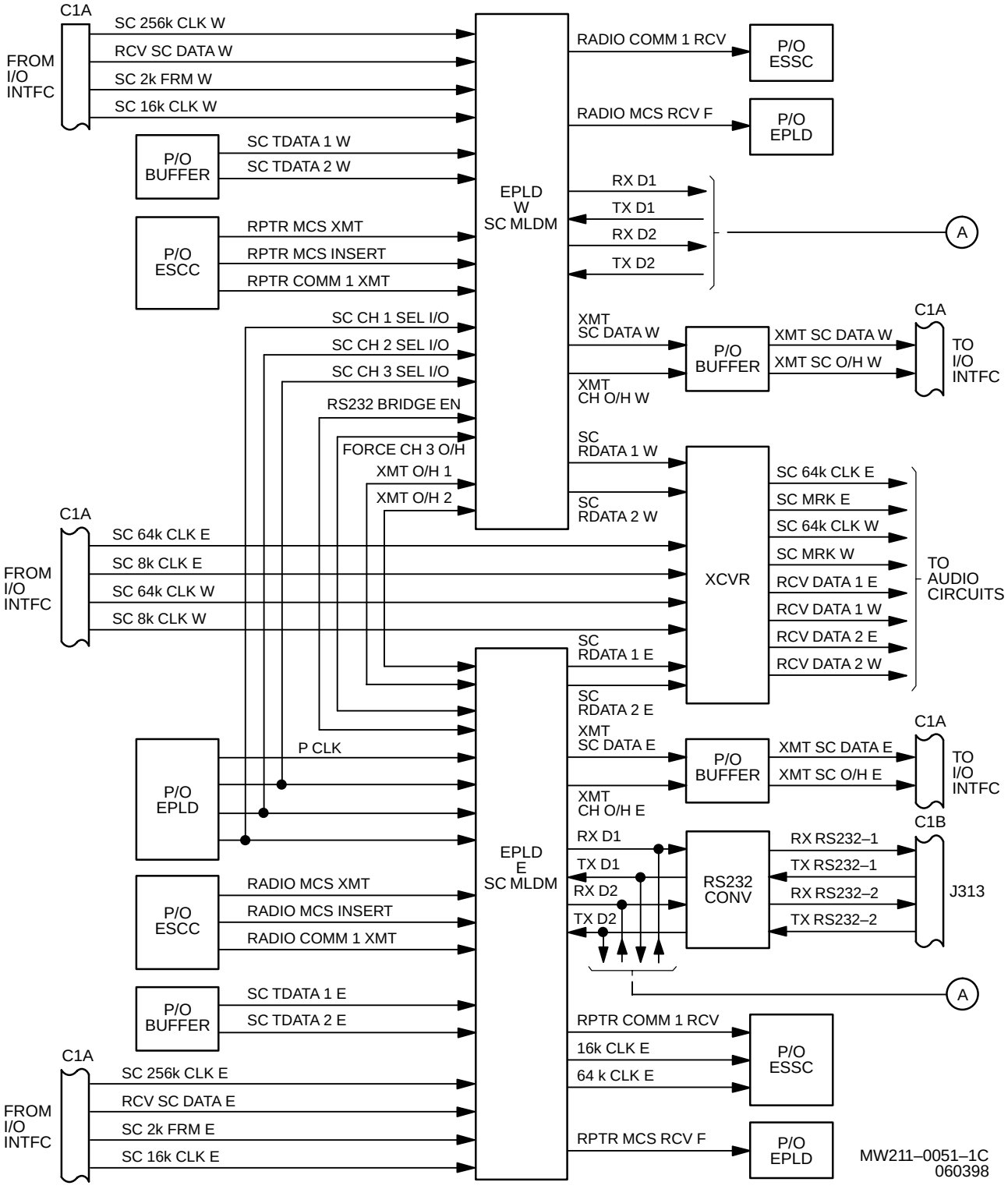

Figure 3-78 Controller/OSS Circuits Functional Block Diagram (Sheet 3 of 4)

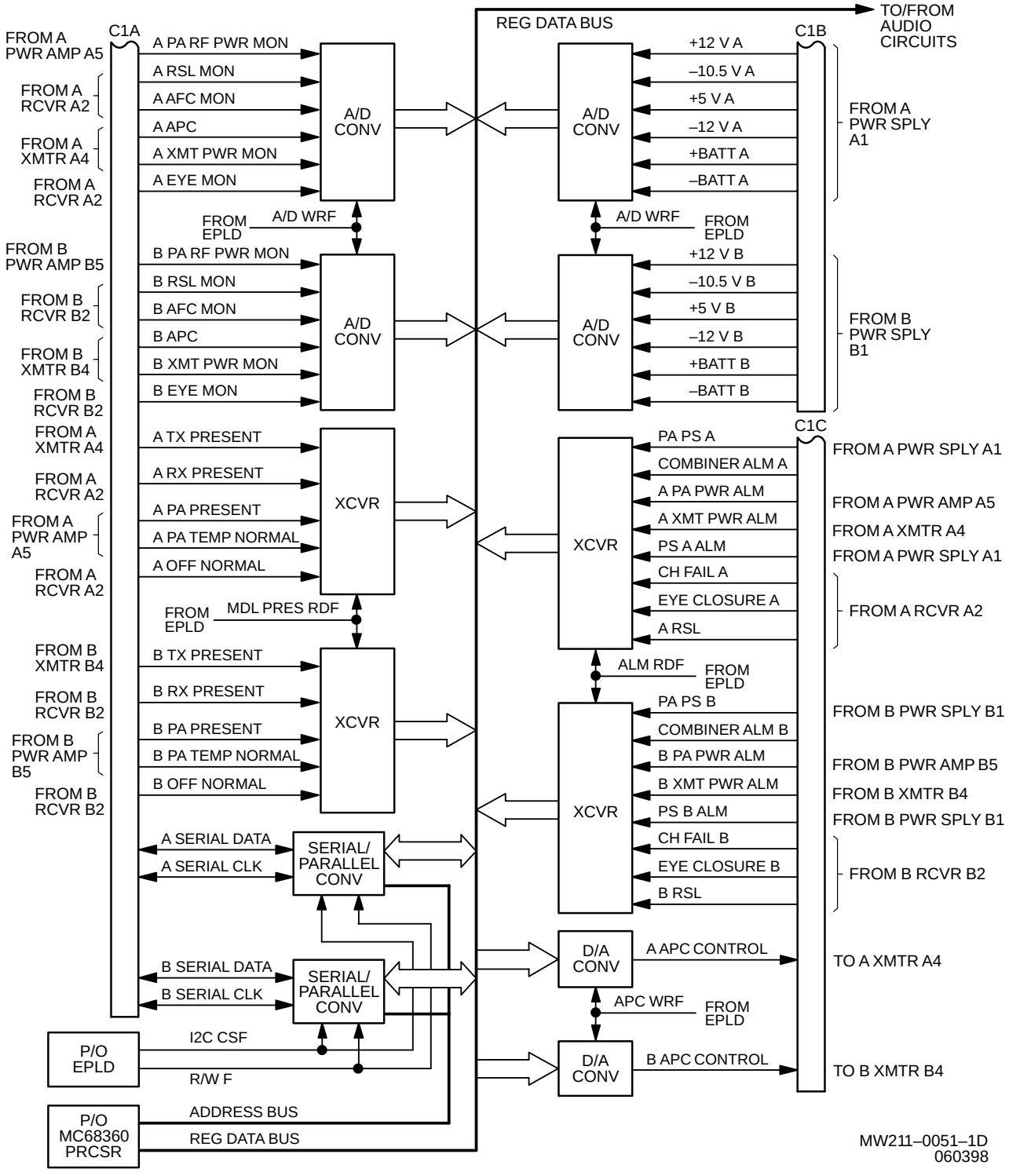

Figure 3-78 Controller/OSS Circuits Functional Block Diagram (Sheet 4 of 4)

3.13.1.2.6.1 Port 1

Note

Applicable signal lines, functions, and components are highlighted on the block diagram. Associated signal lines, functions, and components are faded.

See Figure 3-79. The EAST CLK is used to clock RCV data out of the microprocessor, through the EPLD, and to the east SC muldem. The WEST CLK is used to clock XMT data from the west SC muldem into the microprocessor.

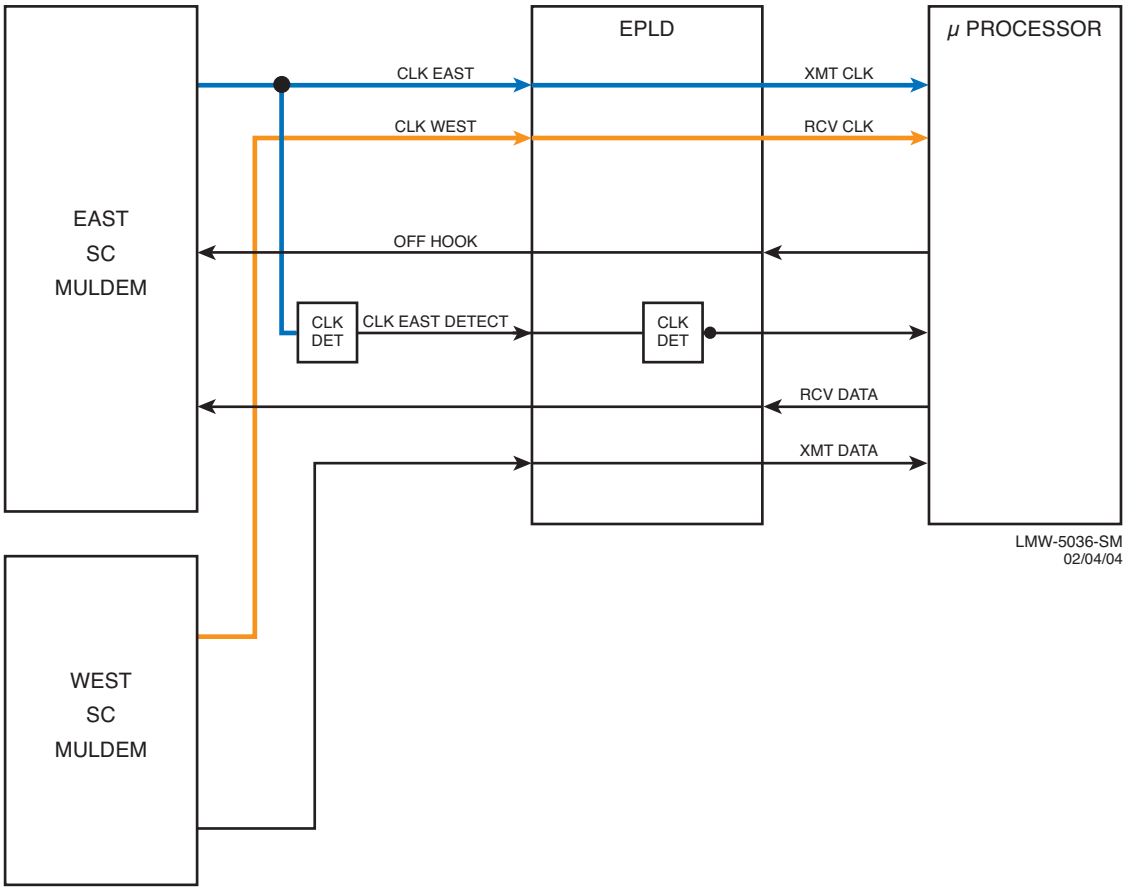

Figure 3-79 MCS-11 Port 1 Clocks Signal Flow

3.13.1.2.6.2 Port 2

Note

Applicable signal lines, functions, and components are highlighted on the block diagram. Associated signal lines, functions, and components are faded.

See Figure 3-80 and Figure 3-81. Port 2 interfaces connector J307 at a terminal or the east and west service channel muldems at a repeater. The interface is controlled by software switching in the EPLD that switches XMT/RCV clock and data to/from the microprocessor.

Note

*MCS-11 must be provisioned **MCS-11 J310 Master/Junction** to enable XMT, RCV, and OUTPUT clocks. If an external modem is being used, provision MCS-11 for **MCS-11 J310 Modem**. This selection disables XMT, RCV, and OUTPUT clocks and all MCS-11 clocks must now be provided by the external modem.*

3.13.1.2.6.3 Terminal

See Figure 3-80. When provisioned as a terminal, the EPLD switches to position 1. XMT DATA at J307 is switched to the EPLD output and clocked into the microprocessor using CLK EAST output of the east SC muldem. RCV DATA is clocked out of the microprocessor by the RTN CLK and is switched through position 1 of the EPLD switch to J307.

3.13.1.2.6.4 Repeater

See Figure 3-81. When provisioned as a repeater, the EPLD switches to position 2. XMT DATA is switched to the EPLD output and clocked into the microprocessor using CLK WEST output of the west SC muldem. RCV DATA is clocked out of the microprocessor by the CLK EAST output of the east SC muldem and is switched through position 2 of the EPLD switch to the west SC muldem.

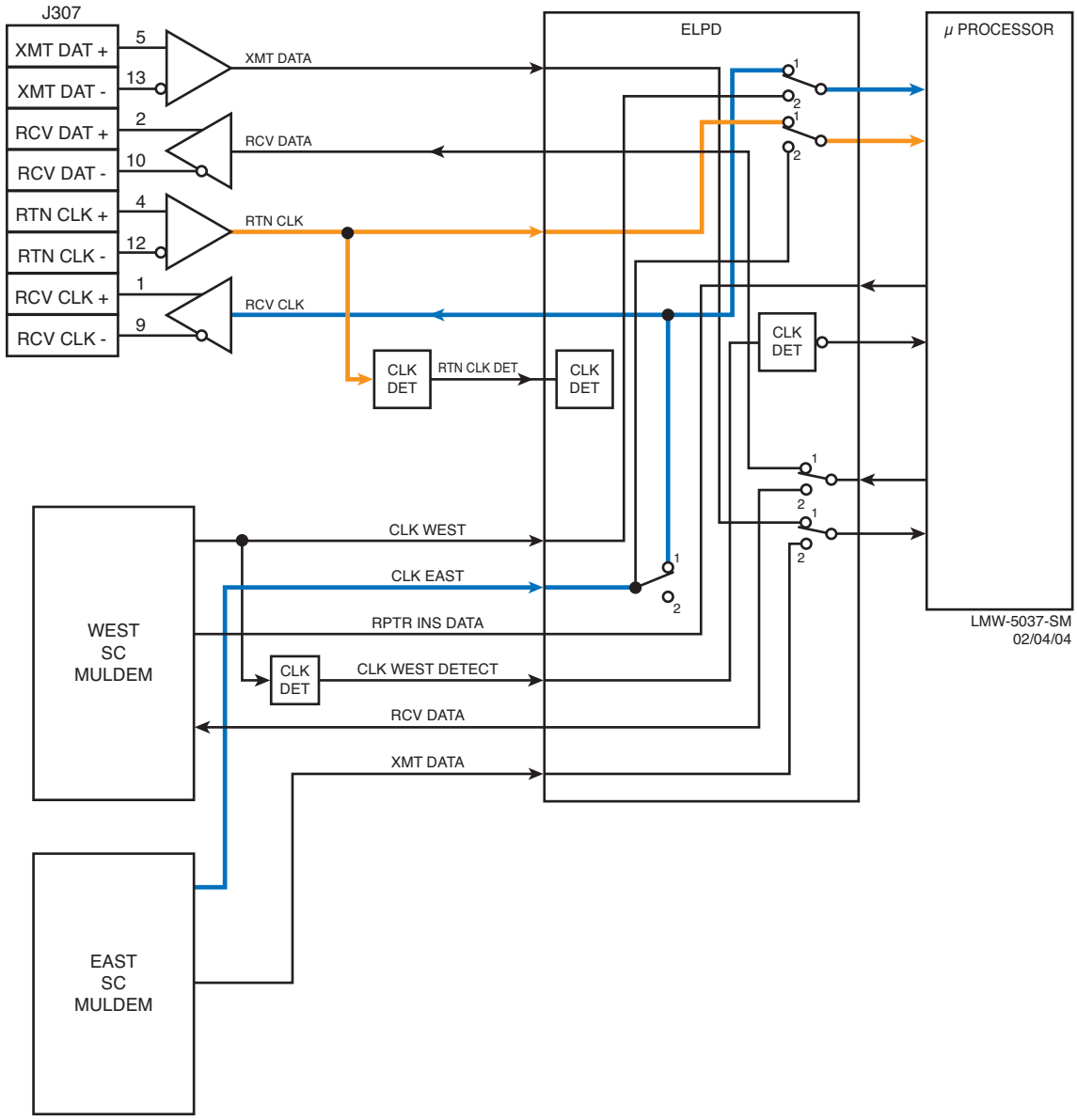

Figure 3-80 MCS-11 Port 2 Clocks Signal Flow, Terminal Configuration

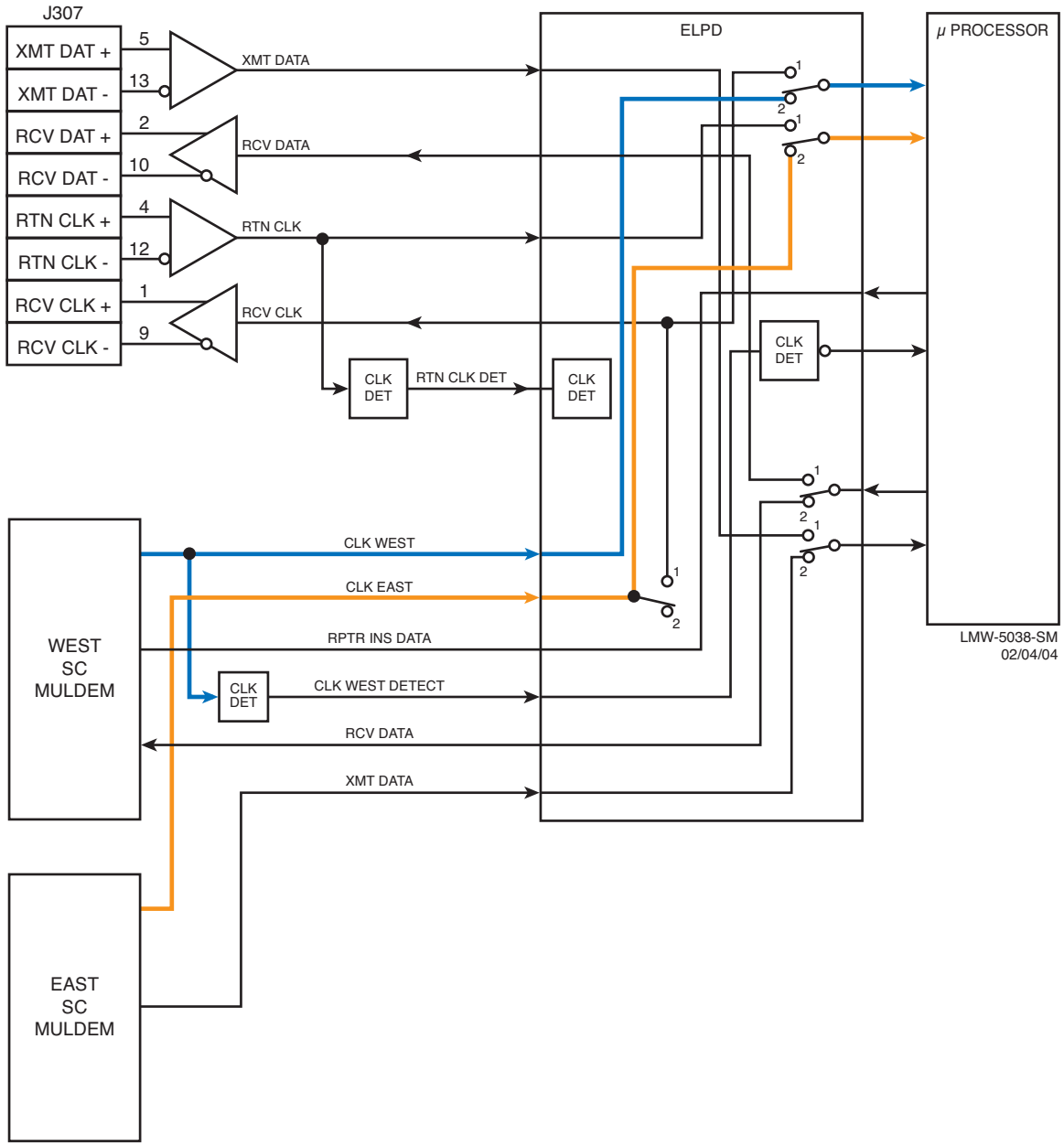

Figure 3-81 MCS-11 Port 2 Clocks Signal Flow, Repeater Configuration

3.13.1.2.6.5 Port 3

Note

Applicable signal lines, functions, and components are highlighted on the block diagram. Associated signal lines, functions, and components are faded.

See Figure 3-82, Figure 3-83, and Figure 3-84. Port 3 XMT data is clocked into the microprocessor by the return clock (RTN CLK). The RTN CLK is generated by an external source in response to the external equipment receiving the RCV CLK (J310-1/9). The RCV CLK driver is enabled by the RCV ENABLE signal from the TX/RXF select control in the EPLD. Port 3 RCV data is clocked out of the microprocessor by one of three clocks; RTN CLK (same clock used by Port 3 XMT), RCV CLK, or CLK EAST.

3.13.1.2.6.6 Return Clock

See Figure 3-82.When the RTN CLK (J310-4/12) is detected, it is switched through position 3 of the EPLD switch to the microprocessor.

3.13.1.2.6.7 RCV Clock

See Figure 3-83. When the RCV CLK is used as an input, the XMT CLK driver (J310-1/9) is turned on by the XMT ENABLE signal from the TX/RXF select control in the EPLD. When the XMT CLK is detected, it is switched through position 1 of the EPLD switch to the microprocessor.

3.13.1.2.6.8 Clock East

See Figure 3-84.When CLK EAST from the east SC muldem is detected, it is switched through position 2 of the EPLD switch to the microprocessor.

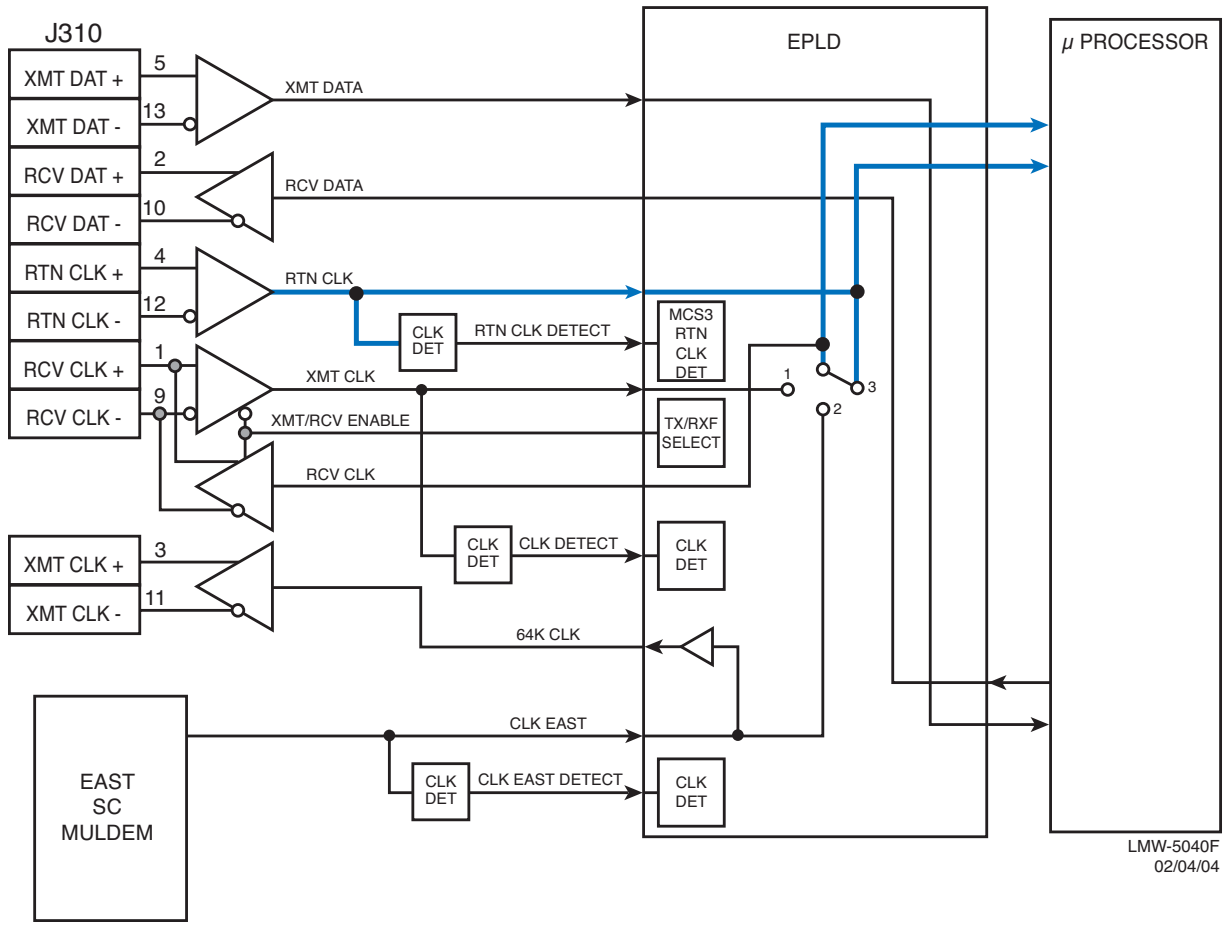

Figure 3-82 MCS-11 Port 3 Return Clock Signal Flow

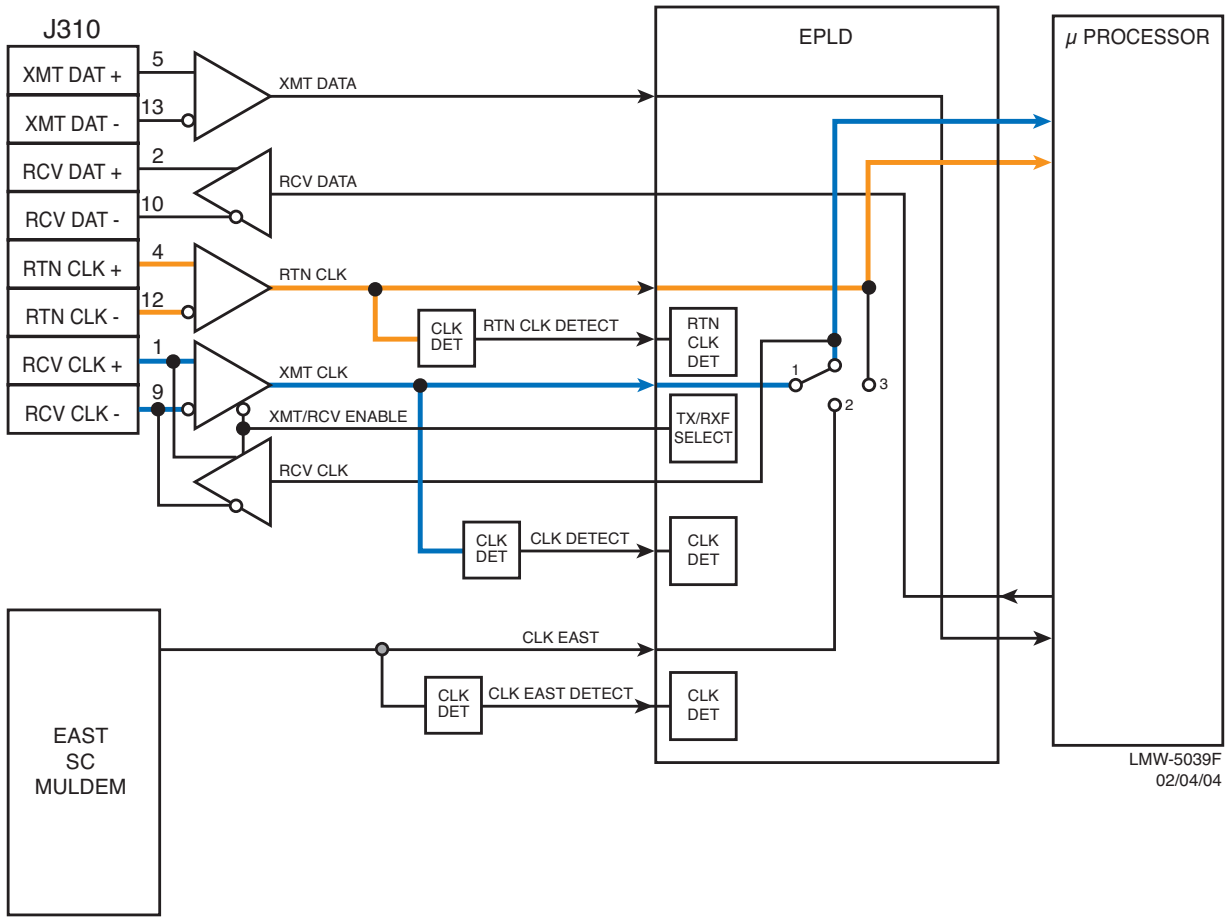

Figure 3-83 MCS-11 Port 3 RCV Clock Signal Flow

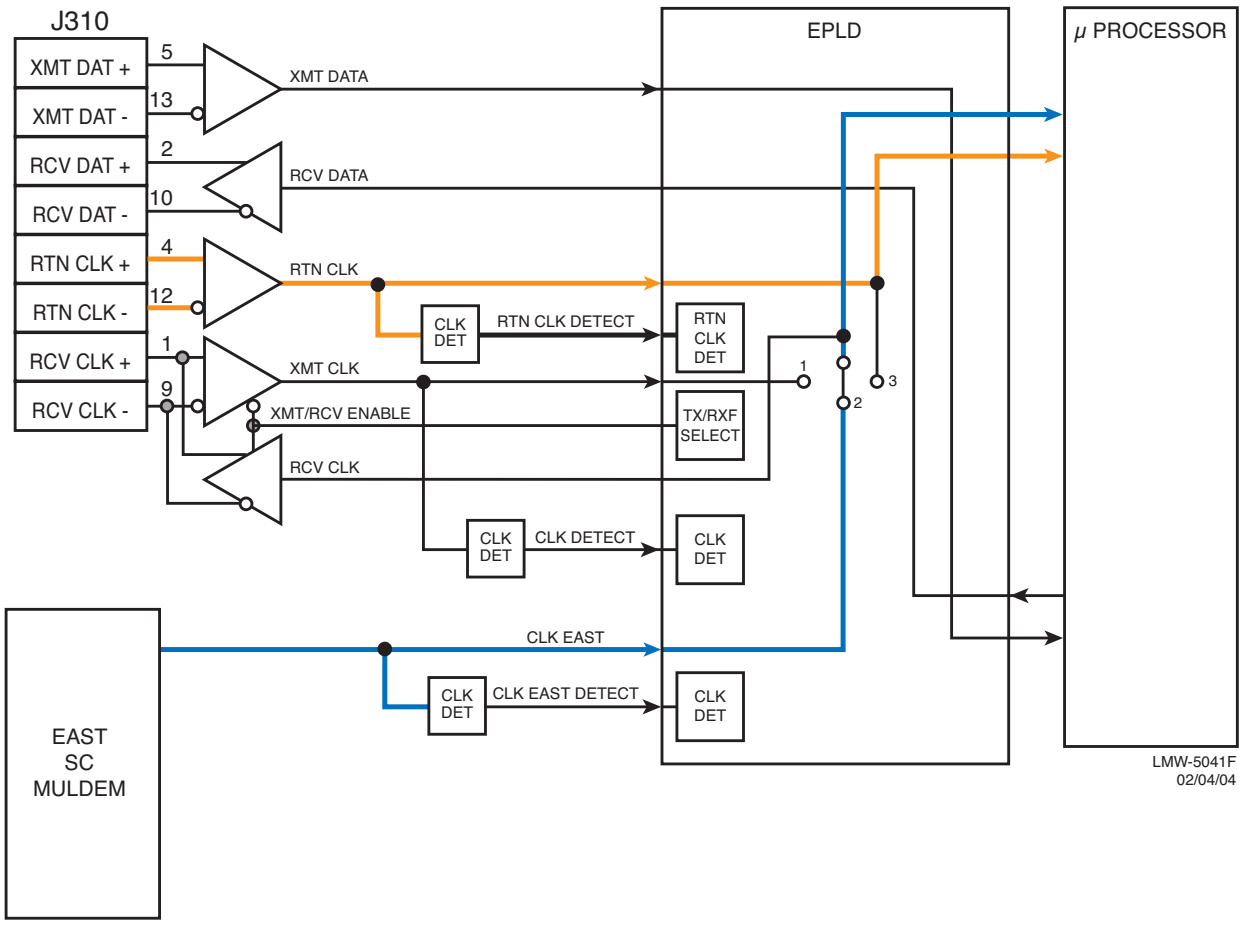

Figure 3-84 MCS-11 Port 3 Clock East Signal Flow

Note

Applicable signal lines, functions, and components are highlighted on the block diagram. Associated signal lines, functions, and components are faded.

Note

Only one connector on an asynchronous port can be used at a time. J308 and J309 can not be used simultaneously in the same shelf.

3.13.1.2.6.9 Port 4

See Figure 3-85, Figure 3-86, and Figure 3-87. Port 4 RCV data is clocked out of the microprocessor by CLK EAST. Port 4 XMT data is clocked into the microprocessor by either of two clocks; CLK EAST or CLK WEST. The XMT CLK and RCV CLK are bi-directional. Direction is determined by bidirectional XCVRs. The bi-directional XCVR is controlled by the switch control logic on the EPLD.

3.13.1.2.6.10 Clock East

See Figure 3-85. When CLK EAST from the east SC muldem is detected, it is switched through position 1 of the EPLD switch to the microprocessor and J308 and J309 output drivers as follows:

SIGNAL NAME	DESTINATION
XMT CLK	MICROPROCESSOR
	J308-3/11
	J309-3/11
RCV CLK	MICROPROCESSOR J308-1/9
	J309-1/9

Note

*When provisioned **J308 Input Clock**, J308 and J309 RCV CLK and XMT CLK and J308 OUTPUT CLK are disabled. Select **J308 Output Clock** to send a 64 kb/s clock to external equipment (OUTPUT CLK J308-4/12) and also enable RCV CLK and XMT CLK.*

When provisioned J308 CLK OUT ENABLE, CLK EAST also drives the output driver for CLK OUT (J308-4/12).

3.13.1.2.6.11 Clock West

See Figure 3-86. When CLK WEST from the west SC muldem is detected, it is switched through position 2 of the EPLD switch to the microprocessor and to the XMT CLK driver (J308-3/11 and J309-3/11).

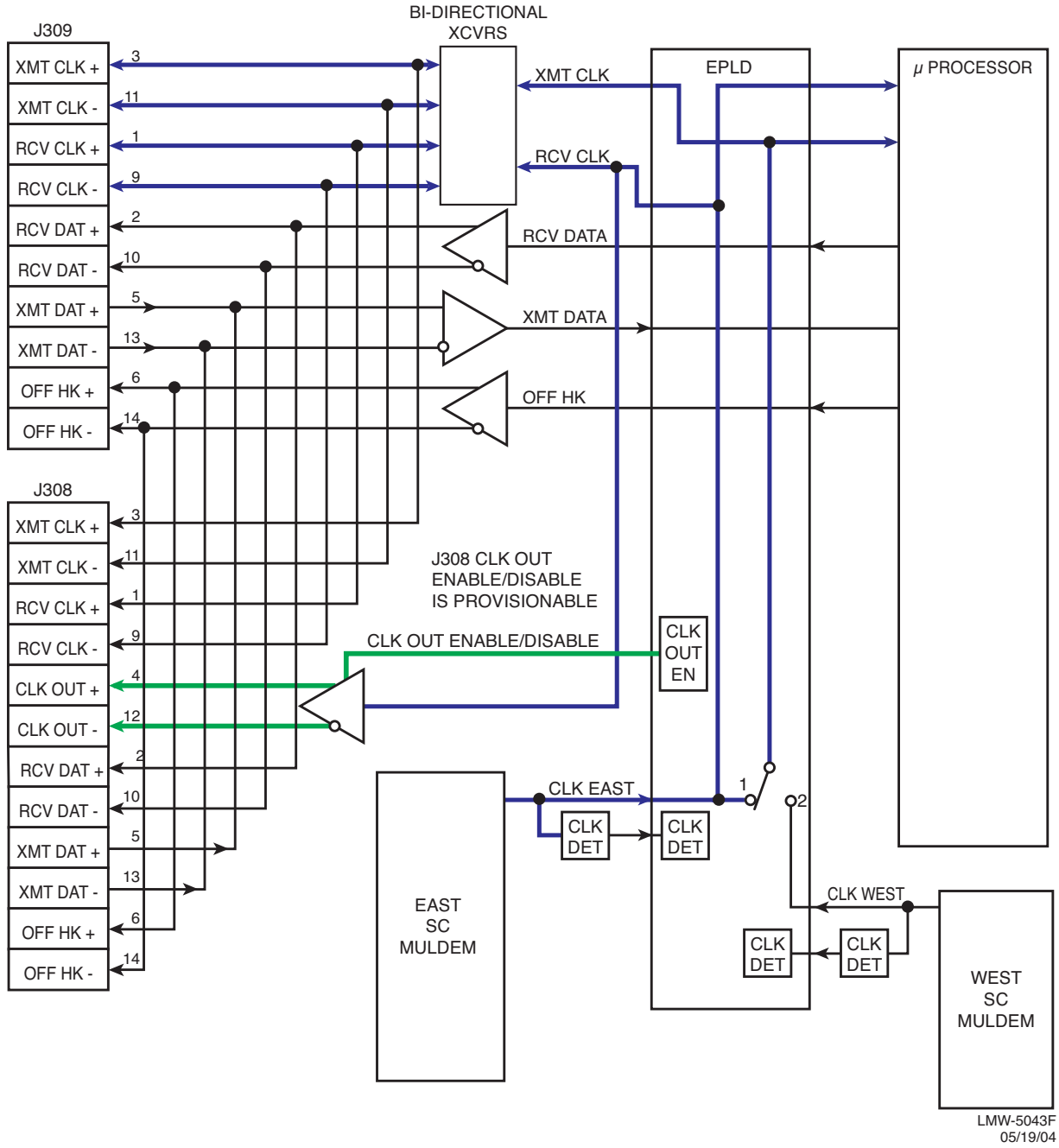

Figure 3-85 MCS-11 Port 4 Clock East Signal Flow

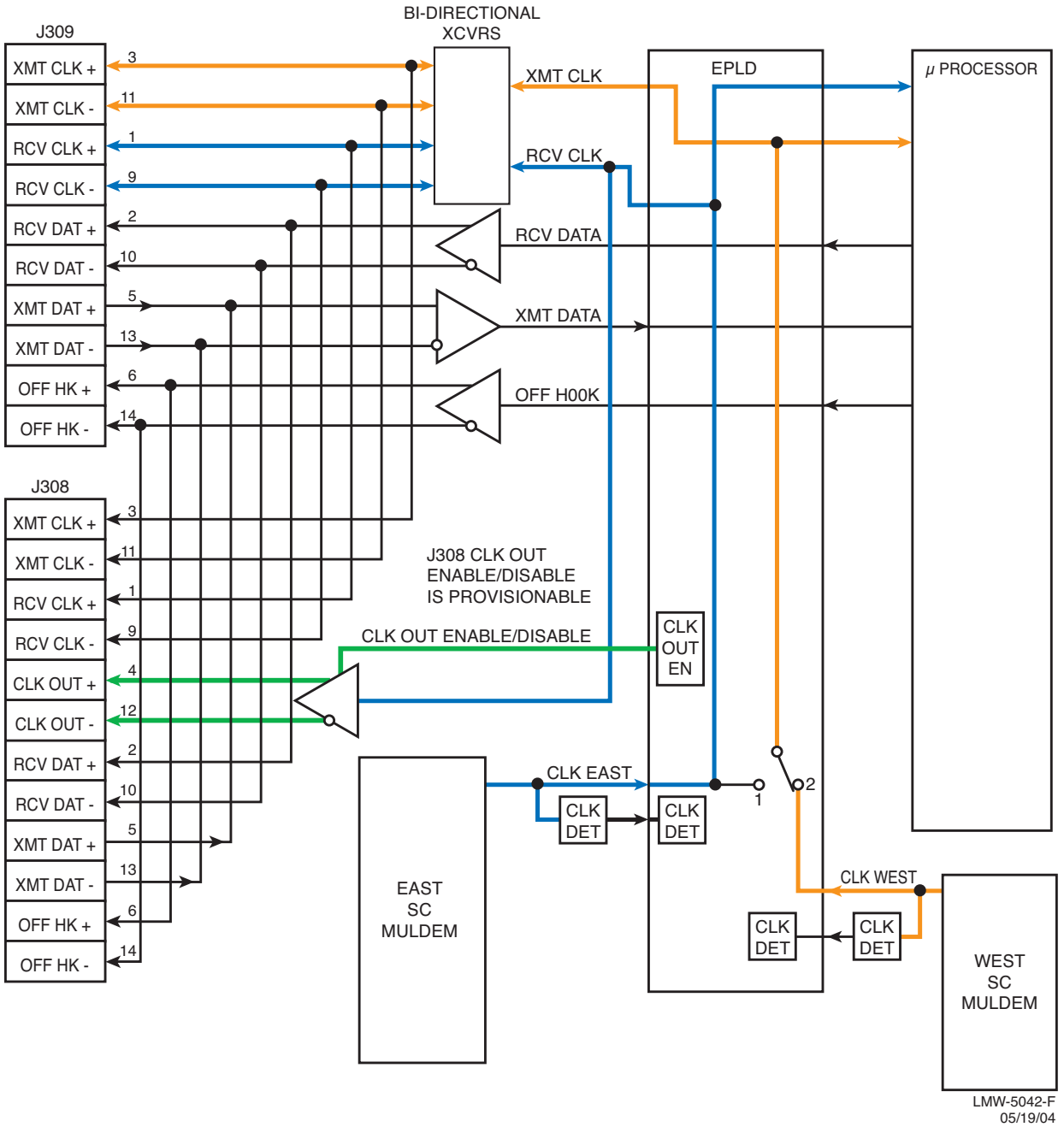

Figure 3-86 MCS-11 Port 4 Clock West Signal Flow

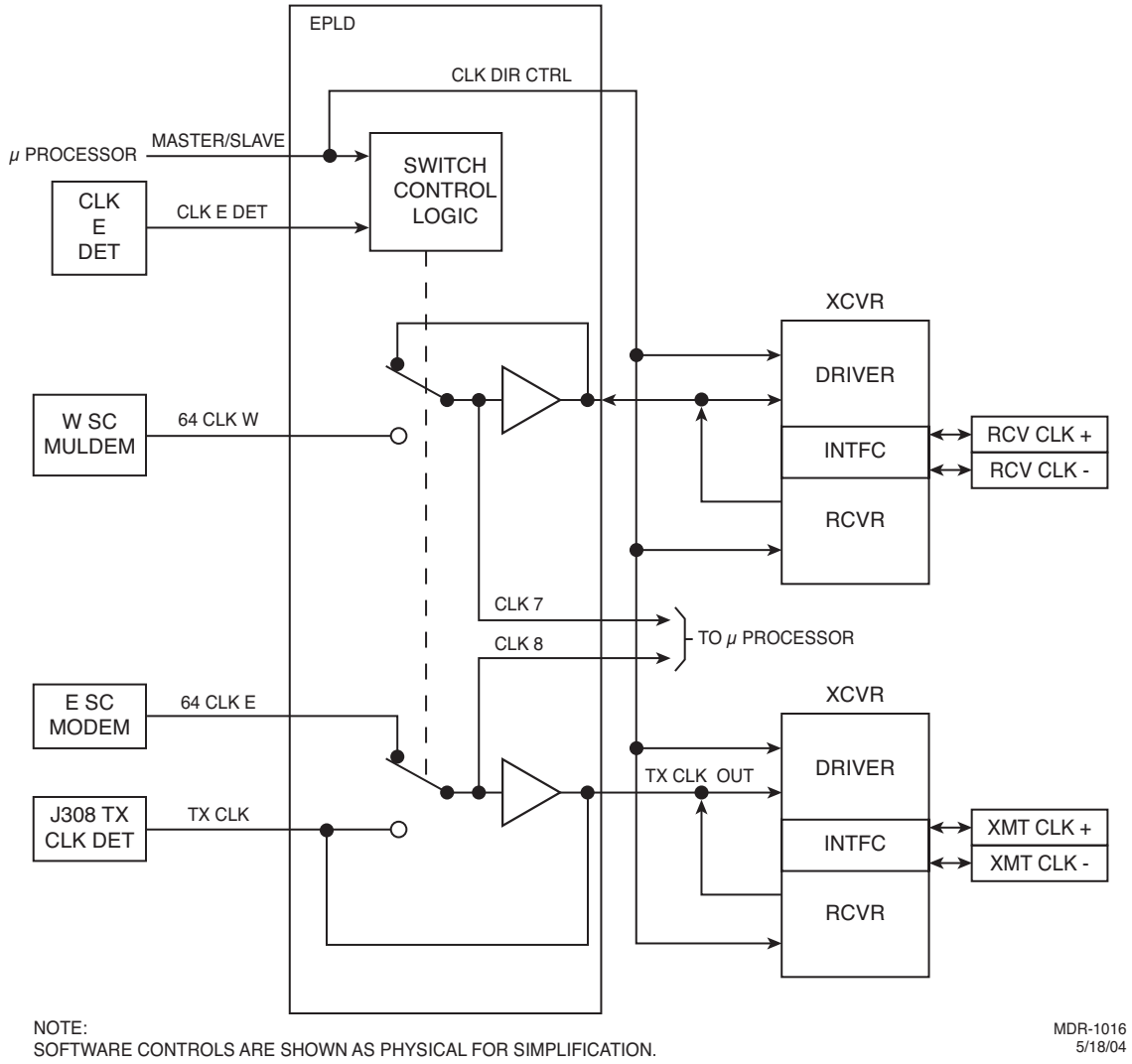

Figure 3-87 XMT and RCV CLK Direction Control

Termination relays are connected in parallel to the MCS( ) XT DT lines applied to the transceiver and, when activated, terminate the data in 120 ohms (approximately). The termination relays are provisionable on or off. Off is the default position. The termination relays are controlled by the MCS TERM control logic from the EPLD to the relay driver and MCS RLY control signal from the relay driver. In a daisy chain MCS scenario, the termination relay contacts should be provisioned open at all controllers except the end controller in the system, which is terminated through the closed contacts of the relay.

3.13.1.2.7 TBOS

The Telemetry byte oriented serial protocol (TBOS) fault alarm function is enabled by selecting displays 1-8 on the radio configuration provisioning screen. This enables the appropriate drivers on the controller and allows the user to view the external display on a PC. The four TBOS lines share pins on connector J305 with station alarm 13 through 16. TBOS to/from the controller or station alarm 13 through 16 to the relay interface are selected via provisioning. TBOS does not require the optional relay interface card. Refer to the Interconnect section for further details.

3.13.1.2.7.1 TBOS Termination

The TBOS termination function on the radio controller is not provisionable. The function is held in the off position by software.

3.13.1.2.8 Controller Alarm Relays

Three separate alarm outputs of the ESCC are applied to three relay drivers/relays. The relay outputs are connected to alarm/status connector J305 on the backplane. The relays are software controlled and two of the three relays share functions. The functions are selected through two provisioning options: major/minor or visual/audible.

3.13.1.2.8.1 Rack (Shelf) Alarm Relay

The rack (shelf) alarm relay is activated by any MDR-8000 alarm. When activated a ground is placed on J305-25.

3.13.1.2.8.2 Visual/Audible Alarms

The visual and audible alarm outputs are an extension of the rack (shelf) alarm. The applicable relays are activated by any MDR-8000 alarm. When activated, a ground is placed on J305-24 (visual alarm) and J305-50 (audible alarm). the audible alarm (only) can be cleared by setting the ACO/LT (alarm cutoff/lamp test) switch on the controller front panel to ACO. ACO will not cutoff the visual alarm. The fault causing the alarm must be cleared before the visual alarm is cleared.

3.13.1.2.8.3 Major Alarm Relay

The major alarm relay is activated by any service affecting alarm. When activated a ground is placed on J305-24. The fault causing the alarm must be cleared before the major alarm is cleared.

3.13.1.2.8.4 Minor Alarm Relay

The minor alarm is activated by any non service affecting alarm. When activated a ground is placed on J305-50. The fault causing the alarm must be cleared before the minor alarm is cleared.

3.13.1.2.9 Controller Interface With AE-27( ) Relay Interface Module

The controller sends relay controls and receives status to/from the AE-27( ) Relay Interface module via a serial data bus. Refer to AE-27( ) Relay Interface functional description in this section.

3.13.1.2.9.1 Shelf/Station Alarms

See Figure 3-88. Sixteen station alarm inputs to the relay interface module (J305) are applied to XCVRs in the relay interface and routed to the MCS and USI software functions over the serial data bus. Station alarm 1 and local rack alarm are OR'ed by a software OR function and an alarm on either input to the OR "gate" causes ann alarm output to the MCS-11 and USI. The rack alarm generated in the controller is also routed as a shelf alarm output to connector J305.

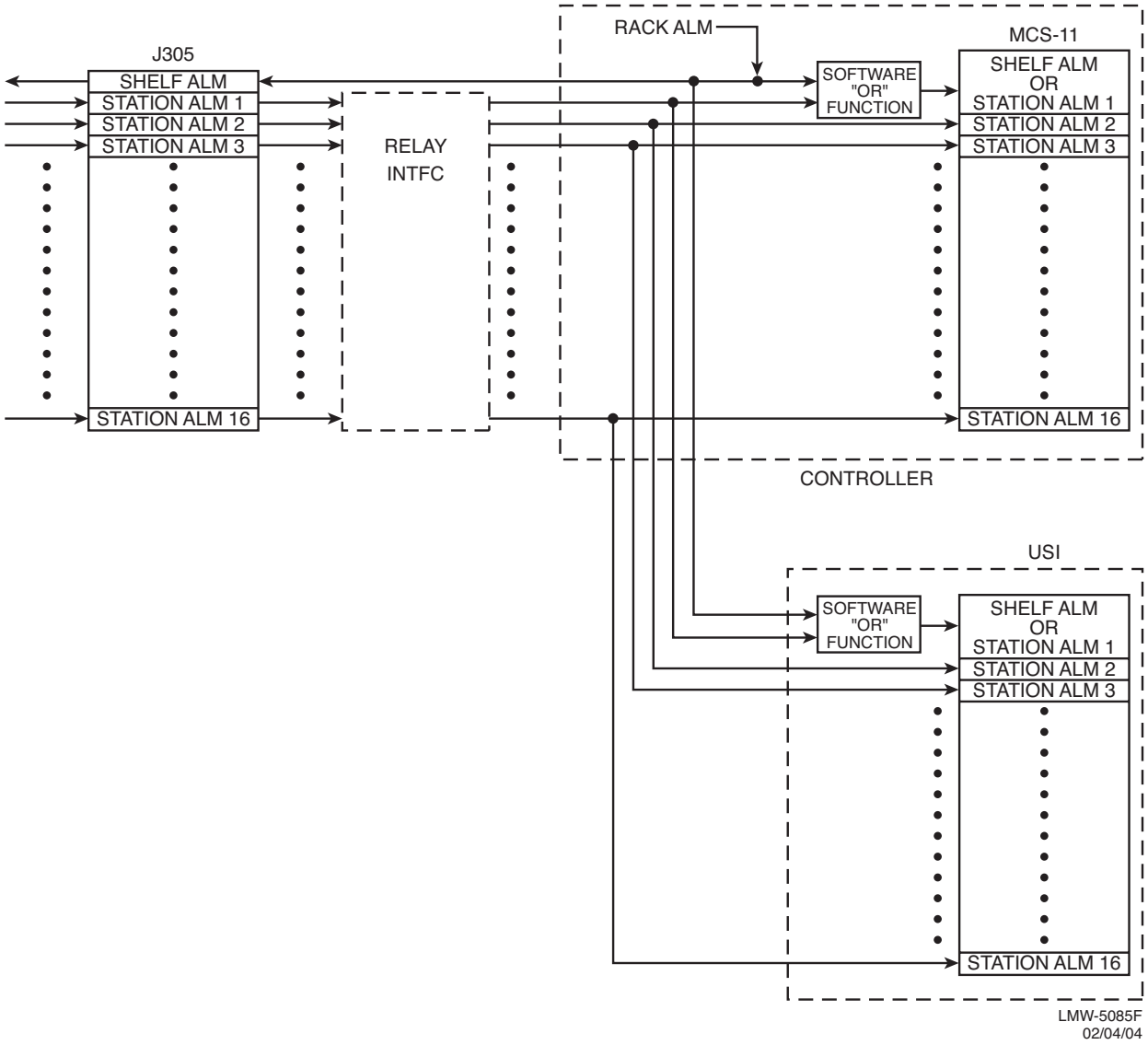

Figure 3-88 Shelf Alarm/Station Alarms 1-16 Signal Flow

3.13.1.2.10 Extended Link Monitor Channel Functions

The Extended Link Monitor Channel (ELMC) function allows provisioning, alarms, status information, and control commands for the local radio and alarms, status information, control commands for addressable remote radios as a standard feature. For remote provisioning and downloading capability, the ELMC option key (695-5647-018) must be installed on the AE-37Y Controller.

3.13.1.2.10.1 Timeout

ELMC timeout is a provisionable function that begins when the ELMC message is sent and ends when the response from the remote radio is received. If the response is not received during the provisioned time, a No Report is displayed on the USI screens. Timeout can be provisioned for up to 10 seconds. More time is needed for systems with more hops, since each radio processes the ELMC signal before sending it on. This individual processing of the signal creates delay.

3.13.1.2.10.2 ELMC Message Processing

Each radio decodes the address on the ELMC message and then if not addressed, sends the message out on its provisioned ports. If the radio is properly addressed, the ELMC message is processed and a response is sent.

3.13.1.2.10.3 ELMC Message

Each message begins with a request for provisioning so that the local radio knows how to paint the provisioning screens for the remote radio and communication with the remote radio is established. The message then requests information peculiar to the USI screen from which the address was entered. For example, if the user enters the remote address on the local status and alarm screen, a request for current alarms is sent to the remote radio. If the user enters the remote address on the local control screen, a request for current control status is sent to the remote radio. If the user enters the remote address on the provisioning screens, an acknowledge bit (keep alive signal) is sent to the remote radio. The remote radio responds with an acknowledge bit. No response to any request or acknowledge signal generates a No Report on the USI. A response after provisioned time-out time has elapsed also generates a No Report.

3.13.1.2.10.4 ELMC Termination

The ELMC termination function on the radio controller is not provisionable. The function is held in the off position by software.

3.13.1.2.11Service Channel Muldems

One EPLD functions as the west service channel muldem to provide multiplexing and demultiplexing between the XMT/RCV SC DATA W and the individual data channels. A second EPLD functions as the east service channel muldem to provide multiplexing and demultiplexing between the XMT/RCV SC DATA E and the individual data channels. The SC DATA signals consist of three 64 kb/s channels and one 16 kb/s channel. Multiplexing and demultiplexing occur in two directions. The eastbound data is received from the repeater rail data and sent to the I/O interface for transmission in radio rails. The westbound data is received from the radio rails and sent to the I/O interface for transmission in repeater rails.

The multiplexing circuits latch data from the 16 kb/s channel into a shift register, and shift the data out using a 64 kHz clock to create a 64 kHz channel. The data from this channel and three other 64 kHz channels are latched into another register and shifted out using a 256 kHz clock. A second set of shift registers is used to multiplex the off-hook so that the I/O interface only inserts XMT SC DATA from active channels.

The demultiplexing circuits clock the RCV SC DATA into a shift register using a 256 kHz clock and then latch the data using a 64 kHz clock to produce four 64 kb/s data streams. The data from the first channel is clocked into another shift register using a 64 kHz clock and the data is then latched using a 16 kHz clock.

3.13.1.2.12Register Data Bus

The register data bus interfaces the controller and OSS circuits. Transceiver chips provides bidirectional buffering of the register data bus. The register data bus drivers are enabled when CSF (channel select function) input is logic 0 and R/WF input is logic 1. Address decoding is used for serial chip selecting and for accessing OSS status/control registers.

3.13.1.2.13Serial Ports

Serial ports can be configured by the controller for asynchronous or synchronous operation using internal or external clocks.

One port provides 16 kb/s command path communication over the RF path and between repeater racks. The data is transported synchronously in the 16 kb/s auxiliary channels. Communication over these ports is stopped at the other end of the RF path or at the repeater rack.

3.13.1.2.13.1 RS-232 Data Ports

In the EPLDs functioning as E and W SC muldems, the RS-232 input data is converted to TTL and sampled at 64 kb/s. The sampled data is inverted and inserted into XMT SC DATA E and W and combined with the data already present in the channel. Data from TXD1 is inserted into channel 1 and data from TXD2 is inserted into channel 2. The receive data from RCV SC DATA E and W is converted to RS-232 levels. Data from channel 1 appears at RXD1 and data from channel 2 appears at RXD2.

3.13.1.2.13.2 RS-232 Bridge

Distribution of RS-232 data is controlled by the provisionable RS-232 bridging function. See Figure 3-89. The purpose of the bridging function is to control distribution of SC data in one direction (terminal) or two directions (repeater or back-to-back terminal).

3.13.1.2.13.3 Bridge Enabled

If the RS-232 bridge is provisioned enabled, the RS-232 input data is converted to TTL and sampled at 64 kb/s. The sampled data is applied to the SC muldem where it is inserted (INSERT E and W) into XMT SC DATA E and W and combined with THRU data already present in the channel. Data from TXD1 (J312) is inserted into channel 1 (shown in the figure), and data from TXD2 (J313) is inserted into channel 2 (not shown).

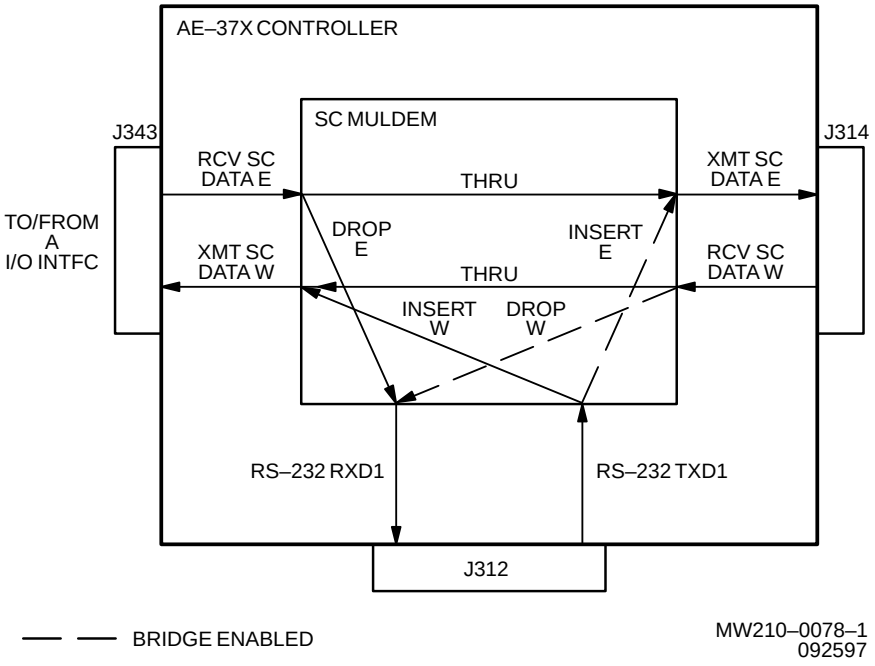

Figure 3-89 Bridge Function Simplified Functional Block Diagram

In the SC muldem, the receive data (DROP E and W) from RCV SC DATA E and W is combined and the output of the SC muldem is then converted to RS-232 levels. Data from channel 1 appears at RXD1 (J312), and data from channel 2 appears at RXD2 (J313).

3.13.1.2.13.4 Bridge Disabled

If the RS-232 bridge is provisioned disabled, insert data from TXD1 and TXD2 is added in the radio transmit direction (XMT SC DATA W) and dropped from the radio receive direction (RCV SC DATA E) only.

3.13.1.3 AUDIO CIRCUIT FUNCTIONS

See Figure 3-90. The AE-37( ) converts audio signals into the 64 kb/s digital data and in the reverse direction converts 64 kb/s digital data into audio signals. It uses pulse code modulation (PCM) to provide two independent audio channels (AUDIO 1 and 2). Audio interfaces are 4-wire and operate at either 0/0 dBm or +7/-16 dBm ratios with E&M lead signaling.

3.13.1.3.1 DTMF

The DTMF function allows signaling individually addressable terminal, repeater, and administration stations in the overhead channel system in the audio channel 1. An internal audio transducer sounds at the addressed station.

The DTMF provisioning option decodes DTMF signals for outgoing calls on the telephone. Push button 1 kHz signaling option is operational with or without the DTMF option. The 1 kHz signal is generated when the * key on the telephone keypad is pressed. Pressing the # key on the telephone concludes a DTMF call.

The DTMF generator output, the handset, the 4-wire E & M audio 1 input port, and the 1 kHz signal from the all-call signaling generator are summed and applied to the AUDIO 1 PCM Codecs for encoding (A/D conversion). The 64 kb/s XMT Data 1 E/W outputs are then sent to the service channel (SC) muldem for multiplexing. The DTMF generator output can be disconnected from the outgoing data by pressing the ***** key (cancelled all calls) on the external DTMF keypad.

3.13.1.3.2 PCM CODECS

The 64 kb/s Rcv Data 1 E/W from the OSS interface circuit function is received and applied to two PCM Codecs which decode the data and convert it to audio signals. There is a separate PCM codec for the East and West bound data directions. The decoded audio signals are fed to the DTMF detector, telephone, and 4-wire E & M lead interface for channel 1. The received audio signal is also looped back to the PCM Codec for insertion in the outgoing service channel 1, in order to provide party-line operations.

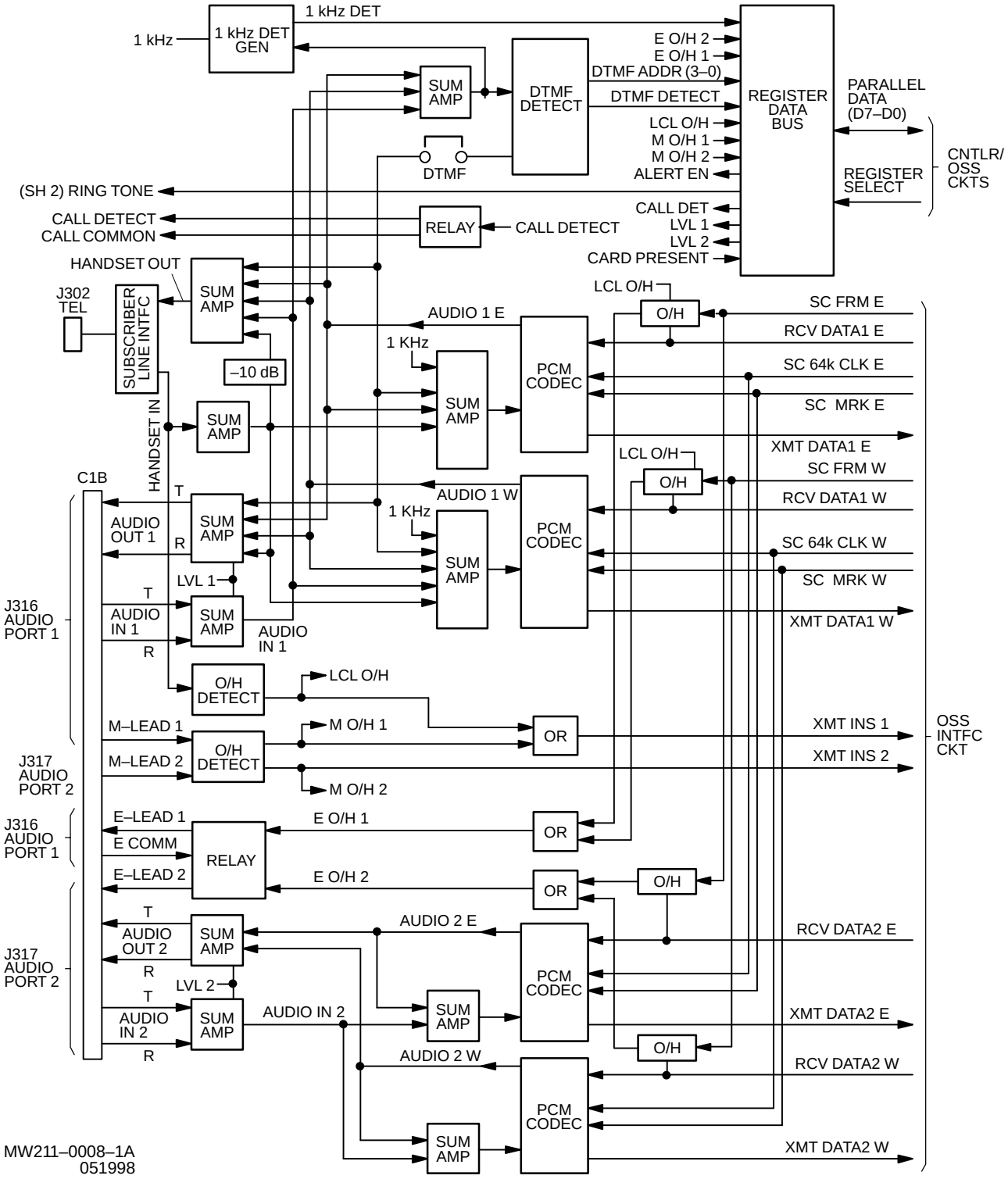

Figure 3-90 Audio Circuits Functional Block Diagram (Sheet 1 of 2)

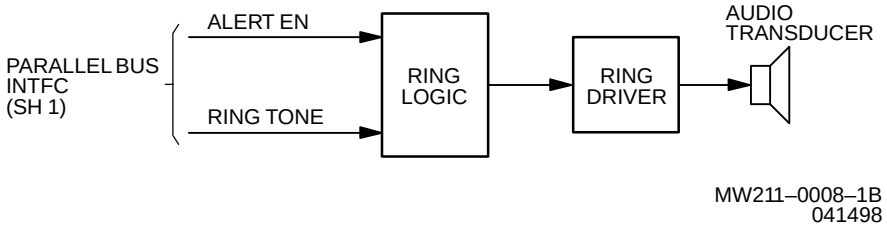

Figure 3-90 Audio Circuits Functional Block Diagram (Sheet 2 of 2)

3.13.1.3.3 Audio Timing

Three clock signals from the I/O interface are used to time the input and the output AUDIO 1 data. The 64 kHz clock is used to define the bit rate on the transmit and receive PCM highway. In the transmit PCM highway, data transitions occur on the rising edge of the 64 kHz . In the received PCM highway, data transitions occur on the falling edge of the 64 kHz. The 8 kHz clock is used to define the beginning of the transmit and receive time-slot on the PCM highway or marks the start of PCM word. The 8 kHz clock is synchronized with the 64kHz clock. The transmit words begin on the rising edge of the 8 kHz clock and the receive words begin on the falling edge of the 8 kHz clock. The 2 kHz clock is used to latch the off-hook signaling bit in the PCM data channel. The transmit off-hook is latched on the rising edge and the receive off-hook is latched on the falling edge.

3.13.1.3.4 Audio 2

The data on AUDIO 2 is processed identically to that of AUDIO 1 data except the audio port 2 provides the audio for the PCM codecs which interface with service channel 2E and service channel 2W. No speaker and handset are provided for AUDIO 2.

3.13.1.3.5 Local Off-Hook

The LCL O/H signal is OR'ed with M-Lead 1 to produce the XMT Ins 1 output to the OSS interface circuit function.

3.13.1.3.6 DTMF Function

The DTMF generator in the telephone generates dual-tone multi-frequency pairs required by the tone-dialing system. The DTMF detector contains the filter and decoder for detection of a pair of tones conforming to the DTMF standard. When the input to the DTMF detector matches the stored DTMF address, a CALL DETECT signal is produced by the microprocessor and a DTMF DETECT signal is sent to the parallel interface bus. The DTMF receiver is always actively enabled.

3.13.1.3.7 Parallel Interface

The parallel interface is used to receive provisioning information from the micro controller, such as the local DTMF address, the level adjustments for AUDIO 1 and AUDIO 2, alert enable, and call detect. The alert enable sets the warbler circuit, which causes the 1 kHz all call signaling tone to be modulated with 10 Hz. The information sent by the parallel interface to the controller circuit function includes Off/Hook from AUDIO 1 and 2 circuits, handset Off/Hook (local off-hook), 1 kHz detect, and DTMF digital outputs. A DTMF call detect signal is sent to the controller circuit when a DTMF address is received that matches the local address.

The input audio from the telephone is summed with the AUDIO 1 E/W PCM Codec inputs and output of audio port 1. The handset input is also sent to an off-hook circuit detector. Whether the off-hook detector detects an off-hook or on-hook depends on the handset input current.

3.13.1.3.8 Ringer Circuit

The audio transducer sounds any time the station is dialed. The ring logic is enabled by the ALERT EN signal from the microprocessor. The applied ALERT EN signal causes the 1 kHz RING TONE modulated by the 10 Hz ALERT EN signal to actuate the audio transducer.

3.13.2 AE-37AA TMN Interface

See Figure 3-91 for a functional block diagram of the AE-37AA TMN Interface module. The AE-37AA TMN Interface module consists of a main printed circuit board and the Power QUICC/Equipment Controller Radio Controller (PQ/ECRC) subboard. The Field Programmable Gate Array (FPGA), located on the main board, is the communications center of the TMN Interface. The PQ/ECRC subboard provides all microprocessor functions for the TMN Interface.

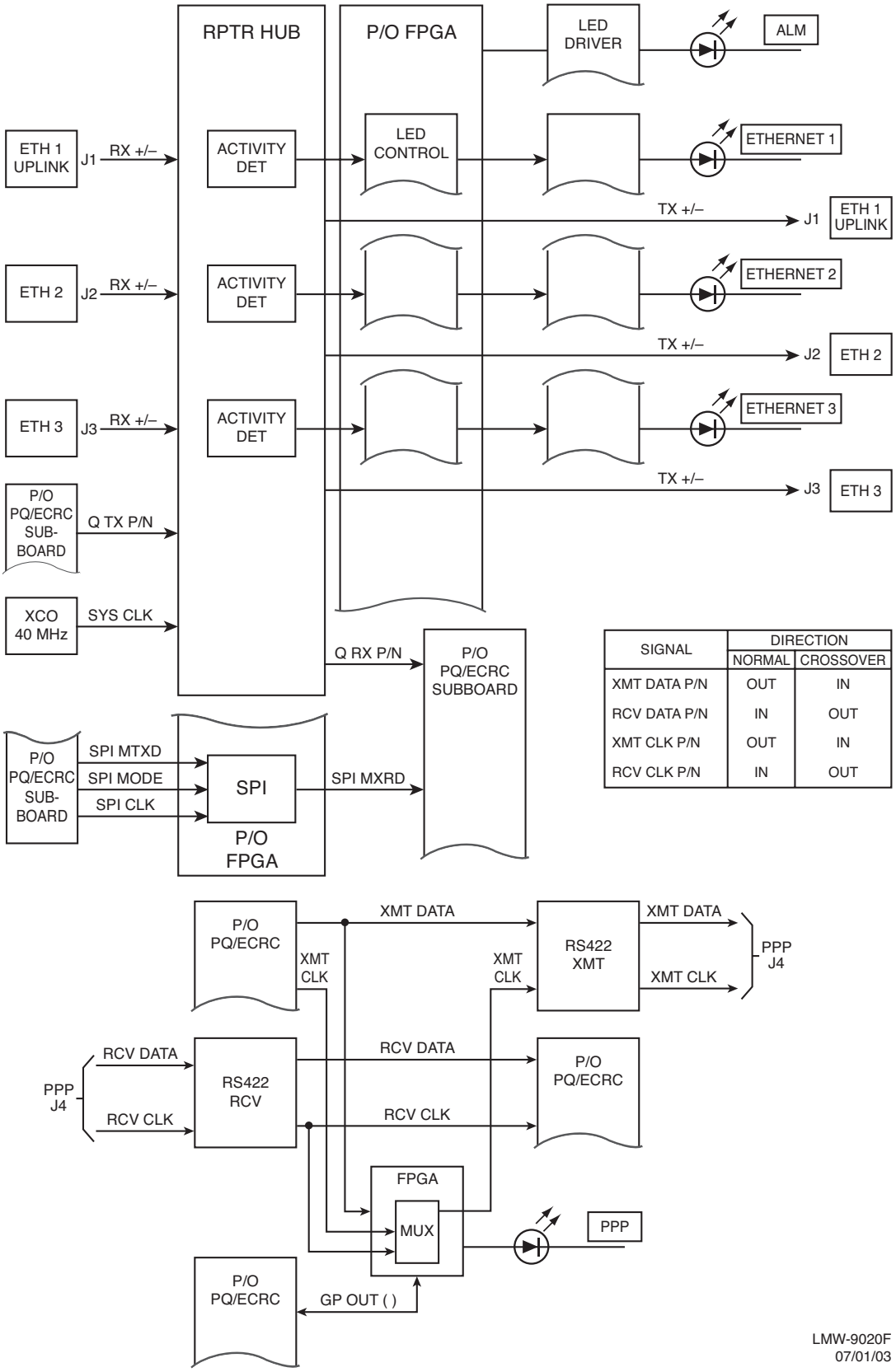

Figure 3-91 TMN Interface Module Functional Block Diagram (Sheet 1 of 2)

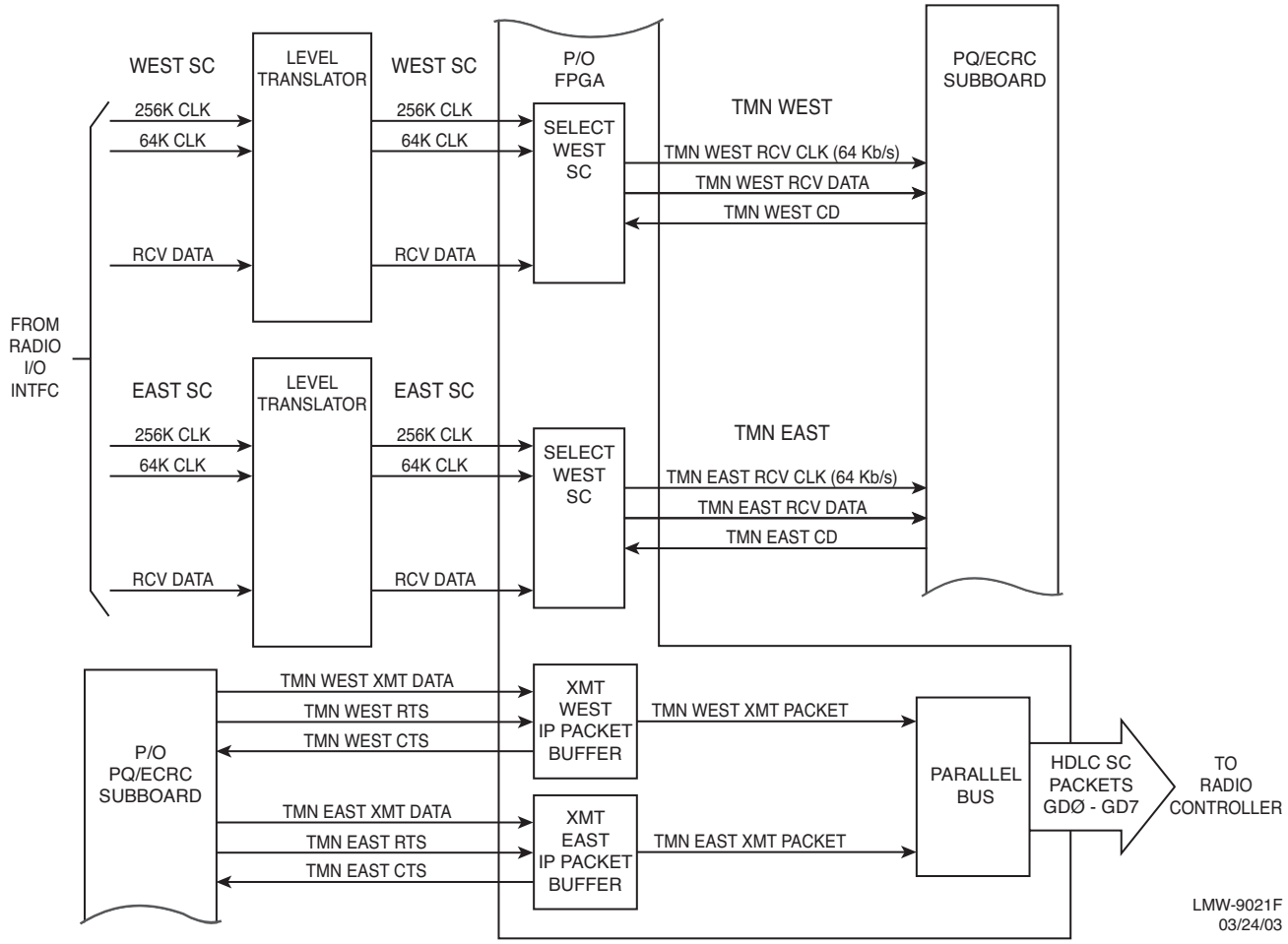

Figure 3-91 TMN Interface Module Functional Block Diagram (Sheet 2 of 2)

3.13.3 Repeater Hub

The repeater hub consists of four 10BASE-T transceivers and activity detectors/LED drivers. It provides four Ethernet ports. Three of the ports go to the front access RJ45 connectors, and the fourth goes to the PQ/ECRC subboard. Data received on any one input is repeated on the other three outputs. The data received on any one input is repeated on the other three outputs. The repeater hub uses the Q interface to communicate with the PQ/ECRC subboard. Inputs and outputs are transformer coupled for isolation and shaping.

The main functions of the repeater hub are data recovery and re-transmission, and collision detection propagation. Data packets received at the Ethernet ports are detected and recovered by the port receivers before being passed to the repeater core circuitry for re-timing and re-transmission. After recovery of a valid data packet, the repeater hub repeats the packet on the remaining ports, except the originator port. (i.e., data received on any one port is repeated on all remaining ports). Transmissions are controlled by collision detection circuitry that monitors the ports for collisions during simultaneous transmissions.

The repeating hub cannot receive simultaneously on more than one port (causes a collision). When a collision is detected, the collision detectors disable (jam) all ports. Any portion of a packet received on two ports will cause a collision.

3.13.4 PPP Interface

The PPP interface is a serial RS-422 logic-level compliant port accessible through an RJ45 connector on the main board. The port provides Transmit Data, Receive Data, Transmit Clock, and Receive Clock balanced signal pairs. Nominal impedance of balanced pairs is 100 ohms.

3.13.5 PPP Modes of Operation

The two modes of operation supported by the TMN interface include normal and crossover. Each mode provides both clock and direction control and clock mode control. The modes are controlled by software via control signals (GPOUT) from the PQ/ECRC subboard to the FPGA.

3.13.5.1 Normal Mode

See Figure 3-92. In the normal mode (default mode), the port mode is DCE, the data/clock follows normal directions (i.e. XMT data/clocks are outputs; RCV data/clocks are inputs), and the clock mode is internal (dual) clock. In the internal clock mode of operation, the XMT clock input to the MUX in the FPGA is passed to the XMT CLK output.

3.13.5.2 Crossover Mode

See Figure 3-93. In the crossover mode, the port mode is DTE, the data/clock follows opposite directions (i.e. XMT data/clocks are inputs; RCV data/clocks are outputs), and the clock mode is external clock. In the external clock mode of operation, the RCV clock input is looped to the XMT CLK output via the MUX in the FPGA. In this mode, the RCV CLK is also used to generate XMT data in the PQ/ECRC.

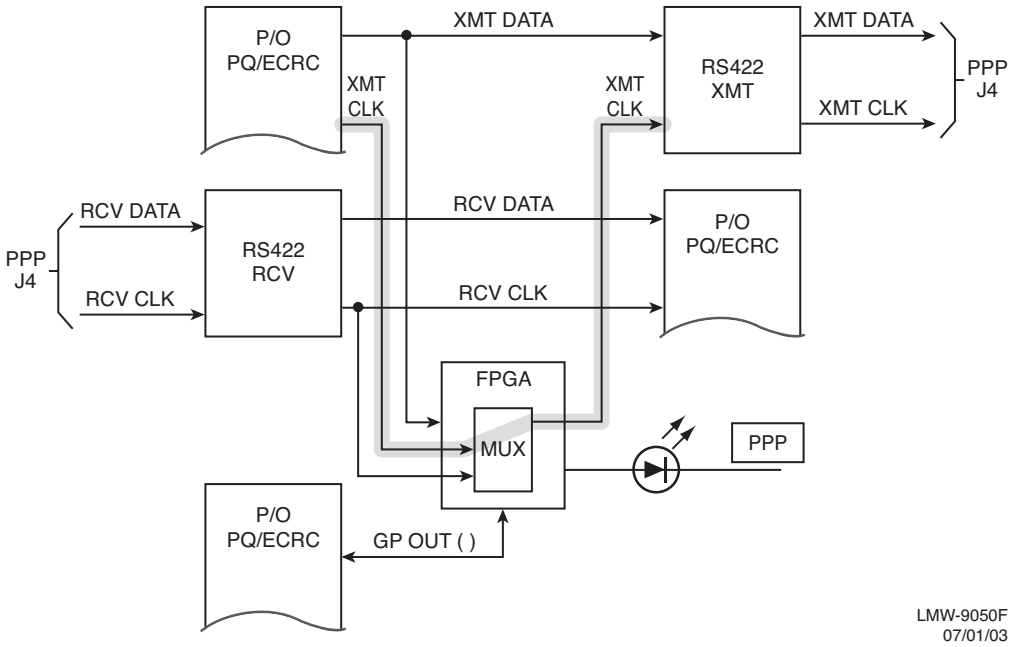

Figure 3-92 Normal Mode

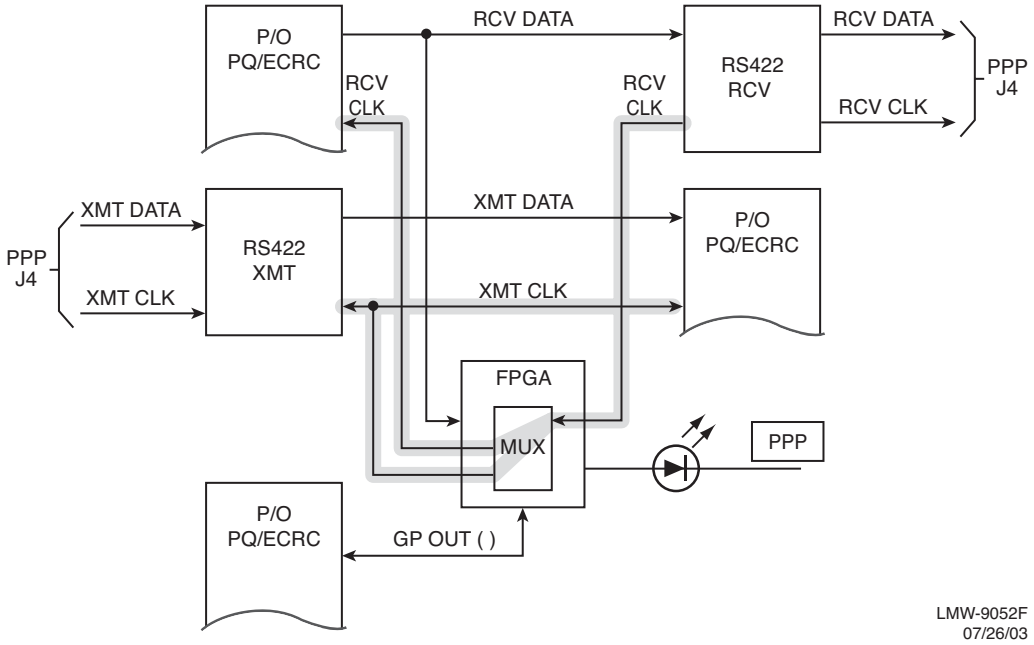

Figure 3-93 Crossover Mode

3.13.6 Front Panel Indicators

3.13.6.1 ALM LED

The red ALM alarm LED lights when the TMN interface fails and during reboot. The PQ/ECRC subboard asserts a PWRFAIL control signal (input to FPGA LED control circuit) when a power failure is detected, turning on the red LED. While reboot is in progress, the ALARM_LED output from the FPGA LED control circuit is asserted, turning on the red ALM LED.

Note

The term active *is used to identify an established link. A link can be active and receiving data or active and receiving idle signals at the port. An inactive link is a link that has not been established and there is no communication between local and farend.*

3.13.6.2 Ethernet 1-3 LEDs

Each of the three Ethernet ports (ETHERNET 1, 2, and 3) contains a bi-color LED indicator: green is used for link status and yellow is for error on the port. An activity detector in the repeater hub monitors each Ethernet input and provides a Link Status and RX Packet output to the FPGA LED control circuit. When activity is detected, the LED control circuits in the FPGA send an output to the LED, through the LED driver, causing the LED to light (or blink). Refer to Table 3-8.

3.13.6.3 PPP LED

The PPP port J4 contains a bi-color LED indicator: green is used for link status and yellow is used for error on the port. The PQ/ECRC subboard asserts a GPOUT( ) control signal (LINK ACTIVE input to FPGA LED control circuit) when the link has been established through the PPP port J4, turning on the green PPP LED. The FPGA monitors both the XMT and RCV data lines to determine activity and idle states. Activity is identified by data characters on the channel. Idle, or absence of data, is identified by a special set of characters hereafter called *idle signal*.

Note

The color green always indicates an active link. The color yellow always indicates an inactive link. Regardless of color, a blinking LED always indicates the associated port is receiving data.

Table 3-8 Front Panel Indicators

LED	COLOR	STATE	INDICATION
ALM	Red	Steady	Module fault. also lights for the duration of reboot and then goes off.
ETHERNET 1-3	Green	Steady	Link is active but no data is being received
ETHERNET 1-3	Green	Blinking	Link is active and receiving data packets on ports J1-J3.
ETHERNET 1-3	Yellow	Steady	Link is not active and port J1-J3 is misconfigured.
ETHERNET 1-3	Yellow	Blinking	Link is not active and collisions are being detected.
PPP	Green	Steady	Link is active.
PPP	Green	Blinking	Link is active and receiving data packets on port J4
PPP	Yellow	Steady	Link is not active and idle signals are being received on port J4.
PPP	Yellow	Blinking	Link is not active but data is being received on port J4.

3.13.7 LAN IP Transport

The TMN East and TMN West serial interfaces from the PQ/ECRC subboard interface directly with the FPGA and indirectly with the radio controller for LAN IP transmission.

3.13.7.1 IP Transmit

The TMN East and TMN West XMT channels are independent. Each XMT channel consists of an IP packet buffer that received inputs from the PQ/ECRC subboard and outputs to the parallel interface. Data flow is controlled by the radio controller software interface. Data flow is controlled by the radio controller software and via Ready To Send (RTS) and Clear To Send (CTS) control signals between the radio controller, the FPGA, and the PQ/ECRC subboard. The PQ/ECRC subboard sets the RTS signal when data is ready for transfer to the

FPGA. The radio controller sets the CTS signal to let the PQ/ECRC subboard know it has not finished reading the previous packet. The IP packet buffers in the FPGA will not accept new data until the radio controller signifies it has finished. When the radio controller has finished reading the previous packet, the data to be transmitted is accepted as an HDLC framed packet into the FPGA IP packet buffer. The FPGA removes the HDLC start and stop bytes and the remaining packet data is stored in the IP packet buffer. After the data in the packet is stored in the IP packet buffer, the FPGA sets the CTS signal to stop data transfer from the PQ/ECRC and inform the radio controller that data is waiting to be read.

3.13.7.2 IP Receive

TMN East and TMN West RCV channels are decoded directly from the 256 kb/s overhead stream by the FPGA. The 64 kb/s channel to be decoded is selected by provisioning. The selected channel can be 1, 3, or 3. Channel 0 is reserved for ELMC and cannot be used. When enabled, the East and West 64 kb/s overhead stream is output, with clock, to the TMN East and TMN West RCV inputs on the PQ/ECRC subboard. The FPGA monitors the 256 kb/s and 64 kb/s clock inputs from the level translators for activity. The FPGA sets the TMN West Carrier Detect (CD) signal and/or East CD signal to inform the PQ/ECRC subboard that it is actively decoding the 256 kb/s overhead channel.

3.13.8 Craft Port (F Interface)

The Craft interface is a serial RS-232 DCE-compliant port accessible through a DB9 Female connector (J5) on the front panel. The Craft port provides a local interface for connecting craft terminals such as the Java craft interface. Connections are implemented as PPP over the serial interface. The craft port provides local access to provision the TMN Interface function as a low end NE manager as well as download new software and FPGA releases. Supports asynchronous, full duplex 8 data bits, 1 stop bit, odd parity, 38400 bps nominal.

3.13.8.1 TMN Activity Indicators

The TMN port will provide two LEDs, one to indicate Link Status and another to indicate RX data activity. Collisions will jam on the RX LED for all active interfaces for approximately one second.

3.13.9 FPGA

The FPGA provides access to the Radio Backplane Parallel Bus to communicate with the Radio Controller. The Parallel Bus consists of an 8-bit data bus and a 10-bit address bus that are used for all communication to the MDR-8000, including transmit access to the 64kb transport service channel. For receiving the 64kb transport service channel, the FPGA directly demultiplexes channel from the 256kb/s Radio overhead. On the TMN Interface side, there are three main interfaces, SPI Bus, TMN_E and TMN_W. The SPI bus is used for general alarm and messaging. The TMN_E and TMN_W interfaces are used to interface to the East and West service channels.

Messages are passed between the TMN Interface and the Radio Controller using a combination of registers and 6kBytes of RAM in the SNMP FPGA. The RAM is divided into six buffers of fixed sizes of 512 and 2048 bytes. The RAM buffers are accessed indirectly through registers using only 256 bytes of address space. The FPGA also directly accepts serial HDLC Framed IP data for transport from the TMN_E and TMN_W ports and writes it directly into the TX East and West IP Packet Buffers. Demultiplexed Receive Service channel data is not buffered and is passed on directly to the TMN_E and TMN_W receive ports.

3.13.10 SPI Interface

The SPI bus is used to configure the FPGA upon initialization and to access registers in the FPGA to pass alarm and control messages to and from the FPGA. The SPI interface is controlled by the host processor on the PQ/ECRC subboard. The MODE signal is used to detect the occurrence of a communication phase. During the communication phase, data is transferred on the interface as 8-bit packets. The first pair of packets received after the assertion of MODE are the command packets. These packets are followed by the data packets. Packets from the PQ/ECRC subboard are received on the MTXD input and echoed back to the PQ/ECRC subboard on the MRXD output to check the received data.

3.13.11 PQ/ECRC Subboard

See Figure 3-94 for a functional block diagram of the PQ/ECRC subboard. The heart of the TMN Interface module is the PQ/ECRC processor card. It is a 50MHz MPC86OT processor with 16Mb RAM. Non-volatile storage is provided by a Compact Flash card. The interface to the motherboard is through two 64 pin connectors. The available interfaces provided are a General PIO interface (16 bit output, 16 bit input), SPI bus, TMN_RF, TMN_E, TMN_W, Ethernet, RS-232 craft, RS-232 debug, JTAG and 12C. The card runs the PSOS operating system. The operating system provides the TCP/IP stack as well as support for the Agent software, and routing of TCP packets through the LAN and TMN interfaces.

3.13.11.1 Clock Generation and Distribution

The system clock is generated and controlled by the 24.576 MHz oscillator and clock buffer circuits.

3.13.11.2 Boot Memory

The boot memory consists of a 2 MByte flash EPROM memory bank and is used to store the program code (firmware) that will take the CPU control after the board reset.

3.13.11.3 System RAM

The system RAM consists of two SDRAMs and is used for both program op codes and data items.

3.13.11.4 Compact Flash Card

The Compact Flash card is a mass memory device used for storage of program executable files for the processor and for logging alarm event reports, performance monitor data, and other data.

3.13.11.5 F Interface (Craft port)

The F interface is used to support the craft terminal function for operation, administration, and maintenance. Refer to description of Craft port.

3.13.11.6 SPI Bus

Used to access RAM in the FPGA to pass messages to and from the Radio Controller.

3.13.11.7 TMN Interfaces

TMN_E and TMN_W ports are used for transporting (TMN) LAN traffic to the Radio Controller via the FPGA for insertion into the East and West overhead streams. The TMN_RF port is connected to the front accessible PP interface to allow connections to external equipment.

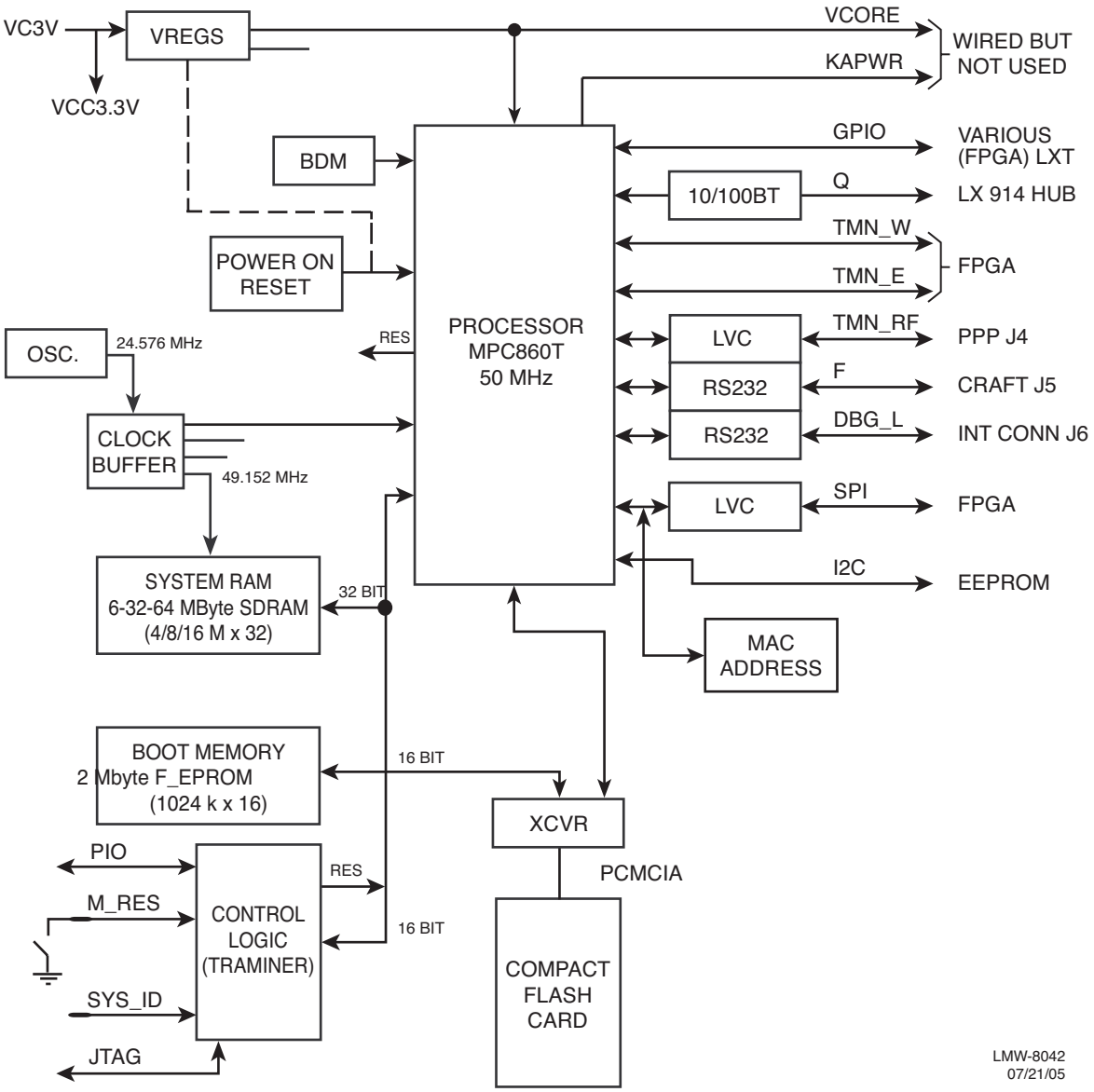

Figure 3-94 PQ/ECRC Subboard Functional Block Diagram

3.13.11.8 Ethernet

The Ethernet port connects to an internal interface of the Ethernet Bridge in the TMN Interface. It provides local LAN access.

3.13.11.9 JTAG

Used to change the programming of the Traminer on the PQ/ECRC board. Is connected in series with the serial EEPROM and FPGA.

3.13.11.10 I^2C

To allow the PQ/ECRC board to access the Motherboard I^2C Inventory EEPROM.

3.13.11.11 Controller Alarm

A single Red LED will be used to indicate boot/fault in the PQ/ECRC Controller. The LED displays a constant RED during bootup and when there is a fault. The PQ/ECRC subboard provides the signal to drive this LED.

3.14 SOFTWARE FUNCTIONAL DESCRIPTION

See Figure 3-95 for a software functional block diagram. The NE SNMP Adaptation Module (NSAM) is the NE peculiar software module used to map NE specific data into the MIB.

3.14.1 TMBN Interface Module Software Modules

3.14.1.1 NSAM

The NE SNMP Adaptation Module (NSAM) is the NE software module that contains the software used to map NE specific data into the format required by the SGPA. The NSAM is loaded from the flash card.

3.14.1.2 SGPA

The SNMP Generic Program Agent (SGPA) is the software module that contains the software used to map data into the MIB. The SGPA software is the same for all NEs. The SGPA is loaded from the flash card.

3.14.1.3 Router

The router is the software module that contains the software used to distribute data between the craft interface, Ethernet, PPP, serial TMNs and SGPA software modules. The router is loaded from the flash card.

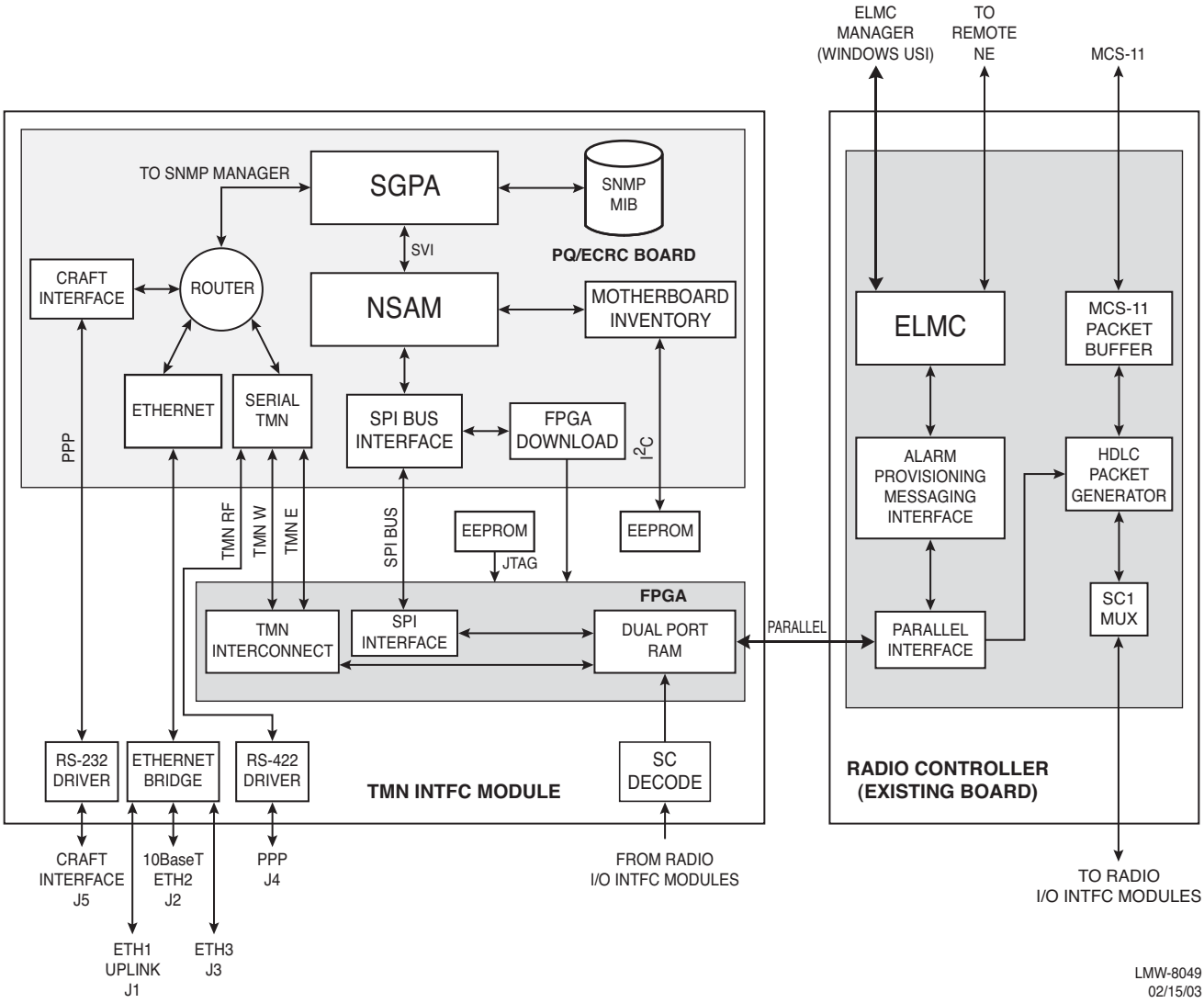

Figure 3-95 Software Functional Block Diagram

3.14.1.4 SNMP MIB

The SNMP MIB is the database that contains the information on the NE used to interpret events. The SGPA MIB is loaded from the flash card.

3.14.1.5 Ethernet

Ethernet is the software module that contains the software used to distribute data to/from the ETH1 Uplink, ETH2, and ETH3 connectors from/to the router software module.

3.14.1.6 Serial TMN

Serial TMN is the software module that contains the software used to distribute data (TMN RF) to/from the PPP connector and data (TMN E and TMN W) to/from the FPGA TMN interconnect software module from/to the router software module.

3.14.1.7 Craft Interface

The Craft interface is the software module that contains the software used to distribute data to/from the Craft interface connector, via the RS-232 driver, from/to the router software module.

3.14.1.8 SPI Bus Interface

The Serial Peripheral Interface (SPI) bus interface is the software module that contains the software used to distribute programming data to/from the FPGA SPI interface software module and to/from the NSAM.

3.14.1.9 FPGA

The FPGA is loaded at power-up by the serial EEPROM. The EEPROM is initially programmed via the JTAG port. At power-up, the FPGA initiates a download to itself from the EEPROM.

3.14.2 Controller Module Software Modules

3.14.2.1 ELMC

The ELMC software module contains the software used to interface the radio windows USI to the alarm provisioning message interface software module. This allows the radio to send and receive alarms/provisioning data to/from remote NEs over the service channel. If the message is addressed to this radio controller, the response is returned over the same port as received. Otherwise the incoming message is retransmitted over the remaining three ports.

3.14.2.2 Alarm Provisioning Messaging Interface

The Alarm Provisioning Messaging interface software module contains the software used to receive and respond to alarm and/or provisioning status requests from/to the TMN Interface module and/or the ELMC.

3.14.2.3 Parallel Interface

The Parallel Interface software module manages all communication between the TMN interface and the radio controller. The interface software stores, reads, and distributes incoming and outgoing messages between the TMN interface and the radio controller. This interface also locks and unlocks the reception/transmission capability between the TMN interface and the radio controller, limiting reception and transmission to no more than one message at a time.

- Transport SNMP data to/from the controller, over the parallel bus on the radio backplane, from/to the FPGA dual port RAM on the TMN interface module.
- Route SNMP data received on the parallel bus to the HDLC packet generator.

3.14.2.4 MCS-11 Packet Buffer

The MCS-11 Packet Buffer (really an interface) software module contains the software used to receive and transmit MCS-11 messages. If the received message is for this radio, the message is sent out the RF and repeater ports. Otherwise, it is sent out the asynch ports.

3.14.2.5 HDLC Packet Interface

The HDLC Packet Interface software module contains the software used to control incoming and outgoing HDLC encoded messages. An incoming receive message is decoded to determine if it is PPP or MCS-11. If PPP, it is discarded since PPP received messages also arrive and are acted on in the TMN Interface module. If the message is for MCS-11, the HDLC header is stripped and the MCS-11 message is sent to the MCS-11 Packet Buffer for further processing. If the incoming MCS-11 or PPP message is for transmission, it is HDLC encoded and transmitted to the Service Channel MUX for transmission to the Radio I/O Interface Modules.

3.14.3 Power Supplies

The available power from the backplane is 12.0V. Switching supplies are used to generate the required 3.3V and limited 5.0V needed by the TMN Interface module. The input to the switching supplies are 'C' sourced from the A and B sources. Power for the FPGA core is provided by a 5.0V to 2.5V linear regulator.

3.14.4 AE-27( ) Relay Interface

See Figure 3-96 for application diagram. See Figure 3-97 for functional block diagram. The AE-27( ) Relay Interface receives control, alarm, and status inputs and provides alarm, status and control relay outputs. All output relays can be disabled or provisioned normally open or normally closed as follows:

Normally open (NO) – relays are normally de-energized and relay contacts are open. When activated, relays are energized. Relay contacts close, connecting the output to ground.

Normally closed (NC) – relays are normally energized and relay contacts are closed and grounded. When activated, relay contacts are de-energized. Relay contacts open, presenting an open (high impedance) to the output.

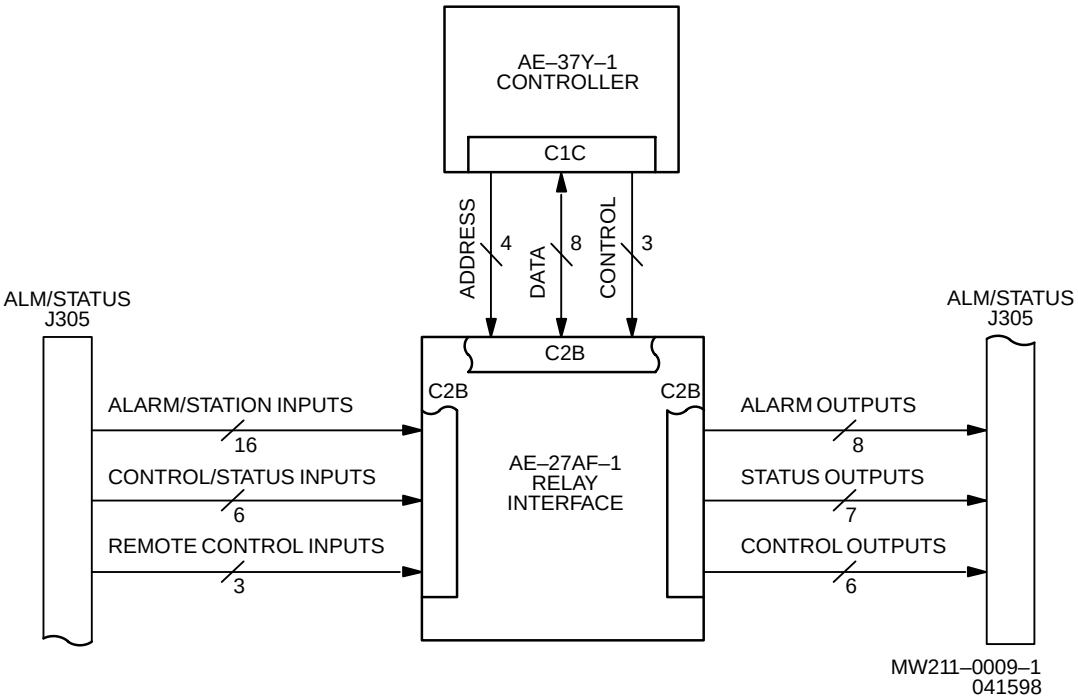

Figure 3-96 AE-27( ) Relay Interface Interconnect Diagram

3.14.4.1 Controller Bus

The Relay Interface communicates with the AE-37( ) Controller card via the processor bus and the data bus. The processor bus, consisting of three address lines, two control lines, and a clock, is applied to a XCVR. The data bus contains the eight data line (D0-D7) is applied to a separate transceiver. Interface with the relay transceivers is provided by the XCVR data bus. When commanded by the AE-37( ) Controller, the decoder/DEMUX decodes and demultiplexes the address and enables the appropriate relay XCVR via the EN2-9 controls. The controller can then write alarm/status/control information to the relay XCVRs, or read alarm/status/control inputs from the relay XCVRs. Further descriptions of the controller interface signals follow:

- Address lines A0 through A3 – HCMOS inputs. 100K Ohm pull-ups. Used by address decoders to enable output registers and input buffers.
- Buffered bidirectional data lines D0 through D7 – HCMOS input/outputs. 10K Ohm pull-ups. Used to write data to output registers and read present bits or data from input buffers.
- ECLK – 2 MHz bus clock. HCMOS input. 100K Ohm pull-up.
- R/WF Read/Write False. HCMOS input. 100K Ohm pull-up. A logic 1 indicates data is being read from an input buffer or the present bits. A logic 0 indicates data is being written to an output register.
- Relay Intfc CSF – Relay Interface Card Select False. HCMOS input. 100K Ohm pull-up. Chip select for relay interface card. Active low.

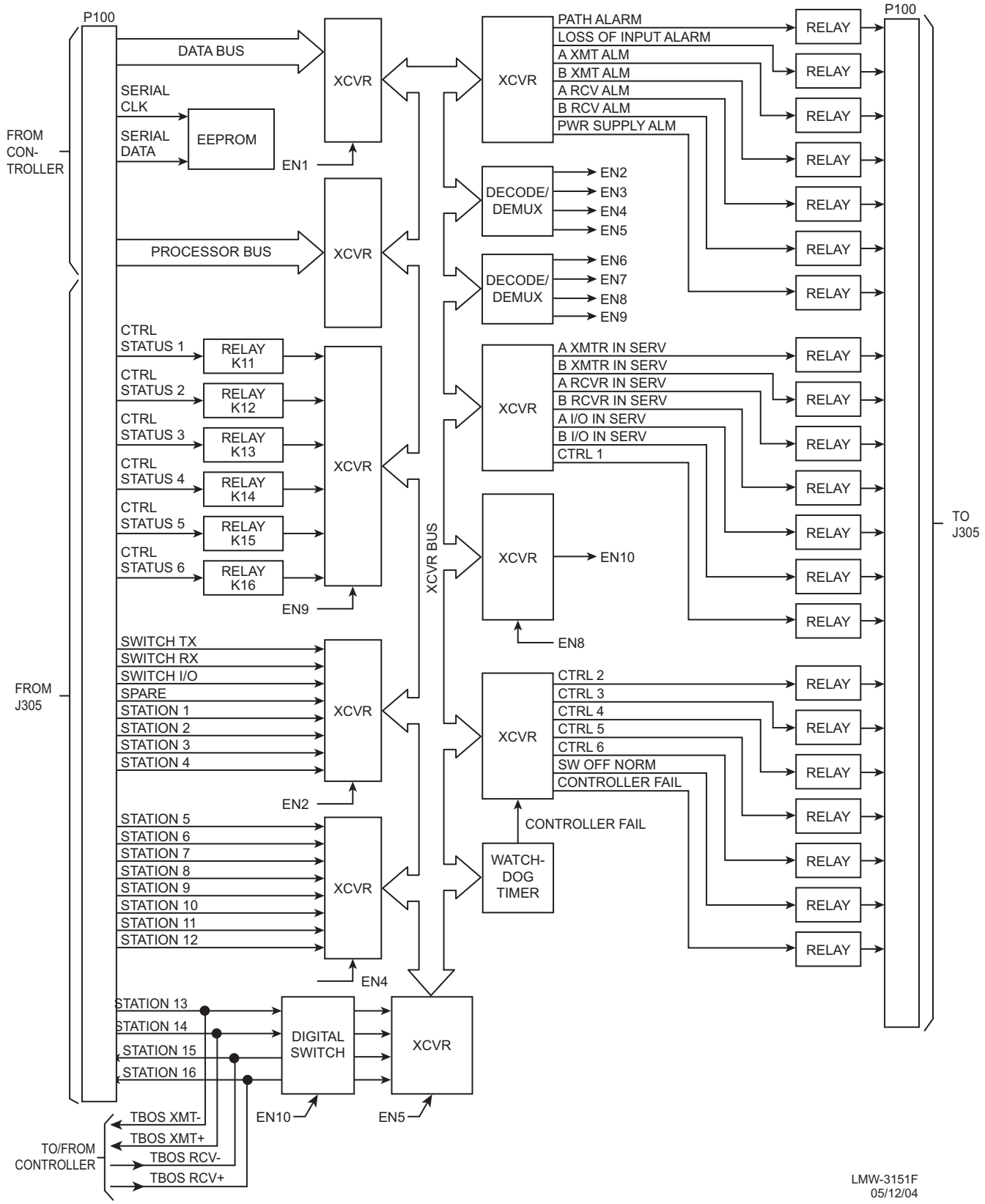

Figure 3-97 AE-27( ) Relay Interface Functional Block Diagram

3.14.4.2 Control Inputs

Nine buffered control inputs are provided. The inputs are diode protected from voltages outside of the 0 to +5 V range, and have a 10K Ohm resistor for current limiting purposes. In addition, each input has a 100K Ohm pull-up resistor.

- Switch Transmitter (SWITCH TX) – buffered HCMOS input, sends signal to controller module to activate the transmitter that is currently not carrying traffic.
- Switch Receiver (Switch RX) – buffered HCMOS input, sends signal to controller module to activate the receiver that is currently not carrying traffic.
- Switch I/O Interface (SWITCH I/O) – buffered HCMOS input, sends signal to controller module to activate the stand-by I/O interface module.

3.14.4.3 Station Alarm / Status Inputs

Station alarm/status inputs are provisionable for MCS-11 and/or TBOS alarm systems. When the radio fault alarm is provisioned **Station Alarm 13-16**, sixteen station alarm/status input signals (STATION 1 THROUGH STATION16) are reported in MCS-11 station responses. When the radio fault alarm is provisioned **TBOS Display 1-8**, the STATION 13-16 inputs are replaced by four TBOS lines.

The alarm/status input signals are buffered HCMOS inputs, diode protected from voltages outside of the 0 to +5 V range, with10K ohm current limiting (series) resistor and 100K ohm pull-up resistor. A logic 0 indicates an alarm state. A logic 1 (or open) indicates a non-alarm state.

3.14.4.4 Relay Alarm / Status Outputs

Note

Alarm / status not designated for a particular type of radio are applicable to all radio types (DS1 / E1, DS3, and OC3 / STM-1).

Eight alarm relay outputs and seven status relay outputs provide relay closure to ground (provisioned NO) or open (provisioned NC) when activated. All relays default to open if card power is lost, except the Power Supply alarms, which default to ground. The maximum contact rating for each relay is 0.5 A, 100 V. The alarm/status relay outputs are:

- Alarms:
    - Path Alarm – This summary alarm is activated by the following alarms:

      A/B Path Distortion

      A/B AGC Threshold
    - Loss of Input Alarm – This summary alarm is activated by the following alarms:

      Loss of DS3 input

      Loss of DS1/E1 input

Loss of wayside DS1 input

- A XMT – A-side transmitter failure. This summary alarm is activated by any of the following alarms (Table 3-9) on the A side:

  XMT SYNC Alarm

  RF Power Alarm

  Common Loss Alarm

ATPC Timeout

MUX Input Loss Alarm

- B XMT – B-side transmitter failure. This summary alarm is activated by any of the following alarms (Table 3-9) on the B side:

  XMT SYNC Alarm

  RF Power Alarm

  Common Loss Alarm

  ATPC Timeout

  MUX Input Loss Alarm

- A RCV – B-side receiver failure. This summary alarm is activated by any of the following alarms (Table 3-9) on the A side:

  Channel Alarm

  RCV Frame Loss

  Eye Closure

  RSL Alarm

- B RCV – B-side receiver failure. This summary alarm is activated by any of the following alarms (Table 3-9) on the B side:

  Channel Alarm

  RCV Frame Loss

  Eye Closure

  RSL Alarm

- PWR Supply Alarm – This summary alarm is activated by any A or B power supply failure.
- Controller Fail – relay is activated if a card select has not been detected in the previous approximately 200 msec.
- Status:

- A XMTR In Service – A-side transmitter module is on-line.
- B XMTR In Service – B-side transmitter module is on-line.
- A RCVR In Service – A-side receiver module is on-line.
- B RCVR In Service – B-side receiver module is on-line.
- A I/O In Service – A-side I/O interface module is on-line.
- B I/O In Service – B-side I/O interface module is on-line.
- Switch Off Normal – Click on OFF NORM LED on USI Status Alarm screen to view message. Indicates manual control enabled or one of following conditions exists:

OFF NORMAL MESSAGE DISPLAYED ON USI STATUS ALARM SCREEN:

A/B Side PA Off – PA ON/OFF switch on A or B power supply is set to OFF.

A/B Side LIO SPI Fail – XMT or RCV circuit failure on Low Capacity I/O ASIC in A or B DS1 I/O interface module.

A/B Side RCV SPI Fail – Failure on the Serial Processor Interface bus causing loss of communication between the controller and RCV circuits on the I/O interface module.

A/B Side DS1 SPI Fail – Failure on the Serial Processor Interface bus causing loss of communication between the controller and DS1 interface circuits on the I/O interface module.

Fan Alarm – Failure of one or more cooling fans or failure of the fan control module on the fan assembly.

IO Loopback On – I/O LOOPBACK function is enabled on USI control screen on DS1 radio.

DS1 Line 1-16 Loopback On – DS1 LINE LOOPBACK RCV to XMT 1-16 function is enabled on USI control screen on DS3 radio.

DS1 Line 1-4 Loopback On – DS1 LINE LOOPBACK RCV to XMT 1-4 function is enabled on USI control screen on DS3 radio.

A/B RCV Prov. ERROR UNIRCV – Failure in communication between processor on controller and UNIRCV ASIC on DS3 I/O interface module.

A/B DS1 Prov. ERROR LEGHORN – Failure in communication between processor on controller and Leghorn ASIC on I/O interface module.

OFF NORMAL MESSAGE DISPLAYED ON USI STATUS ALARM SCREEN (CONT):

A/B ATPC LOW POWER LOCK – A or B Automatic Transmit Power Control low power lock function is enabled on USI control screen on DS1, DS3, or OC3/STM-1 radio. Lock prevents ATPC from going high.

A/B ATPC HIGH POWER LOCK – A or B Automatic Transmit Power Control high power lock function is enabled on USI control screen on DS1, DS3, or OC3/STM-1 radio. Lock prevents ATPC from going low.

EEPROM PROV DOES NOT MATCH MODULE PROV – Stored provisioning in controller memory does not match provisioning stored in module memory.

XMTR Capacity Key Mismatch – Part numbers of capacity keys on A and B XMTRs are different.

RCVR Capacity Key Mismatch – Part numbers of capacity keys on A and B RCVRs are different.

A/B Tx OVERRIDE – A or B XMTR has been switched and locked in-service using controls on the front panel of the controller module. Online XMTR will not switch out-of-service regardless of alarms.

A/B Rx OVERRIDE – A or B RCVR has been switched and locked in-service using controls on the front panel of the controller module. Online RCVR will not switch out-of-service regardless of alarms.

A/B I/O OVERRIDE – A or B I/O interface has been switched and locked in-service using controls on the front panel of the controller module. Online I/O will not switch out-of-service regardless of alarms.

3.14.4.5 Relay Control Outputs

Note

Control outputs and control status inputs operate together to perform control functions. The control status inputs to the relay interface must be properly wired to the external equipment that is being controlled by the associated control output in order to display the ON or OFF status on the USI control screen. Without the control status inputs, the control function on the USI screen will still turn on equipment/functions, but no status will be indicated and, once turned on, the equipment/function cannot be turned off.

Six relay control outputs (CTRL 1-6) provide relay closure to ground (provisioned NO) or open (provisioned NC) when activated. These relays default to open if card power is lost. The maximum contact rating for each relay is 0.5 A, 100 V.

3.14.4.6 Control Status Inputs

Nine buffered status inputs (CTRL STATUS 1-6) from the equipment controlled by the CTRL 1-6 outputs, verifying the controlled function. The inputs are diode protected from voltages outside of the 0 to +5 V range, and have a 10K ohm resistor for current limiting purposes. In addition, each input has a 100K Ohm pull-up resistor.

3.14.4.7 Remote Inventory Function

The 256 X 8 bit EEPROM stores inventory information that is read by the AE-37Y Controller when the remote inventory function is initiated using the USI screens. Inventory data including part number, software revision, type number, and hardware revision are stored in the non-volatile memory.

3.14.4.8 Watchdog Timer (WDT)

If the software is unable to toggle a watchdog circuit clear bit every 70 ms, a hardware watchdog timer resets the module. The circuit is a dual one-shot whose first stage is constantly retriggered every 70 ms to prevent a pulse from being sent to the second stage. Failure of the clear bit to toggle in time after an initial pulse is received causes the second stage to fire and reset the module.

Table 3-9 Alarms

ALARM	FUNCTION
Controller	This alarm indicates a failure in the controller microprocessor operation.
Off Normal (COM)	This alarm is generated by the receive interface, controller switches, or USI computer control functions. It indicates a switch or control is not in the normal position.
MUX Input Loss (COM)	Indicates loss of input signal or inability to recover clock on the alarmed line. May also indicate detection of bipolar violations.
RF Power (TX)	Indicates loss of transmit signal detected at output stage of power amplifier.
Common Loss (TX)	Common Loss Alarm (CLA) is generally an indication of a silent failure (no alarm activated) at the transmitter. The common loss alarm, generated by the AE-37Y Controller, triggers when both A-side and B-side downstream receivers have a radio frame loss or channel failure. In a hot-standby hop, loss of both receivers initiates a request to switch to the standby transmitter, even though no transmit alarms are present. If the path is nominal, the transmitter switches in 5 seconds. If the path is in a fade (ATPC is in active range), the transmitter switches in 30 seconds. If the downstream alarms clear within 5 seconds, a CLA is initiated on the off-line side to indicate a silent transmit failure. If alarms still exist, the transmitter continues to switch at the provisioned rate. This process continues until the receive alarms clear, but no CLA is activated.
APC Timeout (TX)	Indicates ATPC has been active for 5 minutes without returning to normal (only if ATPC has been enabled with timeout).
Channel Alarm (RX)	Indicates loss of signal lock in receive interface. May be due to loss of RX signal or LO off frequency.
RSL Alarm (RX)	Indicates low RSL on alarmed receiver.
Eye Closure (RX)	This alarm usually indicates a degraded signal.
RCV Frm Loss (RX)	Indicates loss of receive radio frame in I/O interface.
DEMUX Alarm (RX)	Indicates loss of receive clock, buffer spills, or alarm insertion signal on the alarmed line. May also be caused by DS1 driver failure.

3.15 POWER DISTRIBUTION

See Figure 3-98. Power is supplied to the basic radio at the backplane. Primary power is ±20.5 to ±60 Vdc. The CE-16BB Power Supplies have floating +/- power inputs that allow for positive or negative ground operation. Strapping on the backplane allows for positive or negative ground connection. Primary power protection for the Power Supply is provided by a 20 amp input fuse.

The power supply converts ±20.5 to ±60 Vdc power from the battery to +10.5, +12, -12, and -5 Vdc outputs. The power supply provides + and -12 Vdc operating power to all modules except the power amplifier and provides +10.5 and -5 Vdc outputs to the power amplifier.

3.15.1 Hot-Standby

In the hot-standby configuration, the A power supply supplies the operating voltage for the AE-37Y Controller, AE-27AF Relay Interface, and the A-side modules. The B power supply supplies the operating voltage for the AE-37Y Controller, AE-27AF Relay Interface, and B-side modules.

3.15.2 Input Power Protection

Input power protection circuits protect the power supply against improper input power, improper input power wiring, and improper module removal and installation.

3.15.2.1 Input Power Wiring Protection

The potential on the +BATT input (J1/J2-1) must be more positive (higher) than the potential on the -BATT input (J1/J2-3) to prevent blowing the input fuses. Since the power supply is floating, and either a positive voltage or round is more positive than the -BATT input, either input is acceptable for normal operation. The input diode(s) on the power supply module provide protection for a wiring error causing reverse input potential.

3.15.2.2 Module Removal / Installation Protection

Hall effect switches on the module insertion and removal tabs prevent the power supply module from being removed or installed with power outputs enabled.

3.15.3 C-Sourced Output Drivers

See Figure 3-99 for block diagram. In the A and B I/O Interface modules, +5 Vdc is developed from the +12 Vdc inputs. In each module, the +5 Vdc is applied to one side of an OR gate and is sent to the other I/O interface module via the backplane. The other side of the OR gate is supplied by the +5 Vdc from the opposite I/O interface. The internally generated +5 Vdc and the +5 Vdc from the other I/O interface module are diode OR'ed to drive the MUX and DEMUX output line drivers. This protects the outputs if power is lost to either the A or B side. During normal operation the higher +5 Vdc is predominate.

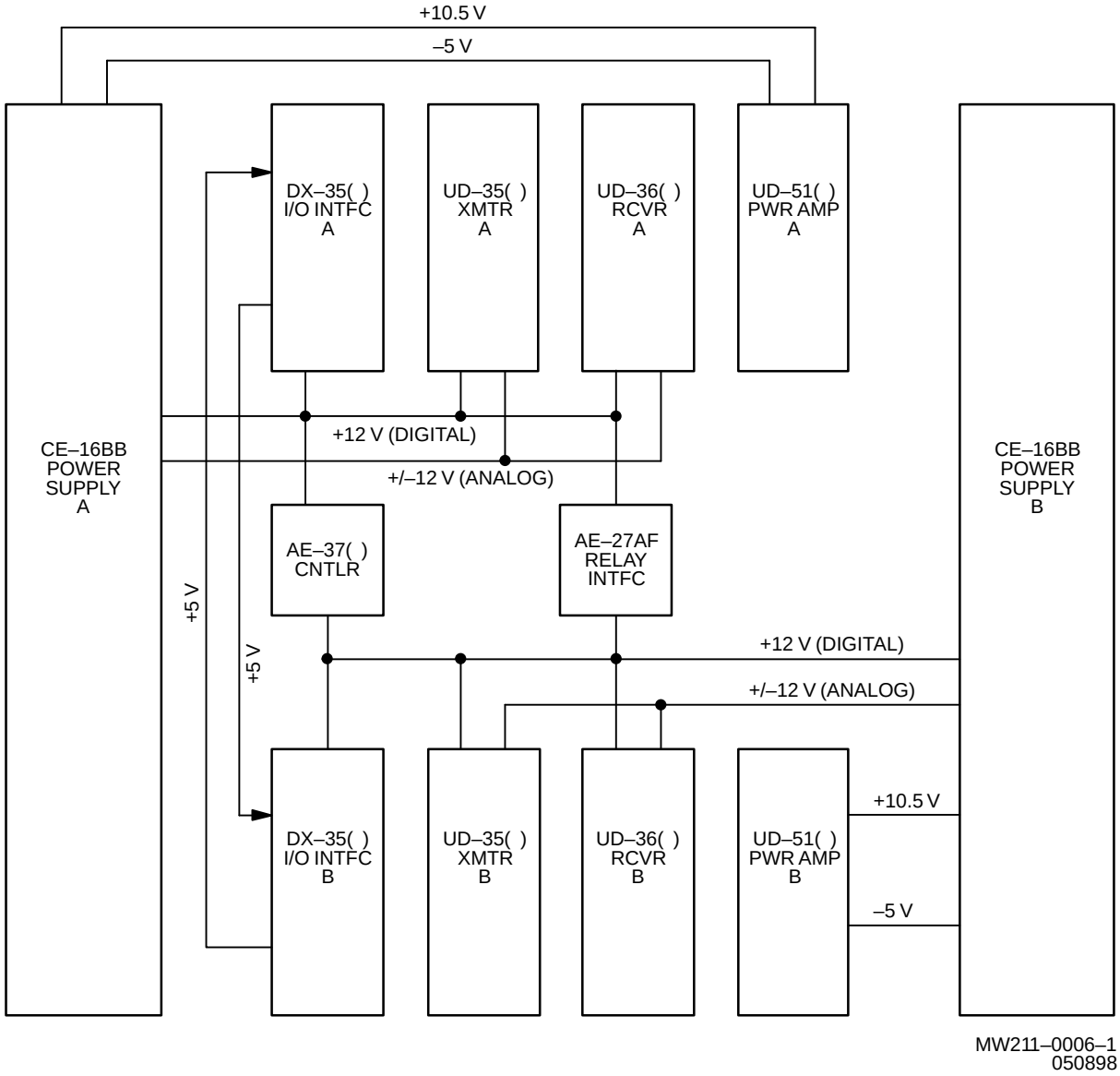

Figure 3-98 Power Distribution Block Diagram

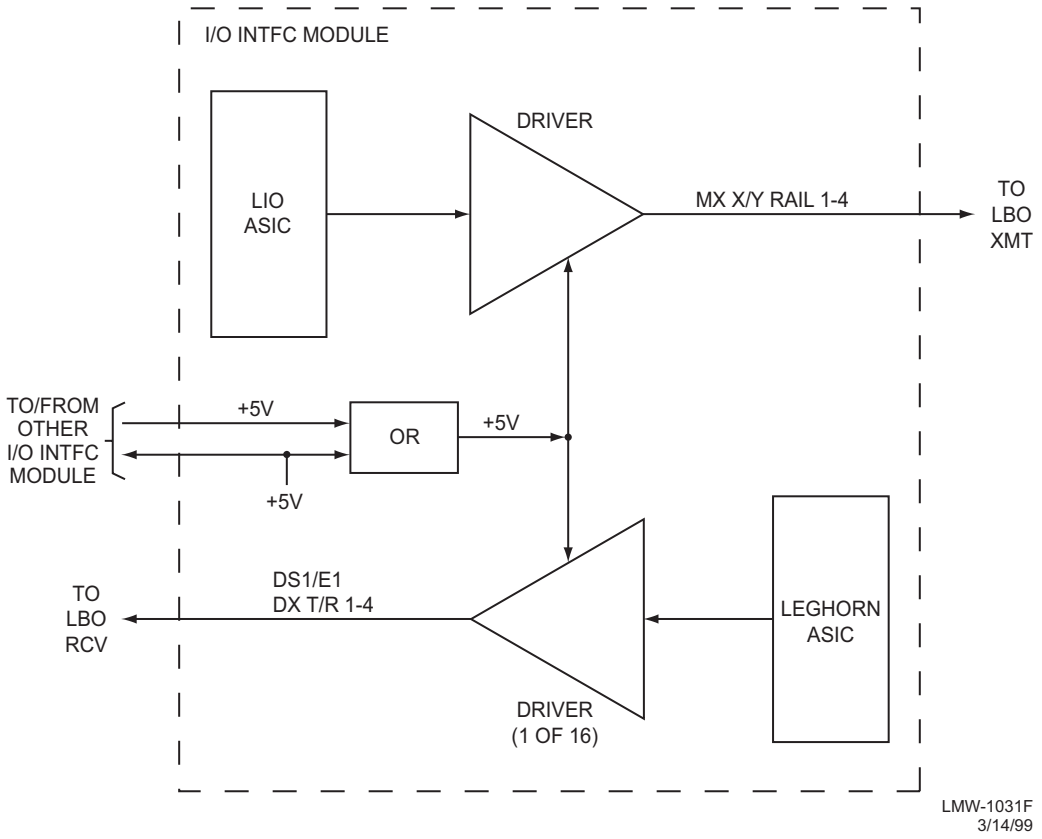

Figure 3-99 C-Source Power to I/O Interface Output Drivers

3.15.4 CE-16BB Power Supply

The CE-16BB Power Supply is a switched-mode supply that provides multiple, regulated outputs from a semiregulated 20.5 to 60 Vdc battery source (Figure 3-101). Regulated output voltages of +10.5, +12, -12 and -5 Vdc are provided with overload and overvoltage protection on all the regulated outputs. Front panel indicators are provided for module alarm and switch off normal status. An alarm is provided for an under voltage condition on any output, a loss of primary power, or a blown fuse. A serial I^2C interface to a 256 byte serial EEPROM is provided for inventory control.

3.15.4.1 Configurations

There are currently four versions of the CD-16BB Power Supply. All have the same part number and functions are identical, with different designs to meet the same design requirements. Alcatel originally designed and manufactured the power supplies that are now being supplied to Alcatel. See Figure 3-100 for the CE-16BB Power Supply interconnect diagram. See Figure 3-101 for a typical functional block diagram.

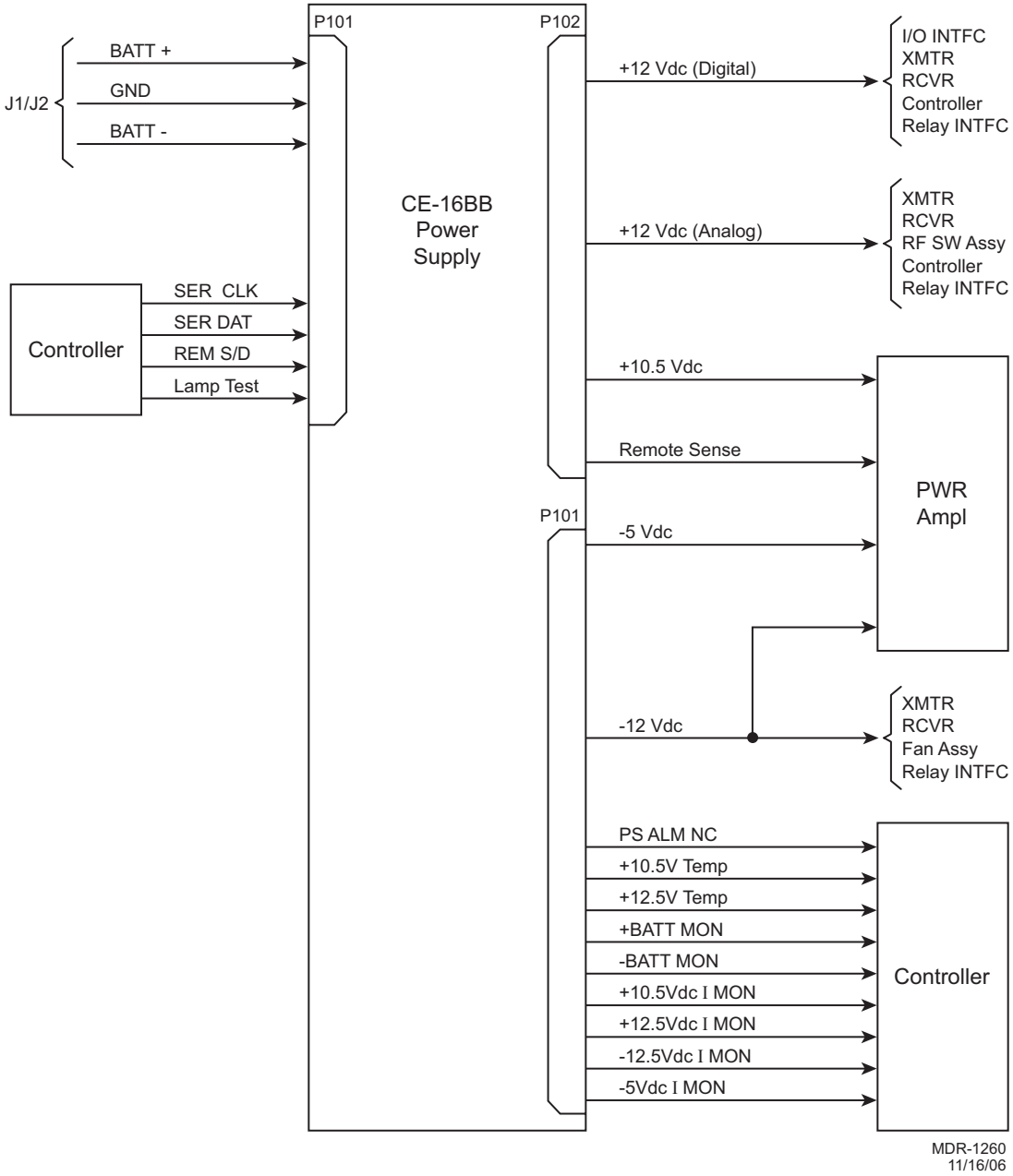

Figure 3-100 CE-16BB Power Supply Interconnect Diagram

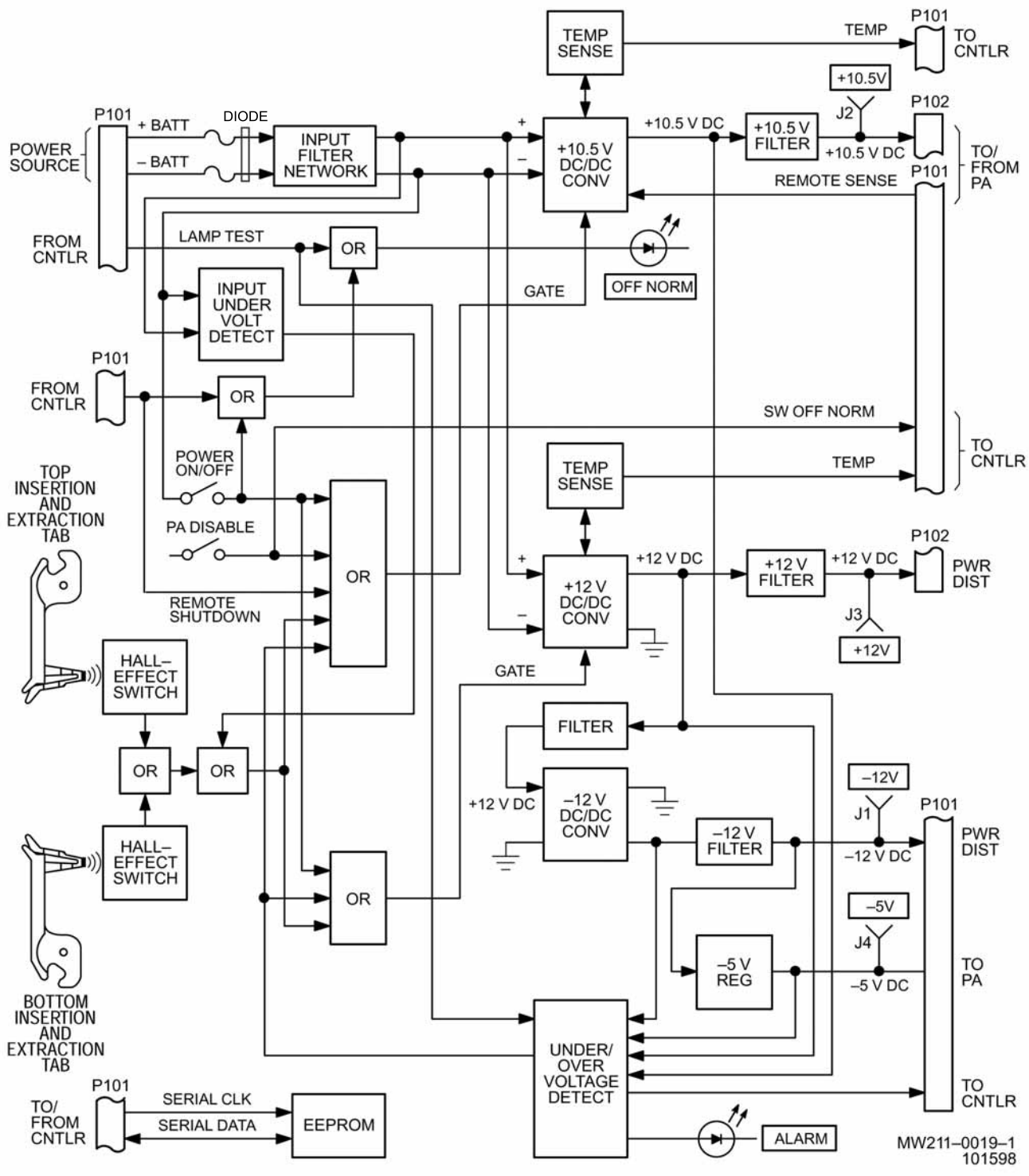

Figure 3-101 CE-16BB Power Supply Functional Block Diagram

The office battery is applied through a 15 A fast-blow fuse to the input filter. Battery noise present on the -48 Vdc inputs is attenuated by the filter, which in turn reduces noise on power supply outputs. The output of the filter is applied to the +10.5 Vdc and +12 Vdc DC/DC converters.

3.15.4.2 Features And Application Notes

Operates from ±20.5 to 60 Vdc input battery voltage to provide regulated output voltages

- Provides +10.5 Vdc, 0 to 12 A
- Provides +12 Vdc, 0 to 9 A
- Provides -12 Vdc, 0 to 700 mA
- Provides -5 Vdc, 0 to 100 mA
- Provides front panel and remote shutdown of +10.5 output
- Provides front-panel indicators for module failure and switch off normal
- Front access +10.5, +12, -12, and -5 Vdc, and GROUND test points
- Provides slow-start power to limit inrush current
- Provides field replaceable main power input fuses

3.15.4.3 +10.5 Volt DC/DC Converter

The +10.5 volt converter is a switching-type regulator that supplies +10.5 volts dc operating power to the power amplifier via connector P102. An overvoltage circuit monitors the power supply output and shuts down the supply if an overvoltage condition occurs. Circuit temperature sensing is provided.

Sensing circuits are used to monitor and automatically control the +10.5 Vdc voltage at the output of the +10.5 volt dc-to-dc converter. The sensing circuits are part of the feedback loop that maintains a constant voltage level at the input to the Pa. Any loss in the voltage at the load (PA) is detected and a REMOTE SENSE control signal is developed. The REMOTE SENSE signal is fed back to the dc-to-dc converter and the +10.5 Vdc output is adjusted to compensate for the loss.

3.15.4.4 +12 Volt DC/DC Converter

The +12 volt converter is a switching-type regulator that supplies +12 volts dc operating power to the applicable modules in the power distribution subsystem and cooling fans (if equipped). Circuit temperature sensing is provided. The +12 volt output is filtered and supplied to the -12 Vdc DC/DC converter.

3.15.4.5 -12 Volt DC/DC Converter

The -12 volt converter is a switching-type regulator that supplies -12 volts dc operating power to the applicable modules in the power distribution subsystem. The -12 volt output is filtered and supplied to the -5 Vdc regulator.

3.15.4.6 -5 Volt Regulator

The -5 volt regulator converts the applied -12 Vdc to -5 Vdc and supplies regulated -5 volts dc operating power to the PA.

3.15.4.7 Under/Overvoltage Sensor And Alarm Circuits

The under/overvoltage detector circuit monitors each of the power supply outputs for a possible undervoltage or overvoltage condition. Should an output voltage drop below or rise above normal, this circuit provides an output to the module alarm circuits. The module alarm circuits monitor the power supply controllers and the under/overvoltage sensor, and they respond to any abnormal condition by lighting the red module ALARM indicator and generating an alarm output to the controller.

Dedicated circuits in the under/overvoltage detector circuit monitor the -5 and -12 volts for undervoltage and shut down the +10.5 volt converter to prevent damage to the FETs.

3.15.4.8 Hall Effect Switch

The Hall effect switch function prevents the power supply from being inserted or removed from the shelf with voltage regulator outputs enabled. The function consists of top and bottom insertion and extraction tabs, Hall effect switches, AND gate, OR gate, +10.5 Vdc DC/DC converter, and +12 Vdc DC/DC converter. The Hall effect switch is triggered by the removal of the magnetic field generated by the magnet attached to the insertion and extraction tab. The field is removed from the associated Hall effect switch when the insertion and extraction tab is lifted to remove the module. When either top or bottom insertion and extraction tab has been lifted, the logic output of the AND gate is applied to the OR gate. Either this logic or the input from the input under voltage protection circuit generates the output of the OR gate which is applied to two other OR gates, controlling the gate voltage to the +10.5 Vdc DC/DC converter, and +12 Vdc DC/DC converter.

3.15.4.9 PA Disable and Remote Shutdown

When closed, the PA DISABLE switch turns off the 10.5 Vdc/DC converter and removes the 10.5 Vdc output to the PA, disabling the PA. The remote shutdown function allows the AE-37Y Controller to turn off the 10.5 Vdc/DC converter and shut down the 10.5 Vdc output to the PA, disabling the PA.

3.15.4.10 I^2C Bus

An EEPROM to interface the I^2C bus is provided. The I^2C bus communicates module part number, serial number, and revision history information to the AE-37Y Controller.