Exhibit 4. Product Overview (Part 2.1033)

4.1 Technical Description

The Access Terminal Modem operates through the PCS wireless infrastructure network. The modem provides the fastest fully mobile wireless link available from a PC to the internet, at data rates of up to 2.4Mbps. The unit incorporates two antennas two improve receiver performance through antenna diversity. One of the antennas also acts as the transmit antenna for communication with base-stations.

The modem can be attached to a laptop computer with velcro for mobile internet use. The modem communicates with the PC via an ethernet or USB cable.

The modem also incorporates a lithium-ion battery for use with a laptop when AC power is unavailable.

4.2 Address of Manufacturer and Applicant 2.1033 (c) (1)

Manufacturer:
Qualcomm Incorporated
5775 Morehouse Drive
San Diego, CA 92121
Telephone**:** (858) 587-1121

Applicant:
QUALCOMM, INC.
5775 Morehouse Dr.
San Diego, CA 92121
Telephone: (858) 587-1121

4.3 FCC Identifier 2.1033 (c) (2)

The FCC identifier is: J9CHDR1

4.4 User Manual 2.1033 (c) (3)

See Exhibit 7: User Manual

4.5 Types of Emissions 2.1033 (c) (4)

1M25F9W F1D wideband data signal

4.6 Frequency Range 2.1033 (c) (5)

The frequency range of terminal modem is the Personal Communications Services (PCS) bands, 1851.25 – 1908.75 MHz for transmission and 1931.25 – 1988.75 MHz for reception. The channel spacing is 1.25 MHz for CDMA.

4.7 Operating Power Levels 2.1033 (c) (6)

The equipment supports Class 3 Mobile Station Power Class, and its power output capability is reported to the Land Station via Station Class Mark.

4.8 Maximum Output Power 2.1033 (c) (7)

The equipment is within the limited 2 watts E.I.R.P.peak power of CFR 47 Part 24.232 (b) and is able to limit the output power to the minimum necessary for successful communications. The maximum peak output power the modem is designed to operate at is a granted power level of 0.490 W EIRP.

4.9 DC Supply and Current Range 2.1033 (c) (8)

The equipment is powered by an AC power supply that converts to 12Vdc. The specified DC operating range is 6-8.5 Vdc.

4.10 List of Semiconductor Active Devices 2.1033 (c) (10)

See exhibit 13: Parts List

4.11 Circuit Diagram 2.1033 (c) (10)

See exhibit 12 Schematics

4.12 Transmitter Adjustment Procedure 2.1033 (c) (9)

All frequency adjustments are set at the factory and there are no frequency field adjustments for this product. Under digital mode, frequency is locked to the base station and controlled by VCTCXO adjustments to offset any possible errors.

4.13 Frequency Stability Device 2.1033 (c) (10)

A temperature compensated, crystal oscillator (TCXO) is employed as a frequency reference for all of the transceiver local oscillators. This crystal oscillator is specified to remain within +/- 2.5 ppm over temperature and voltage variations. The lock status indicator of all synthesizers is monitored by the microprocessor and an out of lock condition will inhibit transmission. The mobile receiver monitors the received signal and adjusts the frequency of the TCXO, this corrects any errors between the mobile frequency and the base station transmitter. The mobile is locked to the base station.

4.14 Spurious Radiation Suppression Devices 2.1033 (c) (10)

Reference Designator	Part Name	Function
FL2	duplexer	Provides protection against transmitter spurious emissions and receiver local oscillator leakage
FL 6	TX Ceramic filter	Provides suppression of spurious energy and transmitter harmonics

4.15 Drawing of Equipment Identification Plate or Label 2.1033 (c) (11)

See Exhibit 8: Identifier Label:

4.16 Photographs 2.1033 (c) (12)

See Exhibit 9: Photographs

4.17 Modulation Technique 2.1033 (c) (13)

The CDMA mode is described in the following pages from the HDR Air Interface Specification. The justification for the CDMA bandwidth of 1.25 MHz is that the chip rate is 1.228 MHz (see page 6-10 of IS-95). When we look 3 dB down from the signal we find 1.25 MHz. Channel spacing is normally set at this 1.25 MHz.

2.1.3 Modulation Characteristics

2.1.3.1 Overview

The reverse link has the overall structure shown in Figure 2-1. The Reverse Channel consists of Access Channel, Pilot Channels, Data Rate Control (DRC) Channels, Reverse Rate Indicator (RRI) Channels and Reverse Traffic Channels. The Pilot and DRC Channels are time multiplexed whereas the RRI Channel is punctured in the Pilot Channel once every slot. Furthermore, the Traffic Data, Pilot, DRC and RRI Channels are orthogonally spread by appropriate Walsh functions. Each Traffic Data and Pilot/DRC Channel is then direct sequence spread by a distinct user long code sequence. The Access Channel is identified by a distinct Access Channel long code sequence.

The temporal structure of the Reverse HDR Channel is described in Figure 2-2. Frames are defined as 26.66... msec in length, the exact time of the Pilot PN rollover. Each frame consists of 16 slots, each 1.66... msec long. Each slot contains 2048 PN chips. The reverse link supports two baseband channels: The Pilot/DRC Channel and the Traffic Channel. Pilot symbols and DRC code symbols are time multiplexed in the Pilot/DRC Channel such that Pilot and DRC channels are each allocated 1024 chips per slot. In addition, Reverse Rate Indicator (RRI) symbols are punctured in the Pilot Channel at a rate of 64 chips per slot. The timing structure of a Pilot/DRC Channel slot is shown in Figure 2-3.

In *Connected* state, the access terminal is constantly transmitting Pilot/DRC channel. These pilot transmissions may be used by the access network for a number of functions, e.g. as an aid to initial acquisition, as a phase reference for the DRC and Data channels, and as an input to the closed loop reverse link power control.

The DRC message, when sent, passes through a (8,4,4) block encoder and is covered with one of 8 orthogonal Walsh functions. The set of possible Walsh covers has a one-to-one relation to sectors in the active set, and is conveyed to the access terminal by a *TrafficChannelAssignment* message. The sector in the active set mapped to the cover of a particular DRC codeword is the sector the access terminal requests forward transmissions from.

There are seven reverse link data rates ranging from 4.8 to 307.2 kbps (see Table 2-2). Data transmissions only begin at a particular slot boundary within a frame. This slot index (ReverseFrameOffset parameter) is assigned to the access terminal by the *TrafficChannelAssignment* message (see 4.7.6.6 for details). All data transmitted on the Reverse Traffic Channel is serially concatenated encoded, block interleaved, sequence repeated, and orthogonally spread by a Walsh function.

For rates up to 153.6 kbps, the "I" and "Q" baseband streams of the QPSK spread modulator are the Pilot/DRC and Traffic (when present) channels, respectively. For 307.2 kbps, the "I" baseband stream also contains the quadrature component of the reverse traffic channel. The reverse link is spread by a user long code sequence in order to allow the access network to distinguish between reverse link transmissions from different access terminals.

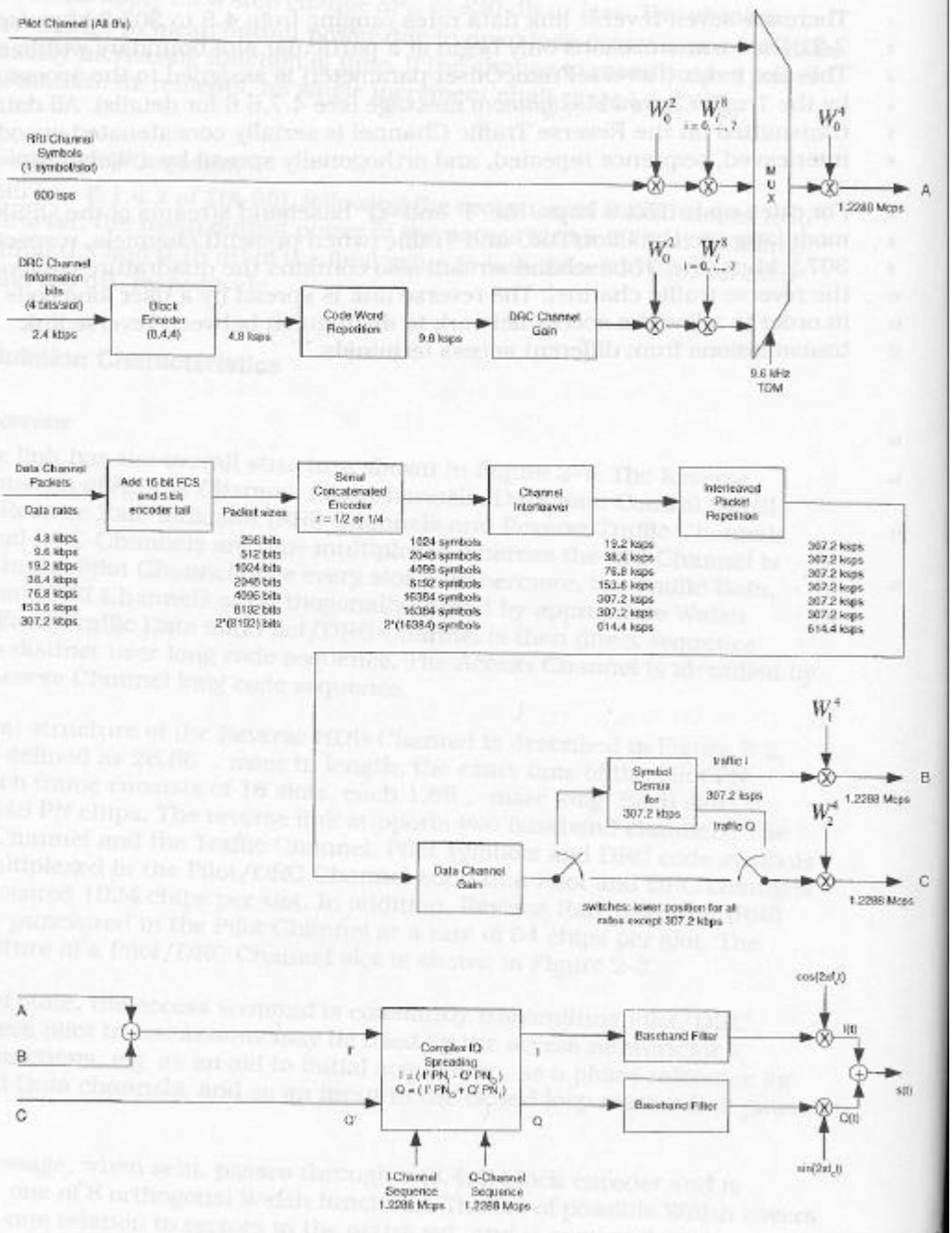

Figure 2-1 Reverse HDR Channel Structure[4]

[4] W_i^N denotes the n-chip Walsh function number i as specified in 2.1.3.5.

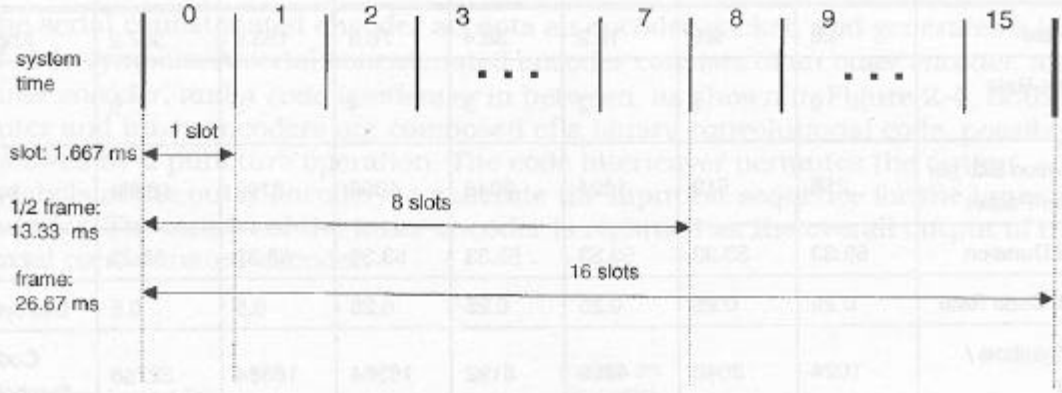

Figure 2-2 Reverse Link Frame Alignment

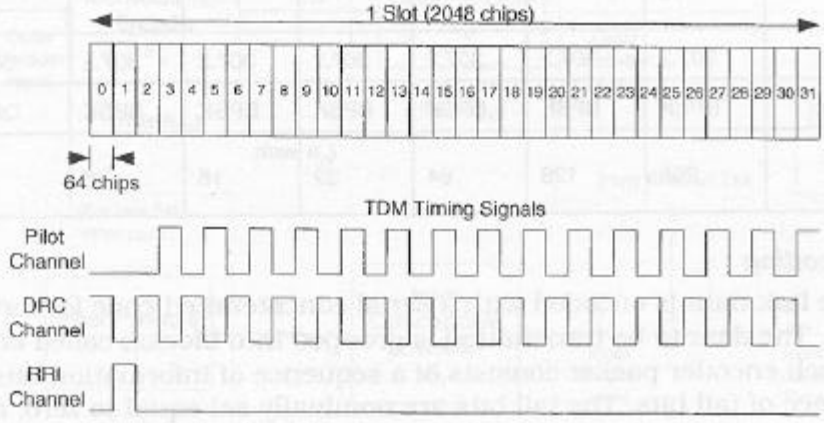

Figure 2-3 Slot Timing of Pilot/DRC Channel

2.1.3.1.1 Modulation Parameters

The modulation parameters for the Reverse Traffic and Access Channels are shown in Table 2-2.

Table 2-2 Modulation Parameters

Reverse Link	Traffic	Traffic / Access[5]	Traffic / Access	Traffic	Traffic	Traffic	Traffic	Units
Data Rate	4.8	9.6	19.2	38.4	76.8	153.6	307.2	Kbps
Reverse Rate Index	0	1	2	3	4	5	6	
Information Bits per Encoder Packet	256	512	1024	2048	4096	8192	16384	bits
Packet Duration	53.33	53.33	53.33	53.33	53.33	53.33	53.33	ms
Overall Code Rate	0.25	0.25	0.25	0.25	0.25	0.5	0.5	bits/sym
Code Symbols / Packet	1024	2048	4096	8192	16384	16384	32768	Code Symbols
Code Symbol Rate	19.2	38.4	76.8	153.6	307.2	307.2	614.4	Ksps
Interleaved Packet Repeats	16	8	4	2	1	1	1	
Mod Rate	307.2	307.2	307.2	307.2	307.2	307.2	307.2	Ksps
Data Modulation	BPSK	BPSK	BPSK	BPSK	BPSK	BPSK	QPSK	
PN Chips per Information Bit	256	128	64	32	16	8	4	PN chips

2.1.3.2 Encoding

The reverse link data is encoded with a serial concatenated code for forward error correction[6]. The data to be transmitted is grouped into blocks, called *encoder packets*. Each encoder packet consists of a sequence of information bits, followed by a sequence of tail bits. The tail bits are nominally set equal to zero, and are later over-written by the encoder. The encoder packet is fed to the serial concatenated encoder, which generates a sequence of code symbols. The actual number of information bits, tail bits, and code symbols associated with an encoder packet is determined by the data rate and frame duration.

The structure and operation of the serial concatenated codes will be described next. This description applies equally well to both the forward and reverse link data. The parameters that are specific to the access terminal transmitter are described in this chapter. In the next chapter, similar information about the access network transmitter is provided.

[5] Access Channel messages can be transmitted either at 9.6 or 19.2 kbps (see 2.1.3.8 for details).

[6] The data is also protected by a frame check sequence (FCS) at the framing layer. The details of this FCS are described in 4.2.2.2

4.18 Test Data 2.1033 (3) (14)

See Exhibit 7: Measurement Results and Exhibit 11: Radiated Test Report

4.19 RF Block Diagram

See Exhibit 12: Block Diagram