Hardware Functional Specification
WM3A5000 Mini PCI 3A 802.11a
(Atheros Chipset)

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1. SUMMARY

The Mini PCI 802.11a (WM3A5000) is Xircom's Mini PCI 3A wireless card. This Type 3A card is designed to operate with the Access Point mother board. This 802.11a wireless card is IEEE compliant, features bus mastering, and supports BPSK, QPSK, 16QAM, and 64QAM modulation schemes. The adapter supports the following data rates: 6, 9, 12, 18, 24, 36, 48 and 54 Mbps and operates in the unlicensed 5-GHz spectrum. The card operates with a 3.3V supply from the host socket. The Host interface is PCI 2.2 and PC Card 7.1 Standards compliant.

2. MRD REQUIREMENTS

The WM3A5000 hardware generally meets the requirements outlined in the Marketing Requirements Document (MRD), Xircom document number 103-0926-001. The WM3A5000 is functionality, virtually identical to Xircom's WCB5000 802.11a adapter. Both products may share the same software drivers.

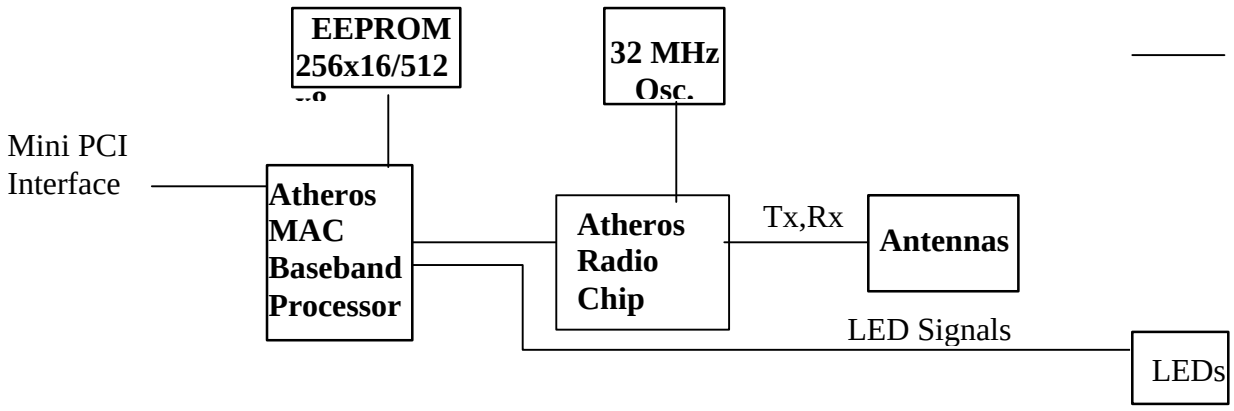
The typical 3.3V current has been measured on pre-production units under a variety of conditions, and is listed in the following chart:

WCB5000 state	**3.3V Current (mA)**
Initial Power-On state	32.0
No Association	420.0
Associated, idle	420.0
Associated, active	450.0-475.0

3. Functional Description

This section contains a complete description of the WM3A5000 hardware architecture. It includes a block diagram of the Mini PCI Card followed by a functional description of each block.

3.1. Functional Block Diagram



3.2. Functional Description of PC Card

3.2.1. Mini PCI Interface

The WM3A5000 interfaces with the host PC via an enhanced 68-pin connector. The 3.3V signaling conforms to the PCI Card Standard. The Mini PCI signals interface with the Athero AR5210 MAC Baseband Processor.

3.2.2. Atheros MAC Baseband Processor (AR5210)

The AR5210 Processor integrates the Media Access Control (MAC) and baseband processing functions. It supports either the PCI or CardBus host interface. When this chip is used along with the Atheros Radio-on-a-Chip (AR5110) the result is an IEEE 802.11a 5GHz design.

The AR5210 Processor implements a half-duplex, Orthogonal Frequency Division Multiplexing (OFDM) baseband processor supporting data rates from 6 Mbps to 54 Mbps. It uses the following modulation schemes: BPSK (binary phase shift keying), QPSK (quadrature phase shift keying), 16QAM (16 quadrature amplitude modulation), and 64QAM (54 quadrature amplitude modulation). Other features include: channel estimation, symbol timing, frequency offset estimation, signal detection, automatic gain

control, and forward error correction coding at rates of 1/2, 2/3 and 3/4.The AR5210 operates in accordance to the 802.11a specification with regards to transmit and receive frame filtering, frame encryption, and error recovery. It also controls data transfers with the host, interrupts, status and error reporting, power-down sequencing and hardware register access. Following is a description of the hardware interfaces on the ASIC utilized by the WM3A5000.

3.2.3.1. Host Interface

The host interface on the AR5210 is designed for PCI/CardBus applications. It consists of 32 bits of address and data, as well as all the required PCI control signals. The chip supports the 3.3V signaling environment, with clock speeds up to 33 MHz. Most of the host interface signals are bi-directional. The DMA block is a full bus mastering descriptor based engine.

3.2.3.2. Serial EEPROM Interface

The WM3A5000 is designed to support an EEPROM. The ROM contains configuration options, subsystem vendor IDs, CIS Pointers to be stored in AR5210, Boot ROM code, and manufacturing information. The EEPROM is a 256x16/512x8.

The AR5210 supports the industry standard I^2C "2-wire" serial interface to an external 256x16 bit EEPROM. The EEPROM stores configuration information for the PCI/CardBus. At power-up, the serial EEPROM reads logic internal to AR5210, automatically downloads configuration information and the Card Information Structure (CIS) into internal SRAM for the host PC to read. For more information on the serial EEPROM, refer to the Atheros AR5210 MAC/Baseband Processor Specification (attached to P/N 419-0024-001).

3.2.3.3. General Purpose Bits

The AR5210 has 6 bi-directional GPIO ports that are independently configured as input or output via the GPIO control register. One port is used on this design as an output LED driver for "ASSOCIATE".

3.2.3.4 LED Drivers

Two output pins are provided for LED drivers. Only one is used on this design, LED_0 which is used for network "ACTIVITY". Blinking of LED indicates network activity.

3.2.3.5 Antenna Switch

The AR5210 supports two antennas through Host software processing. The default antenna is the first antenna on which transmission is attempted. The same antenna is used for receive. If two transmissions fail in a row the second antenna is switched in for transmission and receive.

3.2.3.6 Phase Locked Loop

The PLL takes the base 32MHz clock from the AR5110 and derives either 40MHz or 80MHz as a core frequency. The baseband processor and the ADC/DAC use these clock frequencies.

3.2.3 Single-chip Radio (AR5110)

The AR5110 radio chip is an integrated, IEEE 802.11a compliant, 5GHz CMOS transceiver. It requires no external active components or SAW filters. The transceiver core, digital logic, and VCO are powered by 2.5V. The I/O's are powered by 3.3V.

The AR5110 supports eight channels between 5.15 and 5.35 GHz, leaving two 20MHz channels unused as a guard band. Across the 5.12 and 5.25 GHz band the FCC permits a maximum transmit power of 50mW, the design outputs less than 40mW. The FCC permits a maximum power rating of 250mW in the 5.25 to 5.35 GHz band, but is limited to less than 100mW in this design. The 20MHz channels are divided into 52 carriers, 48 carry data and 4 are pilot signals. All 52 carriers are always used. Varying modulation and error-correction coding supports standard IEEE 802.11a data rates that range from 6 to 54 Mbps. Each of the carriers are ~300KHz wide, resulting in raw data that ranges from 125Kbps to 1.5Mbps.

3.2.4 Antenna Connection

The antennas are connected using UMP SMT connectors. See Access Point descriptions for antenna description.

Special FCC 15.407 Requirements

Frequency Stability (15.407 (g))

FCC 15.407(g) states: "Manufacturers of U-NII devices are responsible for ensuring frequency stability such that an emission is maintained within the band of operation under all conditions of normal operation as specified in the users manual."
The device uses 8 channels between 5.18GHz and 5.32GHz. The carrier is 20MHz wide centered at these frequencies. IE: Channel 6 (5.18GHz) would have the fc centered at 5.18GHz with a bandwidth of 20Mhz or 5.17 to 5.19 GHz. This provides a guard band of 20 MHz (5.17 GHz - 5.15 GHz).

The device also requires a +/- 20 ppm XTAL over temperature and with aging. This is required per the 802.11a specification. Based on the tolerance of the XTAL and the 20 MHz guard band between 5.15GHz and 5.35 GHz the device will maintain emissions within the UNII 1 and 2 bands under normal operating conditions specified in the user manual.

Insuring Indoor Use in 5.15-5.25 GHz Band (15.407 (e))

FCC 15.407(e) states: "Within the 5.15-5.25 GHz band, U-NII devices will be restricted to indoor operations to reduce any potential for harmful interference to co-channel MSS operations."
The user manual includes the following statement:

> "Radio Frequency interference requirements: This device is restricted to indoor use only. Industry Canada and FCC requires this product to be used indoors due to its operation in the frequency range 5.15 to 5.25 GHz"

Discontinue Transmitting with absence of Data or operational failure (15.407 (c))

FCC 15.407(e) states: "*The device shall automatically discontinue transmission in case of either absence of information to transmit or operational failure. These provisions are not intended to preclude the transmission of control or signaling information or the use of repetitive codes used by certain digital technologies to complete frame or burst intervals. Applicants shall include in their application for equipment authorization a description of how this requirement is met*."

Data transmission is always initiated by software, which is then passed down through the MAC, through the digital and analog baseband, and finally to the RF chip. Several special packets (ACKs, CTS, PSPoll, etc...) are initiated by the MAC. These are the only ways the digital baseband portion will turn on the RF transmitter, which it then turns off at the end of the packet. Therefore, the transmitter will be on only while one of the aforementioned packets is being transmitted.