



Elliott Laboratories Inc.
www.elliottlabs.com

684 West Maude Avenue
Sunnyvale, CA 94086-3518

408-245-7800 Phone
408-245-3499 Fax

RE: Intel / Xircom
FCC ID: J3OWCB5000

In response to your comments on the above application, please find our responses to each issue in the text below:

1.) The file entitled "Install Guide Regulatory 2 of 2" appears to indicate there will be multiple antennas associated with this device. These antennas must be listed and identified by type, and/or part numbers and gain, and included in the RF Exposure information. In addition, the language used is not consistent with FCC requirements for mobile devices.

The file "Install Guide Regulatory 2 of 2" is a generic document provided with the full series of products. The information that references multiple antennas is for devices in the Enterprise series solution that are still in development. Page 13 of 18 in the file "Install Guide 1 of 2" contains the relevant information.

An additional document was provided as a part of the rf exposure information. This has further information that will be included in the final manual for the cardbus product. This document has been uploaded a second time as "Theory of Operations – addendum".

2.) The FCC will not allow the inclusion of internal photographs in Confidentiality requests. Supply revised Confidentiality request.

The client does not want the identity of the chipset used in the device to be revealed. I have studied the internal pictures and believe that the chipsets cannot be identified from the photographs provided. If you could also please confirm that the identity of the chipset cannot be determined from these photographs then this is acceptable. The Confidentiality request has been revised and uploaded in anticipation of this.

3.) Block diagram does not meet the requirements of 2.1033(b)(5). Please supply a more detailed diagram.

The majority of the frequency-determining circuitry is included in the chipset. The only external clock/frequencies are a 32MHz reference clock for the chipset and the 33MHz CardBus interface bus. Intel are not privy to the block diagram for the chipset. If this is needed it may be possible to provide ATCB with a copy from the chip set manufacturer.

The block diagram has been modified to better show the external clocks. Please advise if the chipset block diagram will be required.

If you have any questions, please contact me via doc@elliottlabs.com

Regards,

Mark Briggs