Theory of Operation

TT-7000TS-AB

THEORY OF OPERATION:
Control Board Assembly

Power Supplies:

Power is supplied through J1. Pins 1 and 2 are +12 volts; pins 3 and 4 are ground. Ferrite beads are used on all connections on J1 to minimize RF leakage to the power lines. C1 and C2 provide additional RF filtering of the 12 volts before it passes through D1, which provides reverse polarity protection for the transmitter. Filter capacitors are used on the inputs and outputs of the regulators to prevent unwanted oscillations. U2 is a fixed +5 volt regulator used primarily for the logic and prescaler circuits. U1 is a fixed +8 volt regulator used for the audio, video circuits and miscellaneous operational amplifiers. Q2, 5, 6, and R8-15 form a variable voltage regulator for the driver FET that is adjusted by R14 for proper drive levels to the final amplifier. Q1, 3, 4 and R2-6 form a variable voltage regulator for the final amplifier. R16-20 and S1 are placed in the feedback portion of the regulator to provide a selectable voltage output to the PA. Selection of the voltage applied to the final amplifier allows different power levels to be achieved. R19 sets power output to 12 Watt while R20 sets the output power to 2 Watts. R37-40, 51, C36-40, C95, and U5 Generates the negative 2-volt bias required for the FET's on the PA. Q7 and Q8 disable the variable voltage regulators to prevent power from being applied to the PA until the PLL provides a lock detect condition. R44 and C27 remove the narrow pulses originating from the lock detect output of U6 pin 28.

Video circuits:

Video is connected through J2 to the 525-line video pre-emphasis network of R22-26, C12, and L1. R25 allows for the adjustment of the network due to tolerance deviation of components. This network also forms a 75-ohm termination for the video. D4 and D5 provide deviation limiting. R28 adjusts video deviation of the transmitter. C11 and C13 remove the D.C. component of the video signal.

Audio circuits:

Audio for sub-carrier 1 is connected through pins 6 (high) and 7 (low) of J1 to T1, which is configured as a 600-ohm balanced coupling transformer. The output of T1 is terminated with R79 and A.C. coupled to U7 by C48. U7 is a dual gain control circuit. Channel 1(pins 1,2,3,5,6,7,8) is configured to amplify the audio while channel 2 (pins 9,10,11,12,14,15,16) acts as a limiter and provides a 2: 1 compression of the audio signal. R62-64, C59-61 and Q11 form a three pole 10 KHz low-pass filter. R65 is used to adjust the deviation of the sub-carrier. R66-70, C62-65, L2, D8, and Q12 form a series tuned colpitts oscillator. L2 is a variable inductor for tuning the frequency of the oscillator. Sub-carrier frequencies available are 4.83Mhz, 5.8Mhz, 6.2Mhz, 6.8Mhz and 7.5Mhz. C62 couples the audio to the oscillator. D8 is the varactor diode, which modulates the sub carrier. Q13 is a buffer amplifier and L3 and C67 provides tuning (peaking) for the amplifier. R74 is used to adjust the sub- carrier insertion level.

THEORY OF OPERATION:
Control Board Assembly

Audio circuits:

Audio for sub-carrier 2 is connected through pins 8 (high) and 9 (low) of J1 to T2, which is configured as a 600-ohm balanced coupling transformer. The output of T2 is terminated with R78 and A.C. coupled to U8 by C71. U8 is a dual gain control circuit. Channel 1(pins 1,2,3,5,6,7,8) is configured to amplify the audio while channel 2 (pins 9,10,11,12,14,15,16) acts as a limiter and provides a 2: 1 compression of the audio signal. R86-88, C82-84 and Q14 form a three pole 10 KHz low-pass filter. R89 is used to adjust the deviation of the sub-carrier. R90-94, C85-88, L4, D9, and Q15 form a series tuned colpitts oscillator. L2 is a variable inductor for tuning the frequency of the oscillator. Sub-carrier frequencies available are 4.83Mhz, 5.8Mhz, 6.2Mhz, 6.8Mhz and 7.5Mhz. C85 couples the audio to the oscillator. D9 is the varactor diode, which modulates the sub carrier. Q16 is a buffer amplifier and L5 and C90 provides tuning (peaking) for the amplifier. R98 is used to adjust the sub- carrier insertion level.

PLL circuits:

PLL IC:

It is beyond the scope of this document to discuss the theory of Phase Locked Loop design only the support circuits and operation will be detailed. U6 is a low frequency CMOS PLL. It contains a reference oscillator, selectable-reference divider, two output phase detector, 10-bit programmable divide-by-N counter, 6-bit programmable divide-by-A counter, dual modulus controller, and a lock detect circuit. If combined with a VCO, dual modulus, and loop filter, then frequency synthesis up to the devices frequency limit can be achieved. Tron-Tek, Inc. equipment also incorporates a Micro-Controller to allow operation only within the user designated frequencies of 1990-2110, 2025-2135 and 2450-2499. Additionally this equipment utilizes an external temperature compensated reference oscillator (TCXO).

VCO:

See VCO section for description.

Dual Modulus:

U4 is a Dual Modulus which divides the VCO frequency by 64 or 65 depending on the status of the A counter within U6. Control of the divide ratio is provided by U6 pin 9. R36 provides proper input load. C28 A.C. couples the VCO frequency into U4. R53 provides an output load while C34 A.C. couples the output of U4 into the U6 Pin 1. The A and N counter then divide this frequency and present it to the phase detector for comparison to the reference frequency. C31-33 and C35 provide de-coupling for U4.

THEORY OF OPERATION:
Control Board Assembly

PLL circuits:

Loop Filter/Buffer:

R45-50, C17-25, and U3 form the low pass loop filter. This filter removes the narrow pulses inherent in the phase detector and provides a loop error signal. The video, audio and loop filter signals are summed at the base of Q9, which buffers this signal. R35 provides a load for the buffer and R34 decouples the high frequency of the VCO while coupling the control voltage to the VCO.

TCXO:

R41, R43, R52, R100, C42, C43, Q10, Y1, and C45-47 form a 16MHz oscillator. C47 and R52 provide temperature compensation for the crystal. C45 in parallel with C46 provide frequency adjustment. C41 couples the oscillator into U6. U6 pins 4,5, and 6 program a counter to divide the 16 MHz input by 128. This produces a reference frequency of 125 KHz used by the phase detector.

Micro-Controller

Frequency selection is accomplished by controlling the 12 bit binary word present on the inputs of the A and N counters of U6 pins 10-25. To program the frequency, the user simply dials in the frequency on the push-wheel switches (S2-S5). The micro-controller inputs the switch settings and checks the validity of the frequency then generates the binary word for that frequency. If the frequency is invalid the micro-controller outputs a binary word (all ones) which causes the PLL lock detect output to go low (See section on POWER SUPPLIES). This process is repeated once each second to determine if a new frequency is desired. U9 is a programmable micro-controller, which contains an on-chip oscillator, two 8-bit bi-directional I/O ports one 4-bit bi-directional I/O port, 15-stage multifunctional counter, 5120 bytes of user EPROM, and 384 bytes of RAM. Port A pins 19-26 and port B pins 9-12 are configured as outputs for the 12 bit binary word and are connected to U6 pins 10-18, 22 and 24-25. Port B pins 5-8 are active low outputs that select which switch will be read. Only one output will be low at any given time. Port C pins 15-18 forms the 4-bit BCD input bus for the switch data. Data is present on the 4-bit input bus when an output from port B goes low. Depending on the switch setting this low will pull the corresponding BCD pins low. This process continues until all BCD data from the switches have been input and remained static for two seconds. The binary word is then generated and checked for a valid frequency before updating the output register. Because the switch data present on port C is multiplexed, diodes D10-23 are required to isolate the switches that are not being read. R104-107 provides pull-up resistors for the 4-bit input bus.

THEORY OF OPERATION:

VCO Assembly

VCO:

The VCO is a fundamental mode voltage controlled colpitts oscillator. The frequency of the VCO runs at 3.5 Ghz, +/- 300 Mhz. The frequency is determined by the varactor, D1 and C22. The output of the VCO is coupled through C24 to the gate of Q2. Q2 and Q3 are general purpose, low noise, low power FET's with an Ft of 12Ghz. L3, along with the distributed capacitance of L3, tunes the gate of Q2 at 3.5 Ghz cause the FET to self-bias. Two 470 Ohm are provided and act as dropping resisters when self biased and current limiting resisters when not self biased. The tuned circuit amplifies the second harmonic and couples it into Q3 through C28. The circuitry around Q3 performs identically to Q2. The output of Q3 is coupled into a High-Pass filter through C60. The filter consists of C55-C60 and L8-L10. L8-L10 are the tuning elements of the filter and are adjusted for maximum output of the VCO the tuning range 7.0 Ghz +/- 125 Mhz. The output of the filter is coupled through C55 to the gate of Q4. Q4 is self biased with R18 providing a DC return as well as a stabilizing element. The output is matched to 50 Ohms through a printed capacitor and L6. The typical output of Q4 is 70mW from 6875-7125 with the 2^{nd} harmonic of 3.5 Ghz measuring greater than –40dBc.

THEORY OF OPERATION:
PA Assembly

Power Amplifier:

The PA uses two GaAs FET amplifiers to produce up to 2-Watts of output power. The VCO output enters the PA via a 50-ohm transmission line into C1, which couples the exciter output into the matching network of C1. This matching network is required due to the low input impedance of FET1. R1 couples the negative bias into FET1. C2-4 and C14-17 decouple the negative bias of FET1. C5-7, C18-20, and C24-32 decouple the 10-volt supply of the driver amplifier. C8-10, and C37-47 decouple the negative bias for FET2. R2 couple the negative bias into FET2. C11-13, C21-23, C34-35, C48-53, 55-71 and the RFC's decouple the 10-volt supply on the final amplifier. C36 couples the signal from FET1 into FET2, while C54, L3, and L4 couple and tune the output of FET2 into the Low Pass Filter assembly.

Isolator and Low-Pass Filter assembly:

Isolator:

The isolator ISO is used to ensure a matched condition to the PA regardless of changing load conditions at the antenna.

Low-Pass Filter:

The LPF consist of a 50 Ohm line, T1, a 1.5pF capacitor and empirically derived transmission line for maximum harmonic reduction and matching into a 50 Ohm load, T2.

Theory Of Operation:

Block Diagram