THEORY OF OPERATION:
Control Board Assembly

Power Supplies:

Power is supplied through J1. Pins 1 and 2 are +12 volts; pins 3 and 4 are ground. Ferrite beads are used on all connections on J1 to minimize RF leakage to the power lines. C1 and C2 provide additional RF filtering of the 12 volts before it passes through D1, which provides reverse polarity protection for the transmitter. Filter capacitors are used on the inputs and outputs of the regulators to prevent unwanted oscillations. U2 is a fixed +5 volt regulator used primarily for the logic and prescaler circuits. U1 is a fixed +8 volt regulator used for the audio, video circuits and miscellaneous operational amplifiers. Q2, 5, 6, and R8-15 form a variable voltage regulator for the driver FET that is adjusted by R14 for proper drive levels to the final amplifier. Q1, 3, 4 and R2-6 form a variable voltage regulator for the final amplifier. R16-20 and S1 are placed in the feedback portion of the regulator to provide a selectable voltage output to the PA. Selection of the voltage applied to the final amplifier allows different power levels to be achieved. R19 sets power output to 12 Watt while R20 sets the output power to 2 Watts. R37-40, 51, C36-40, C95, and U5 Generates the negative 2-volt bias required for the FET's on the PA. Q7 and Q8 disable the variable voltage regulators to prevent power from being applied to the PA until the PLL provides a lock detect condition. R44 and C27 remove the narrow pulses originating from the lock detect output of U6 pin 28.

Video circuits:

Video is connected through J2 to the 525-line video pre-emphasis network of R22-26, C12, and L1. R25 allows for the adjustment of the network due to tolerance deviation of components. This network also forms a 75-ohm termination for the video. D4 and D5 provide deviation limiting. R28 adjusts video deviation of the transmitter. C11 and C13 remove the D.C. component of the video signal.

Audio circuits:

Audio for sub-carrier 1 is connected through pins 6 (high) and 7 (low) of J1 to T1, which is configured as a 600-ohm balanced coupling transformer. The output of T1 is terminated with R79 and A.C. coupled to U7 by C48. U7 is a dual gain control circuit. Channel 1(pins 1,2,3,5,6,7,8) is configured to amplify the audio while channel 2 (pins 9,10,11,12,14,15,16) acts as a limiter and provides a 2: 1 compression of the audio signal. R62-64, C59-61 and Q11 form a three pole 10 KHz low-pass filter. R65 is used to adjust the deviation of the sub-carrier. R66-70, C62-65, L2, D8, and Q12 form a series tuned colpitts oscillator. L2 is a variable inductor for tuning the frequency of the oscillator. Sub-carrier frequencies available are 4.83Mhz, 5.8Mhz, 6.2Mhz, 6.8Mhz and 7.5Mhz. C62 couples the audio to the oscillator. D8 is the varactor diode, which modulates the sub carrier. Q13 is a buffer amplifier and L3 and C67 provides tuning (peaking) for the amplifier. R74 is used to adjust the sub- carrier insertion level.

THEORY OF OPERATION:
Control Board Assembly

Audio circuits:

Audio for sub-carrier 2 is connected through pins 8 (high) and 9 (low) of J1 to T2, which is configured as a 600-ohm balanced coupling transformer. The output of T2 is terminated with R78 and A.C. coupled to U8 by C71. U8 is a dual gain control circuit. Channel 1(pins 1,2,3,5,6,7,8) is configured to amplify the audio while channel 2 (pins 9,10,11,12,14,15,16) acts as a limiter and provides a 2: 1 compression of the audio signal. R86-88, C82-84 and Q14 form a three pole 10 KHz low-pass filter. R89 is used to adjust the deviation of the sub-carrier. R90-94, C85-88, L4, D9, and Q15 form a series tuned colpitts oscillator. L2 is a variable inductor for tuning the frequency of the oscillator. Sub-carrier frequencies available are 4.83Mhz, 5.8Mhz, 6.2Mhz, 6.8Mhz and 7.5Mhz. C85 couples the audio to the oscillator. D9 is the varactor diode, which modulates the sub carrier. Q16 is a buffer amplifier and L5 and C90 provides tuning (peaking) for the amplifier. R98 is used to adjust the sub- carrier insertion level.

PLL circuits:

PLL IC:

It is beyond the scope of this document to discuss the theory of Phase Locked Loop design only the support circuits and operation will be detailed. U6 is a low frequency CMOS PLL. It contains a reference oscillator, selectable-reference divider, two output phase detector, 10-bit programmable divide-by-N counter, 6-bit programmable divide-by-A counter, dual modulus controller, and a lock detect circuit. If combined with a VCO, dual modulus, and loop filter, then frequency synthesis up to the devices frequency limit can be achieved. Tron-Tek, Inc. equipment also incorporates a Micro-Controller to allow operation only within the user designated frequencies of 1990-2110, 2025-2135 and 2450-2499. Additionally this equipment utilizes an external temperature compensated reference oscillator (TCXO).

VCO:

See VCO section for description.

Dual Modulus:

U4 is a Dual Modulus which divides the VCO frequency by 64 or 65 depending on the status of the A counter within U6. Control of the divide ratio is provided by U6 pin 9. R36 provides proper input load. C28 A.C. couples the VCO frequency into U4. R53 provides an output load while C34 A.C. couples the output of U4 into the U6 Pin 1. The A and N counter then divide this frequency and present it to the phase detector for comparison to the reference frequency. C31-33 and C35 provide de-coupling for U4.

THEORY OF OPERATION:
Control Board Assembly

PLL circuits:

Loop Filter/Buffer:

R45-50, C17-25, and U3 form the low pass loop filter. This filter removes the narrow pulses inherent in the phase detector and provides a loop error signal. The video, audio and loop filter signals are summed at the base of Q9, which buffers this signal. R35 provides a load for the buffer and R34 decouples the high frequency of the VCO while coupling the control voltage to the VCO.

TCXO:

R41, R43, R52, R100, C42, C43, Q10, Y1, and C45-47 form a 16MHz oscillator. C47 and R52 provide temperature compensation for the crystal. C45 in parallel with C46 provide frequency adjustment. C41 couples the oscillator into U6. U6 pins 4,5, and 6 program a counter to divide the 16 MHz input by 128. This produces a reference frequency of 125 KHz used by the phase detector.

Micro-Controller

Frequency selection is accomplished by controlling the 12 bit binary word present on the inputs of the A and N counters of U6 pins 10-25. To program the frequency, the user simply dials in the frequency on the push-wheel switches (S2-S5). The micro-controller inputs the switch settings and checks the validity of the frequency then generates the binary word for that frequency. If the frequency is invalid the micro-controller outputs a binary word (all ones) which causes the PLL lock detect output to go low (See section on POWER SUPPLIES). This process is repeated once each second to determine if a new frequency is desired. U9 is a programmable micro-controller, which contains an on-chip oscillator, two 8-bit bi-directional I/O ports one 4-bit bi-directional I/O port, 15-stage multifunctional counter, 5120 bytes of user EPROM, and 384 bytes of RAM. Port A pins 19-26 and port B pins 9-12 are configured as outputs for the 12 bit binary word and are connected to U6 pins 10-18, 22 and 24-25. Port B pins 5-8 are active low outputs that select which switch will be read. Only one output will be low at any given time. Port C pins 15-18 forms the 4-bit BCD input bus for the switch data. Data is present on the 4-bit input bus when an output from port B goes low. Depending on the switch setting this low will pull the corresponding BCD pins low. This process continues until all BCD data from the switches have been input and remained static for two seconds. The binary word is then generated and checked for a valid frequency before updating the output register. Because the switch data present on port C is multiplexed, diodes D10-23 are required to isolate the switches that are not being read. R104-107 provides pull-up resistors for the 4-bit input bus.

THEORY OF OPERATION:

VCO Assembly

VCO:

The VCO is a fundamental mode voltage controlled colpitts oscillator. VAR1, L1, C3, and C6 are the main frequency determining elements with the capacitance of Q1 completing the colpitts circuit. The fundamental frequency of operation is 1.7 to 2.3 GHz. L1 is adjusted to set the control voltage at 3-5 volts for a tuning frequency of 1850 to 2150 MHz (best linear tuning range of VAR1). R5 is selected as large as possible and L1 as small as possible for a smooth tuning bandwidth of 500 to 600 MHz. The VCO is further stabilized with R8 at the junction of C10 and C11. R6 and C5 couple the signal to U1, which divides the frequency by 2. This signal (1/2vco) is fed to the PLL circuit to generate an error voltage for the VCO. The RF level at the output of C11 is approximately 3 mW which is fed to Q2 through R9. R9 reduces drive to Q2 and swamps out some of the base reactance of Q2 being reflected back into the VCO. Q2 and Q3 are isolation amplifiers. Bias resistors R11 and R15 are selected to set the collector voltage of Q2 and Q3 to approximately 4 volts. R14 reduces drive to Q3 and swamps out some of the base reactance of Q3 from being reflected back into Q2. The output level of Q3 is approximately 15 mW. The signal is coupled through C24 to the matching network of L5 and C28. Q4 is a current source for Q5. R19 and R21 set's the base voltage on Q4 to produce a 1-volt drop across R20, thus limiting the collector current of Q5 to 45 mA. The collector of Q4 provides current to the base of Q5 through R22. R22 drops half the collector voltage of Q4 and acts as a current limiter to the base of Q5. Q5 is a common emitter amplifier, which results in a very stable hi-gain amplifier with good bandwidth properties. L7 and C34 are the matching elements and C35 is the coupling capacitor. Typical output power is 125 mW into a 50-ohm load at specified frequency. This amplifier exhibits no spurious oscillations or break up with the output open, shorted or exposed to any load or phase angle.

THEORY OF OPERATION:

PA Assembly

Power Amplifier:

The PA uses two GaAs FET amplifiers to produce up to 12-Watts of output power. The VCO output enters the PA via a 27-ohm resistor into C1, which couples the VCO into the matching network of C33-34 and L1. This matching network is required due to the low input impedance of FET1. R1 couples the negative bias into FET1. C4, and C8-9 decouple the negative bias voltage. C6, C10-16, C18, and RFC decouple the 10-volt supply of the driver amplifier. DCR and C35 tune the frequency response of the amplifier C36 and L2 filter this frequency. C2 couples the driver amplifier into the matching network of C37-38 and L3. This matching network is required due to the low input impedance of FET2. R2 couples the negative bias into FET2. C19-20 decouples the negative bias voltage. C23-32 and RFC decouple the 3-10 volt supply of the final amplifier. DCR and C39 tune the frequency response of the amplifier; C40 and L4 filter this frequency. C3 couples the final amplifier into the isolator-matching network of C41-43 and L5, 6. The output of the network if then connected to the isolator input.

Isolator and Low-Pass Filter assembly:

Isolator:

The isolator ISO is used to ensure a matched condition to the PA regardless of changing load conditions at the antenna..

Low-Pass Filter:

C1-3 and L1-2 form a 5-element Chebyshev low pass filter to suppress spurious and harmonic emissions