Theoretical Process Gain with Chip/bit Data rate

As per our phone conversation this morning, here is my proposed answer to the FCC's first question. If this is acceptable, I will include it in the update to our Processing Gain Test documentation and send you an updated copy.

1) What is the theoretical process gain? Chip/bit and spread rate/data rate for each data rate.

Theoretical
CCK Modulation Processing
Bit Rate Symbol Rate Chip Rate Chips/Symbol Coding Gain* Gain**
(Mb/s) (MS/s) (MC/s) (dB) (dB)
-------- ----------- --------- ------------ -------------- -------------
1 1 11 11 N/A 10.4
2 1 11 11 N/A 10.4

5.5 1.375 11 8 1.6 10.6
11 1.375 11 8 1.6 10.6

* CCK Modulation (used at 5.5 and 11Mb/s) provides a Coding Gain of 1.6dB.

** Theoretical Processing Gain Calculation
1 & 2Mb/s rates : $10*\log(\text{Chips/Symbol}) = 10*\log(11) = 10.4\text{dB}$
5.5 & 11Mb/s rates: $10*\log(\text{Chips/Symbol}) + \text{Coding Gain}$
$= 10*\log(8) + 1.6\text{dB} = 9.0\text{dB} + 1.6\text{dB} = 10.6\text{dB}$

Regards,
Jeff

--
Jeff Kelm SpectraLink Corp.
Sr. RF Engineer 5755 Central Ave.
jkelm@spectralink.com Boulder, CO 80301
303-583-5312