CIRCUIT DESCRIPTION: BS HH16 UHF

GENERAL INFORMATION

The BS HH16 UHF has two printed circuit boards; Interface board, Radio Frequency, CPU and Audio Frequency (RF) board.

The RF board contains the VCO/Synthesizer section, Transmitter Section, Receiver Section, Transmitter Audio circuitry, CPU (the Microprocessor/Control Section).

Receiver Audio circuitry, and Battery Section.

MICROPROCESSOR / CONTROL SECTION

The microprocessor **IC801** is constantly operating when the radio is turned ON. It is continuously monitoring,the PTT line and other internal inputs such as the squelch detect, etc.

When a change occurs, the microprocessor makes the appropriate response.

The microprocessor is used for control. The Radio emits a beep on channel change and the synthesizer is loaded with the correct frequency information. The microprocessor runs off a 8.4 MHz oscillator which is composed of **X801**, **C802**,**C803,C804** and **R802**.

When the radio is first turned on, the microprocessor reads the radio status from the EEPROM **IC804**.

VCO / SYNTHESIZER SECTION

This section consists of the Temperature-Compensated Crystal Oscillator (TCXO) circuit **(X301)**, Voltage Controlled Oscillators (VCO) circuit, Synthesizer and the Loop Filter.

Temperature-Compensated Crystal Oscillator (TCXO) circuit

The circuit of TCXO is included in **X801**.

The temperature compensated crystal-oscillator is held within the specified ±2.5 PPM from -30 to +60 degree C.

Voltage-Controlled Oscillators circuit

Only one of the VCOs runs at a time, which is controlled by **IC801**. When the PTT is pressed, **IC801** pin55 goes low (approx. 0V) disabling the receive VCO by the **Q302** and biases on **Q304** to enable the transmitter VCO.

The receive VCO consists of **C301-C308**, **L301**, **L303**, and **Q301**, **Q302**.

This VCO oscillates at 45.1 MHz above the programmed receive frequency.

The VCO's oscillating frequency is tuned by the varactor **D301**.

The tuning voltage is supplied from the output of the Loop Filter.

The output of the VCO is AC coupled (**C303,312**) to the synthesizer and the output VCO **Q301,303** respectively.

The output of the VCO buffer **Q307** is AC coupled (**C344**) to the synthesizer and the output buffer **Q308** respectively.

The transmitter VCO consists of **C312-C318**, **L304**, **L305**, **Q303**, **Q304 and D302**.

This VCO oscillates on the programmed transmit frequency. The VCO's oscillating frequency is tuned by the varactor **D304.** The tuning voltage is supplied from the output of the Loop Filter.

The transmit voltage controlled oscillator is directly frequency-modulated and operates on the carrier frequency. In the receive mode, the transmit VCO is disabled and the receive VCO is enabled, producing the receive local oscillator signal at a frequency 45.1MHz above the incoming receive frequency.

The synthesizer is tuned in 5.00kHz or 6.25kHz step.

Synthesizer

The frequency synthesizer is a large-scale monolithic synthesizer integrated circuit **IC301**.

The synthesizer IC contains a dual modulus prescaler, programmable divide-by-N counter, prescale control (swallow) counter, reference oscillator, reference divider, phase detector, charge pump and lock detector.

Also, included in **IC301** are shift registers and control circuits for frequency controls and general device control.

RF output from the active VCO is AC coupled to the synthesizer **IC301** prescaler input at Pin 8. The divide counter chain in **IC301**, consisting of the dual-modulus prescaler, swallow counter and programmable counter, divides the VCO signal down to a frequency very close to 5.00kHz or 6.25kHz which is applied to the phase detector. The phase comparator compares the phase with the 5.00kHz or 6.25kHz reference signal from the reference divider.

The synthesizer unlock detector circuit prevents the operation of the transmitter and receiver, when the phase lock loop (PLL) is unlocked. The following discussion assumes the unit has been placed in the transmit mode. **IC301** lock detector Pin 6 goes high when the PLL is locked. This high level is applied to Pin 20 of the microprocessor **IC801**. A software timing routing brings the ANT _B/TX line High (Pin 28, 29 of **IC801**). With the ANT_B/TX line High, **Q405** is on and **Q405** is biases on passing **TX6** to **Q404,** it biases on **Q404** to pass switched **TX6** to the transmitter amplifier string which enables transmission.

When the PLL become unlocked, the lock detector at **IC301** Pin7 will begin pulsing low. A RC circuit converts pulsing low to a low level for the microprocessor. The microprocessor then changes the RX/TX line to a high, thus signaling the other transistor switches to drive **Q404** into cutoff which disable transmission.

Loop Filter

The Loop Filter, a passive lead-lag filter consisting of **R312-R316**, **VR301** and **C325-C327** output to produce the DC turning voltage for the VCO. One parasitic pole, consisting of RFchokes **L303/L306**, prevent modulation of the VCOs by the 5.00kHz or 6.25kHz reference energy remaining at the output of the loop filter. Direct FM is obtained for modulating frequencies outside the PLL bandwidth by applying the CTCSS/DCS signals and the pre-emphasized, limited microphone audio to the VCO modulation circuit. The modulation circuit consists of **R310**and **C324**.

TRANSMITTER SECTION

RF POWER Amplifier

After the PTT is pressed, the **TX6** line switches to approximately 6V. **Q304** is turned on enabling transmit VCO. The VCO buffer, pre-driver, driver and power amplifier are biased on by **Q404** and **Q304**. RF output from the transmit VCO(**Q303**) is applied to the VCO output buffer **Q307**.

Output from **Q307** feeds the buffer **Q308**. The output signal from **Q308** feeds the pre-driver amplifier **Q401**, and feeds the driver amplifier **Q402**, whose output from the driver stage feeds the final RF power amplifier **Q403** to produce the rated output power of 4Watts. The output of the final is applied to a low-pass filter (**C414-C421**, **C428**, **L418** and **L419**) and then to the transmit/receive switch **D101**. RF power is then fed to the antenna via the output low-pass filter consisting of **C101-C105**, **L101-104**.

Antenna Switching

Switching of the antenna between the transmitter and the receiver is accomplished by the antenna transmit/receive switch consisting of diodes **D101** and **D102**. In the transmit mode, switched **TX6** is applied through **R410** and RF choke **L408**, hard forward biasing the two diodes on. **D101** thus permits the flow of RF power from output of the low-pass filter.

L105 and **C105** are preventing receiver circuit from Tx power input.

POWER CONTROL

Output power is controlled by the microprocessor (**IC801**), the D/A converter (**IC803**), the dual Op-Amp (**IC401**), which is used as a differential amplifier and comparator.

Current is sensed by the voltage drop across **R412**.

When the radio Hi power mode, this voltage is compared to D/A converter voltage at the 4-watt.

When the radio Low power mode, this voltage is compared to D/A converter voltage at the 1-watt.
The power output is then reduced or increased by varying the applied voltage to the gate of the power amplifier **Q402, Q403.**

Transmitter Audio Circuits

The transmitter audio circuits consist of the audio processing circuits, the CTCSS circuits and the DCS circuits.

Audio Processing

Transmit speech audio is providing by either the internal electric microphone **M1001** or the external microphone.
The audio is pre -emphasized by 6dB per octave by **C506** and **R508**, and then signal amplification.
The microphone audio is applied to amplifier **IC501A, IC502A** and High-pass filter **IC502B, 502C** and **IC602D**.
IC503 has limiting function and low-pass filter **IC504B, IC504A**.
The MOD. ADJ. is done by **IC803** which applied to a four-pole active low-pass filter.
The resulting signal is then limited and is applied to low pass filter (-18dB per octave roll-off above 3KHz).
The audio is then applied through the 25KHz/12.5KHz channel spacing SW **IC803** to varactor diode **D302** in transmit VCO.
By varying the voltage on the varactor diode **D302** at an audio rate, VCO output is frequecy-modulated.

CTCSS Tone Encoder / Digital Code Squelch (DCS) Encoder

CTCSS signals and DCS signals are synthesized by microprocessor **IC801** and appear as pulse waveform on **IC803** Pin2(DCS),Pin3(CTCSS). This output line is applied to a digital-to-analog converter network (consisting of **R501-R504**, **C501-C502**) which produces a pseudo-sine wave at its output. The waveform is smoothed by low pass filters **IC501D** to produce an acceptable sine wave output. The CTCSS tone signal is adjust to the proper level by **RV301**.

RECEIVER SECTION

Receiver Front End

In the receive mode, the RF signal enters thorough the antenna, then through the low-pass filter **C101**-**C105**, and **L101**-**L104**. The diodes **D101** and **D102** are biased off so that the output of the low-pass filter is coupled (**L105** and **IC102**) to the first band-pass filter **C106**-**C108**, **C110,112,113,129**, **L107-110**, **D103**, **D104R101,R102**.
The signal from the band-pass filter is applied to the input of the RF amplifier **Q101**.
The output of the RF amplifier feeds the input to three more stages of band-pass filters consisting of **C115**-**C118**, **C122**, **L112**-**L114**, **D105, D106** and **R107**. The output from the band-pass filter is applied to the mixer's **Q102**.

Local Oscillator (LO)

The Receive VCO (**C344-C351**, **L302**, **L305**, **L306**, **L312-L314**, and **Q311**, **Q324**.) provides the LO signal. The VCO is running at 45.1 MHz above the desired receive frequency and is applied to output Buffer **Q308**/**Q416**. The output of the buffer through the low-pass filter **C430**, **C431**, **L409** and applied to the mixer **Q407/L408**.

Mixer

The mixer is a FET type (**Q102**). The mixer LO frequency is 45.1 MHz above the desired receiver frequency.
When the receiver frequency is present, the mixer output will be a 45.1MHz signal. The mixer output is peaked for 45.1MHz at **L116**, **C125** , **R115** and **R201**, and the signal is filtered by crystal filter **F201,F202** and amplified by **Q201** before being applied to the input of the IF IC **IC201**.
The 45.1MHz IF signal and LO frequency of 44.645 MHz (PLL) are mixed in **IC201**. The 455kHz ceramic filter **F203** or **F204** filter the second mixer's output. The resulting signal is the second IF signal. The mixer's output is then fed to the internal limiting amplifier and then on to the FM decoder.

FM Detector and Squelch

The FM detector output is used for squelch, decoding tones and audio output.
The squelch amplifier is inside of **IC201** and its output is fed to an internal rectifier and squelch detector.
The output on **IC201** Pin 26 signals the microprocessor **IC801** with a low (0V) to unmute the radio.
The audio is unmuted by the microprocessor **IC801** Pin 48 switching to a high (3.3V) thus biasing on **Q803**.
The audio is then routed to the audio amplifier **IC805**.

Receiver Audio Circuit

The detector's audio output also is fed to the tone (CTCSS and DCS) low-pass filter **IC202D**.
Then the output of the low-pass filter is routed to the second stage filter **IC202C**. The output of Q505B is passed to Q505C input. The output of **IC202B** is applied to the squaring circuit **IC202A** and finally to the microprocessor **IC801** Pin51 for decoding.

The detector output feeds the audio high-pass filter **IC202**. The output of the audio high-pass filter feeds the Volume Control **SW901** (VOL). From the wiper arm on the Volume Control, the input to the audio power amplifier Pin4 of **IC805**. The output of the audio power amplifier is routed through the **CN1002** to the internal speaker **SP1001**.

BATTERY SECTION

The battery connects to the contactor (**CN701**). The positive terminal of the battery connects to the ON/OFF Volume control switch (**SW901**) and the negative terminal connects to PWB ground.
Low battery sense **R701**/**R702**, voltage regulator **IC701**.

Battery voltage status is monitored by the microprocessor **IC801** through **R701**/**R702**.
When the battery voltage goes down, the output is inputted into the Pin59 of the microprocessor **IC801**.