GDL88

Minimum Performance Specification Test Procedure

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Dwg. Number:
004-00294-00 Rev. 2

	Approvals	Date
Drawn	DLE	12/06/10
Chkd.	CEP	12/06/10
Proj. Mgr.	TGH	12/06/10
Released	MKD	12/07/10

File Type: MS Word

Rev.	Date	Description of Change	ECO #
1	12/06/10	Initial Release	------
2	4/18/11	Minor Corrections	80715

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1. PURPOSE

This document shall specify the performance of the GDL88 family of appliances:

- 011-02369-00, GDL88
- 011-02370-00, GDL88 w/ Internal WAAS
- 011-02371-00, GDL88D
- 011-02372-00, GDL88D w/ Internal WAAS

This document specifies the test methods to be used to verify the product. It should be used to design the test equipment. The requirements these tests and specifications were derived from can be found in the GDL88 Hardware Requirements Document (005-00358-36). The actual manufacturing, calibration, and test procedures shall be designed to assure that the unit meets the specifications of this document.

2. STANDARDS

2.1 APPLICABILITY

Unless otherwise noted, all specifications cover the entire design range of supply voltages, signal loads, and standard environmental conditions.

2.2 REGULATORY DOCUMENTS

Refer to the GDL88 Hardware Requirements Document (005-00358-36).

2.3 STANDARD LOADS AND TOLERANCES

All tolerances and load impedances are ±5% unless otherwise specified. The test tolerances listed in the acceptance criteria in some tests may be tighter tolerance than the specified system or hardware requirement. This may be done because the circuit easily exceeds the required tolerances (to give a better indication of any component problems), or to provide additional margin for the tested specification (to better insure against aging or environmental stresses the appliance may undergo).

2.4 TSO CATEGORIES AND CLASSES

TSO/ETSO	Category	Class	Notes
TSO-C154c	UAT	Class A1S	GDL88 Only
TSO-C154c	UAT	Class A1H	GDL88D Only
TSO-C166b	1090ES	Class A1 Receive Only	
TSO-C195	ASAS	Class C1, C2, C3, C4	
TSO-C145c	GPS	BETA 2	

2.5 STANDARD TERMS

Refer to the GDL88 Hardware Requirements Document (005-00358-36).

2.6 SIGNAL SPECIFICATIONS

Unless otherwise specified, all tests will be performed with the input as follows:

Aviation Power: +27.5 ± 0.5VDC

Signal specifications shall be provided with the test wherever applicable.

3. TEST CONDITIONS

3.1 CALIBRATION

The appliance must be calibrated before the test procedures are run. During manufacturing test, the calibration may be combined with the test procedures in a common temperature cycle, if desired.

3.1.1 Initial VCO Calibration

This procedure learns the preliminary frequency resolution VCO per output step of the DAC. This resolution is used to build the VCO Temperature Table in the next procedure. This procedure shall be run at ambient temperature before running the VCO Temperature Table procedure.

1. Provide a valid 1PPS or WAAS signal to the appliance.
2. Disable the PPS phase and frequency adjustment.
3. Force the appliance state to “UTC Coupled”.
4. Start the built-in software VCO calibration routine.

3.1.2 VCO Temperature Table

This procedure produces a preliminary table of VCO frequency shift versus temperature. This table is used to maintain the VCO at 25MHz in the event that a valid 1PPS is not available to the appliance. The appliance will build the table automatically during this procedure.

1. Provide a valid 1PPS or WAAS signal to the appliance.
2. Set the appliance state to “UTC Coupled”.
3. Sweep the ambient temperature at 2°C/min or less across the entire operating temperature range of the appliance.

3.1.3 Transmitter Temperature Table

This procedure produces a calibrated table of transmitter control settings versus temperature. This table is used to keep the appliance transmitter within the TSO-defined power limits.

1. Sweep the temperature at 2°C/min or less across the temperature range -45°C to 95°C, as reported by the test mode software.
2. At 15°C intervals or less, find the digital potentiometer settings (letting DAC1=DAC2) required to output 46.5 ± 0.15dBm from each antenna.
3. At each interval, record the digital potentiometer settings for each antenna.

3.1.4 MTL Temperature Table

This procedure produces a preliminary table of 1090 receiver MTLs versus temperature. This table is used to ensure the 1090 receiver will receive messages at the sensitivity level without being triggered by noise.

1. At ambient, cold, and hot temperatures find the highest MTL that guarantees −83dBm messages are received at a 90% rate.
2. At the same temperatures, find the lowest MTL that results in a thermal noise trigger rate of 1 message per second or less.
3. Store the final calibration curve, using each temperature and the average of its two MTLs.

3.1.5 1090 Receiver Gain

This procedure learns the nominal gain of the 1090 receiver ADC. This value is used to attune the FPGA’s retriggering threshold with the hardware. This procedure shall be run at ambient temperature.

1. Average the perceived signal level for a −30dBm 1090 message, with at least 3 samples.
2. Average the perceived signal level for a −50dBm 1090 message, with at least 3 samples.
3. Store the final calibration value, using one-half the difference between the two averages.

3.1.6 UAT Hardware Delays

These values compensate for the internal path delays in the UAT transmitter and receiver. These values are programmed in manufacturing to allow hardware updates without software changes.

1. Store 521.76µs for the UAT transmitter delay.
2. Store 45.36µs for the UAT receiver delay.

3.2 COVERS AND SHIELDS

All tests shall be performed with the final assembled appliance. All shields and covers shall be installed unless otherwise stated.

3.3 ENVIRONMENTAL CONDITIONS

The certification environmental conditions are specified in the GDL88 Environmental Qualification Form (005-00358-20). The following temperatures and tolerances were derived from guidance in DO-160F, and apply to TSO compliance testing.

Ambient Temperature	25 ± 10°C
Operating High Temperature	70 ± 3°C
Operating Low Temperature	−45 ± 3°C

The appliance must be soaked for sufficient time to bring the internal temperature within the desired temperature range before conducting compliance tests.

The production environmental conditions are specified in the GDL88 Test Methodology (005-00650-00).

3.4 TEST MODE

All tests specified in this document are conducted using the built-in test mode, unless otherwise specified. The appliance can be placed in test mode by grounding the *Test Mode* discrete input on the appliance 78−pin connector. In order to access test mode, versions of the Boot Block, Application Software, and Main FPGA approved on the appliance Configuration Index must be loaded into nonvolatile memory.

3.5 TEST SETUP

All tests shall be conducted with the 12’ GDL88 Environmental Cable (320-00399-00), unless otherwise specified.

4. PIN FUNCTIONS

4.1 REAR CONNECTOR, J2201

This is a 78−pin DSUB connector, GPN 330-00063-78

Pin #	I/O	Name	Comment
1		Spare	
2	O	232 Port 5 Transmit	
3	I/O	PPS Low Port 1	Differential or Ground
4	O	Audio High	AC-Coupled
5	O	232 Port 4 Transmit	
6	O	232 Port 3 Transmit	
7	O	232 Port 2 Transmit	
8	O	232 Port 1 Transmit	
9	I/O	PPS Low Port 2	Differential or Ground
10	O	429 Port 1 Transmit A	
11	O	429 Port 2 Transmit A	
12	I	Fan Tach	
13	O	Discrete Output 3	
14	O	Discrete Output 1	
15	O	Discrete Output 2	
16	I	Discrete Input 1	
17	I	Remote Off	Ground to turn ON
18		Ground	
19	I	Aviation Power	+9V to +33V
20	I	Aviation Power	+9V to +33V
21	I	232 Port 5 Receive	
22	I/O	PPS High Port 1	Differential or Single
23		Audio Ground	
24	I	232 Port 4 Receive	
25	I	232 Port 3 Receive	
26	I	232 Port 2 Receive	
27	I	232 Port 1 Receive	
28	I/O	PPS High Port 2	Differential or Single
29	O	429 Port 1 Transmit B	
30	O	429 Port 2 Transmit B	
31	O	Fan Power	+5V
32	I	422 Port 2 Receive A	
33	I	422 Port 2 Receive B	
34	O	422 Port 2 Transmit A	
35	O	422 Port 2 Transmit B	
36	I	Discrete Input 2	
37	I	Discrete Input 3	
38	I	Discrete Input 4	
39	I	Discrete Input 5	

Pin #	I/O	Name	Comment
40		232 Port 5 Ground	
41		USB Ground	
42	I	USB VBus	+5V
43		232 Port 4 Ground	
44		232 Port 3 Ground	
45		232 Port 2 Ground	
46		232 Port 1 Ground	
47	I	429 Port 2 Receive A	
48	I	429 Port 1 Receive A	
49	I	429 Port 3 Receive A	
50		Ground	
51	I	Ethernet 1 Receive A	
52	I	Ethernet 1 Receive B	
53	O	Ethernet 1 Transmit A	
54	O	Ethernet 1 Transmit B	
55		Discrete Output 4	
56	O	422 Port 1 Transmit A	
57	I	422 Port 1 Receive A	
58	I	Discrete Input 6	Test Mode
59	O	1090 Suppress	
60	I/O	USB D-	
61	I/O	USB D+	
62	I/O	I2C Data	
63	O	I2C Clock	
64		I2C Ground	
65	O	I2C Power	+3.3V
66	I	429 Port 2 Receive B	
67	I	429 Port 1 Receive B	
68	I	429 Port 3 Receive B	
69		Ground	
70	I	Ethernet 2 Receive A	
71	I	Ethernet 2 Receive B	
72	O	Ethernet 2 Transmit A	
73	O	Ethernet 2 Transmit B	
74		Spare	
75	O	422 Port 1 Transmit B	
76	I	422 Port 1 Receive B	
77		Ground	Aviation Ground
78		Ground	Aviation Ground

Table 1: Rear Connector Pinout

4.2 MAIN/RF CONNECTOR, J2301

This is a 2x25−pin, 0.1” pitch rectangular socket, GPN 335-00166-50

Pin #	I/O*	Name	Comment
1		Ground	
2	O	25 MHz Clock	RF Synthesizer input
3	I	RF Version	Fixed analog voltage
4		Ground	
5	I/O	I2C Data	Digipot control only
6	O	I2C Clock	Digipot control only
7	O	Synthesizer Data	
8	O	Synthesizer Clock	
9	O	Synthesizer Latch	
10	I	Synthesizer Lock Detect	
11		Spare	
12	O	Transmit PA Enable	
13		Ground	
14		Ground	
15	I	1090 RX-	
16		Ground	
17	I	1090 RX+	
18		Ground	
19		Ground	
20		Ground	
21	I	UAT RX-	
22		Ground	
23	I	UAT RX+	
24		Ground	
25		Ground	
26		Ground	
27		Ground	
28		Ground	
29	O	UAT TX+	
30		Ground	
31		Ground	
32		Ground	
33	O	1030 Modulation	
34	O	5V Switch Enable	
35	O	Mode S TX Data	
36	O	Auxiliary Control	
37	O	+6V	
38		Ground	
39	O	+12V	
40		Ground	

Pin #	I/O*	Name	Comment
41	O	+5V	
42		Ground	
43	O	Antenna Select	
44		Ground	
45	O	+VTX	
46	O	+VTX	
47	I	Bottom Antenna Test	
48	I	Bottom Power Detect	
49	I	Top Antenna Test	
50	I	Top Power Detect	

** From main board perspective*

Table 2: Main Board to RF Board Connector

4.3 MAIN/WAAS CONNECTOR, J2104

This is a 2x6−pin, 0.1” pitch rectangular socket, GPN 335-00097-06

Pin #	I/O*	Name	Comment
1	O	Battery	+3.6V
2	O	Power	+5V
3		Ground	
4		Spare	
5		Spare	
6	I	1PPS Input	
7		Ground	
8	I	GPS Receive	
9	O	GPS Transmit	
10		Ground	
11	I	LAAS Receive	Unused
12	O	LAAS Transmit	Unused

** From main board perspective*

Table 3: Main Board to WAAS Module Connector

4.4 RF TOP CONNECTOR

In appliances designated GDL88/D, this is a female BNC connector, GPN 325-00100-00

4.5 RF BOTTOM CONNECTOR

In all appliances, this is a female BNC connector, GPN 325-00100-00

4.6 RF WAAS CONNECTOR

In appliances with internal WAAS, this is a female BNC connector, GPN, 325-00241-01

5. TESTS

5.1 RESERVED

5.2 RESERVED

5.3 GENERAL

5.3.1 [GEN100] Appliance Serial Number

Test Method: Read the appliance *Serial Number* using the test mode interface.

Note: If the appliance serial number has never been programmed in nonvolatile memory, first program it using the test mode interface, then reboot the appliance.

Acceptance: [GEN100a] The appliance *Serial Number* **shall** match the printed serial number sticker on the chassis exterior.

Reference: SRD R00232637

5.3.2 [GEN110] Appliance Version Numbers

Test Method: Read the following information using the test mode interface.

Acceptance: [GEN110a] The *Main FPGA* part number **shall** match the part number listed in the appliance BOM.

[GEN110b] The *Main FPGA* version number **shall** be one of the valid version numbers listed in the Configuration Index.

[GEN110c] The *Boot Block* part number **shall** match the part number listed in the appliance BOM.

[GEN110d] The *Boot Block* version number **shall** be one of the valid version numbers listed in the Configuration Index.

[GEN110e] The *Application Software* part number **shall** match the part number listed in the appliance BOM.

[GEN110f] The *Application Software* version number **shall** be one of the valid version numbers listed in the Configuration Index.

[GEN110g] If an internal WAAS module is installed, the *WAAS Software* part number **shall** match the part number listed in the appliance BOM.

[GEN110h] If an internal WAAS module is installed, the *WAAS Software* version number **shall** be one of the valid version numbers listed in the Configuration Index.

Reference: SRD R00232608, R00232614, R00232616, R00232625, R00232627, R00232629, R00232675, R00232676

5.3.3 [GEN120] Internal Temperature

Test Method: Power the appliance off and soak in a stable temperature environment for at least 10min. Power the appliance on and read the temperature using the test mode interface within 5s after the test mode interface connects.

Acceptance: [GEN120a] The appliance temperature **shall** be within ±5°C of ambient.

Reference: HRD R00033080

5.3.4 [GEN130] Assembly Code

Test Method: Read the appliance assembly code using the test mode interface.

Acceptance: [GEN130a] Each “0” in the 4-bit appliance code **shall** correspond to a populated resistor in R1001, R1003, R1005, and R1007 (MSB to LSB) in the appliance BOM.

[GEN130b] Each “1” in the 4-bit appliance code **shall** correspond to an unused resistor in R1001, R1003, R1005, and R1007 (MSB to LSB) in the appliance BOM.

Reference: HRD R00031020

5.3.5 [GEN140] Hardware Revisions

Test Method: Read the appliance hardware codes using the test mode interface.

Acceptance: [GEN140a] The Main hardware **shall** match the version in the appliance BOM.

[GEN140b] The RF hardware **shall** match the version in the appliance BOM.

[GEN140c] The WAAS hardware **shall** match the version in the appliance BOM.

Reference: HRD R00033060, R00033070; SRD R00232776

5.3.6 [GEN150] GPS Information

Test Method: If the appliance has an internal WAAS module, connect a GPS data source to the WAAS Antenna and allow the WAAS module to acquire a GPS fix (typically 5min). Read the current GPS information using the test mode interface.

Acceptance: [GEN150a] The GPS time/date field **shall** match the GPS source time/date.

[GEN150b] The GPS latitude/longitude **shall** match the GPS source position.

[GEN150c] The GPS navigation fix status **shall** be “3D fix”.

Reference: HRD R00031080; SRD R00250710, R00250715, R00250714

5.3.7 [GEN160] Operating history

Test Method: Record each of the following operating history values using the test mode interface, after the appliance has been on at least 2min. Power the appliance off. Power the appliance on again and record each of the operating history values again using the test mode interface, after the appliance has been on at least 2min.

Acceptance: [GEN160a] The appliance **shall** provide a power up event counter that is incremented by 1 over the first recorded value.

[GEN160b] The appliance **shall** provide the elapsed operating time that is greater than the operating time of the first recorded values.

[GEN160c] The appliance **shall** provide a lifetime maximum temperature greater than or equal to the current reported ambient temperature.

[GEN160d] The appliance **shall** provide a lifetime minimum temperature less than or equal to the current reported ambient temperature.

[GEN160e] The appliance **shall** provide a lifetime average temperature less than the lifetime maximum and greater than the lifetime minimum temperatures.

Reference: SRD R00253573, R00253574, R00253671, R00253672

5.3.8 [GEN170] Temperature reset

Test Method: Command the appliance to reset the operating temperature values using the test mode interface. Reboot the appliance and read the operating history values and the current appliance temperature using the test mode interface within 1m.

*Note: Always run this test **after** running* **[GEN160]** *during production test.*

Acceptance: [GEN170a] The appliance lifetime maximum temperature **shall** be within ±5°C of the current appliance operating temperature.

[GEN170b] The appliance lifetime minimum temperature **shall** be within ±5°C of the current appliance operating temperature.

[GEN170c] The appliance average operating temperature **shall** be less than the lifetime maximum and greater than the lifetime minimum temperatures.

Reference: SRD R00239919

5.3.9 [GEN180] Clock Accuracy

Test Method: Connect an external PPS source with <100ns pulse jitter to the appliance and configure it as the primary PPS source using the test mode interface. Allow the appliance to idle for at least 30s, and read the 25MHz clock frequency using the test mode interface.

Acceptance: [GEN180a] The clock frequency **shall** be 25MHz ± 5Hz.

Reference: HRD R00032060

5.3.10 [GEN210] Processor RAM

Test Method: Execute each of the following tests using the test mode interface.

Acceptance: [GEN210a] The processor RAM **shall** pass the test.

Reference: SRD R00229812

5.3.11 [GEN230] Configuration Module

Test Method: Send a valid read or write command to the configuration module on the I2C bus.

Acceptance: [GEN230a] Reception of the command result **shall** be successfully confirmed by the configuration module.

Reference: SRD R00230109

5.3.12 [GEN240] Global Reset Startup

Test Method: Power the appliance off and remove the appliance cover. Observe the *Aviation Power* and *Global Reset* signals after applying +28V to Aviation Power.

Acceptance: [GEN240a] The *Global Reset* signal **shall** be asserted before the appliance is powered on.

[GEN240b] The *Global Reset* signal **shall** remain asserted at least 100ms after *Aviation Power* has reached +14V.

Reference: HRD R00031050, R00032040

5.3.13 [GEN250] Watchdog Timer | Full

Test Method: Remove the appliance cover and observe the *Watchdog Control* signal and *Global Reset* signal. Disable the appliance software from watchdog control module using the test mode interface, and search for the assertion of the *Global Reset* signal.

Acceptance: [GEN250a] The time between the last transition on the *Watchdog Control* signal and the assertion of the *Global Reset* signal **shall** be less than 2.0s.

[GEN250b] The *Global Reset* signal **shall** remain asserted for at least 100ms before de-assertion.

Reference: HRD R00031030, R00032040, R00034020

5.3.14 [GEN255] Watchdog Timer | Fast

Test Method: Disable the appliance software from watchdog control module using the test mode interface.

Acceptance: [GEN255a] The PC-side test mode interface software **shall** report a communication error within 3 seconds after sending the command.

Reference: HRD R00034020

5.3.15 [GEN260] Watchdog Timer Input

Test Method: Remove the appliance cover and temporarily disconnect the *Watchdog Control* signal from the CPU. Input a signal that conforms to the following characteristics on the watchdog side of the broken *Watchdog Control* signal. Observe the behavior of the *Global Reset* signal.

- The signal shall remain low for at least 1.1s.
- The signal shall transition high for 90ns, then transition low again.
- The signal shall remain low for 1.1s, then transition high for another 1.1s.
- The signal shall transition low for 90ns, then transition high again.
- The signal shall remain high for 1.1s, then transition low for another 1.1s.

Repeat the signal sequence from step 2 for at least 10 cycles. Reconnect the *Watchdog Control* signal to the CPU after the test is complete.

Acceptance: [GEN260a] *Global Reset* signal **shall** become de–asserted within 1ms after the initial low-to-high transition.

[GEN260b] The *Global Reset* signal **shall** remain de-asserted for the entire test.

Reference: HRD R00032020, R00032030

5.3.16 [GEN270] Watchdog Power Input

Test Method: Remove the appliance cover. For each of the indicated power supplies, connect a variable current load to the supply output. Beginning with 0mA load, gradually increase the load on the indicated supply until the *Global Reset* signal asserts. Immediately measure the output voltage of the power supply. Remove the load, allow the *Global Reset* signal to de-assert, and apply a short circuit between the output of the indicated power supply and *Ground*.

Acceptance: [GEN270a] *3.3V Supply*: The voltage **shall** be above 2.97V when the *Global Reset* signal asserts for the first time.

[GEN270b] *3.3V Supply*: The time between the application of the short circuit and the assertion of the *Global Reset* signal **shall** be less than 50µs.

[GEN270c] *2.5V Supply*: The voltage **shall** be above 2.25V when the *Global Reset* signal asserts for the first time.

[GEN270d] *2.5V Supply*: The time between the application of the short circuit and the assertion of the *Global Reset* signal **shall** be less than 50µs.

[GEN270e] *1.8V Supply*: The voltage **shall** be above 1.62V when the *Global Reset* signal asserts for the first time.

[GEN270f] *1.8V Supply*: The time between the application of the short circuit and the assertion of the *Global Reset* signal **shall** be less than 50µs.

[GEN270g] *1.3V Supply*: The voltage **shall** be above 1.17V when the *Global Reset* signal asserts for the first time.

[GEN270h] *1.3V Supply*: The time between the application of the short circuit and the assertion of the *Global Reset* signal **shall** be less than 50µs.

[GEN270i] *1.2V Supply*: The voltage **shall** be above 1.08V when the *Global Reset* signal asserts for the first time.

[GEN270j] *1.2V Supply*: The time between the application of the short circuit and the assertion of the *Global Reset* signal **shall** be less than 50µs.

Reference: HRD R00032020, R00032030

5.3.17 [GEN280] Antenna Self-Test

Test Method: Enable the internal antenna detection self-test for the indicated antenna using the test mode interface. Use a DC-grounded antenna, follow the instructions.

Acceptance: [GEN280a] Connect the antenna to the *Top Antenna* port: the top antenna test **shall** pass.

[GEN280b] Disconnect the antenna from the *Top Antenna* port: the top antenna test **shall** fail.

[GEN280c] Connect the antenna to the *Bottom Antenna* port: the bottom antenna test **shall** pass.

[GEN280d] Disconnect the antenna from the *Bottom Antenna* port: the bottom antenna test **shall** fail.

Reference: HRD R00033130, R00033140

5.4 MECHANICAL

5.4.1 [MEC100] Appliance Weight

Test Method: Disconnect the test cable harness and attach an empty connector backshell assembly to the appliance. Weigh the appliance.

Acceptance: [MEC100a] The measured weight **shall** be strictly less than 4lb.

Reference: HRD R00042010

5.4.2 [MEC110] Appliance Dimensions

Test Method: Disconnect the test cable harness and attach an empty connector backshell assembly to the appliance. Measure the height, width, and depth of the appliance.

Acceptance: [MEC110a] The maximum depth of the appliance **shall** be strictly less than 7.500in, measured orthogonal to the 78-pin connector's plane.

[MEC110b] The maximum width of the appliance **shall** be strictly less than 6.250in, measured parallel to the 78-pin connector's major axis.

[MEC110c] The maximum height of the appliance **shall** be strictly less than 1.625in, measured parallel to the 78-pin connector's minor axis.

Reference: HRD R00042020, R00042030, R00042040

5.4.3 [MEC120] Remote Rack Width

Test Method: Disconnect the test cable harness and place the appliances in the remote rack assembly. Attach an empty connector backshell assembly to the rack. Measure the width of the entire assembly.

Acceptance: [MEC120a] The maximum width of the entire assembly **shall** be strictly less than 6.300in, measured parallel to the 78-pin connector's major axis.

Reference: HRD R00042050

5.4.4 [MEC130] Modular Rack Width

Test Method: Disconnect the test cable harness and place the appliances in the modular rack assembly. Attach an empty connector backshell assembly to the rack. Measure the width of the entire assembly.

Acceptance: [MEC130a] The maximum width of the entire assembly **shall** be strictly less than 6.300in, measured parallel to the 78-pin connector's major axis.

Reference: HRD R00042060

5.5 POWER

5.5.1 [PWR100] External Supply Voltage

Test Method: Set the nominal *Aviation Power* source to the indicated voltage, and read the appliance input voltage level using the test mode interface.

Acceptance: [PWR100a] 9.5V: The voltage **shall** be 9.0 ± 0.45V.

[PWR100b] 33.0V: The voltage **shall** be 33.0 ± 1.65V.

Reference: HRD R00052010, R00053020

5.5.2 [PWR110] Power On Time

Test Method: Set *Aviation Power* less than 1.0V for at least 1.0s, then set it to the indicated voltage and wait for the test mode interface to connect

Acceptance: [PWR110a] 9.5V: The connection **shall** start within 10s after power is applied.

[PWR110b] 33.0V: The connection **shall** start within 10s after power is applied.

Reference: Derived

5.5.3 [PWR120] Power Consumption

Test Method: Set *Aviation Power* to the indicated voltage and calculate the power consumption of the device using

$$P = V_{source} \cdot I_{source}$$

Acceptance: [PWR120a] 9.5V: The steady-state power consumption **shall** be less than 20W.

[PWR120b] 33.0V: The steady-state power consumption **shall** be less than 20W.

Reference: HRD R00052020

5.5.4 [PWR140] Power Interrupt | Full

Test Method: Remove the appliance cover and observe *Aviation Power*, *+5.0V Supply* output, and the *Global Reset* signal. Set *Aviation Power* to the indicated voltage, and generate at least 2 power interruptions of 215ms to 225ms in length that repeat at an interval of 2.90s to 3.10s.

Acceptance: [PWR140a] 9.0V: The *+5.0V Supply* output **shall not** drop below 4.75V at any point during the test.

[PWR140b] 9.0V: The *Global Reset* signal **shall not** become asserted at any point during the test.

[PWR140c] 33.0V: The *+5.0V Supply* output **shall not** drop below 4.75V at any point during the test.

[PWR140d] 33.0V: The *Global Reset* signal **shall not** become asserted at any point during the test.

Reference: HRD R00052070, R00052080, R00053040

5.5.5 [PWR145] Power Interrupt | Fast

Test Method: Set *Aviation Power* to the indicated voltage, and generate at least 2 power interruptions of 215ms to 225ms that repeat at an interval of 2.90s to 3.10s for the indicated voltages.

Acceptance: [PWR145a] 9.5V: The appliance **shall** operate normally.

[PWR145b] 33.0V: The appliance **shall** operate normally.

Reference: Derived

5.5.6 [PWR150] Internal Supply Voltages

Test Method: Verify that each of the following power supply levels using the test mode interface. Each power supply output voltage **shall** fall within the indicated voltage range.

Acceptance:

[PWR150a]	*VTX Supply*:	26.60V	to	29.40V	
[PWR150c]	*+12V Supply*:	11.40V	to	12.60V	
[PWR150d]	*−12V Supply*:	−11.40V	to	−12.60V	
[PWR150e]	*6.0V Supply*:	5.70V	to	6.30V	
[PWR150f]	*5.0V Supply*:	4.75V	to	5.25V	
[PWR150g]	*3.3V Supply*:	3.14V	to	3.46V	
[PWR150h]	*2.5V Supply*:	2.38V	to	2.63V	
[PWR150i]	*1.8V Supply*:	1.71V	to	1.89V	
[PWR150j]	*1.3V Supply*:	1.24V	to	1.36V	
[PWR150k]	*1.2V Supply*:	1.14V	to	1.26V	
[PWR150l]	*0.9V Supply*:	0.86V	to	0.94V	
[PWR150m]	*Battery*:	3.40V	to	3.80V	[Only with internal WAAS]
[PWR150n]	*WAAS AGC*:	0.20V	to	1.80V	[Only with internal WAAS]

Reference: HRD R00051050, R00052030, R00053030; SRD R00250713

5.5.7 [PWR160] Internal Current Limit

Test Method: Create an intentional short circuit between the *5.0V Supply* and *Ground*. Measure the current provided by *Aviation Power* for each of the indicated *Aviation Power* voltages.

Note: It is acceptable for the test mode interface program to lose communication.

Acceptance: [PWR160a] 9.5V: The current **shall** be at most 4.0A.

[PWR160b] 33.0V: The current **shall** be at most 2.0A.

Reference: HRD R00054030

5.5.8 [PWR170] Battery Current

Test Method: If an internal WAAS module is installed, remove the appliance cover and measure across R2109.

Acceptance: [PWR170a] The voltage **shall** be less than 8.0mV when the appliance is on.

[PWR170b] The voltage **shall** be less than 0.8mV when the appliance is off.

Reference: HRD R00052050, R00052060

5.5.9 [PWR180] Battery Safety

Test Method: If an internal WAAS module is installed, remove the appliance cover and measure the current through an intentional short between *Battery* and *Ground* for at least 10s under each of the following conditions.

Acceptance: [PWR180a] Appliance Off: the maximum absolute value of the current **shall** be less than 35 mA.

[PWR180b] Appliance On, after 30s: the maximum absolute value of the current **shall** be less than 35 mA.

Reference: HRD R00054010

5.5.10 [PWR190] Battery Charging

Test Method: If an internal WAAS module is installed, remove the appliance cover and disconnect the internal WAAS module to prevent damage. Connect an external DC power supply of the indicated voltage to *Battery* and measure the voltage between *Battery* and *Ground* for the following conditions.

Acceptance: [PWR190a] 0.5V: The voltage at the *Battery* terminal **shall** be 3.60V to 3.80V.

[PWR190b] 3.5V: The voltage at the *Battery* terminal **shall** be 3.60V to 3.80V.

[PWR190c] 10.0V: The voltage at the *Battery* terminal **shall** be 3.60V to 3.80V.

Reference: HRD R00054020

5.5.11 [PWR200] Power Supply Sync

Test Method: Remove the appliance cover and measure the frequency and duty cycle of the *Power Supply Sync* signal.

Acceptance: [PWR200a] The frequency of *Power Supply Sync* **shall** be 405.8kHz ± 40Hz.

[PWR200b] The duty cycle of *Power Supply Sync* **shall** be 85 ± 1% on time.

Reference: HRD R00152020, R00152030

5.5.12 [PWR210] Remote Power Control | Full

Test Method: Test each of the following networks connected to the *Remote Off* control pin on the appliance rear connector

Acceptance: [PWR210a] 11kΩ connected to *Ground*: The appliance **shall** power on.

[PWR210b] 190kΩ connected to *Ground*: The appliance **shall** power off.

[PWR210c] +3.7V referenced from *Ground*: The appliance **shall** power on.

[PWR210d] +6.2V referenced from *Ground*: The appliance **shall** power off.

Reference: HRD R00052110, R00052120

5.5.13 [PWR215] Remote Power Control | Fast

Test Method: Test each of the following networks connected to the *Remote Off* control pin on the appliance rear connector

Acceptance: [PWR215a] *Remote Off* control pin connected to *Ground*: The appliance **shall** power on.

[PWR215b] *Remote Off* control pin open circuit: The appliance **shall** power off.

[PWR215c] *Remote Off* control pin connected to *Aviation Power*: The appliance **shall** power off.

Reference: HRD R00052110, R00052120

5.5.14 [PWR220] Power Fail Interrupt

Test Method: Remove the appliance cover and observe Aviation Power and the Power Fail Interrupt signal. Apply Aviation Power of +28V for at least 10s, reduce the voltage to 7.75V for 100ms, then increase the voltage to 8.75V for at least 10s. Restore Aviation Power to +28V for at least 10s. Using a shunt load, quickly remove Aviation Power for 100ms, then disconnect the shunt and quickly restore +28V.

Acceptance: [PWR220a] The *Power Fail Interrupt* **shall** be asserted after the *Aviation Power* has been reduced to 7.75V.

[PWR220b] The *Power Fail Interrupt* **shall** be de-asserted after the *Aviation Power* has been increased to 8.75V.

[PWR220c] The *Power Fail Interrupt* **shall** be asserted within 1.0ms after *Aviation Power* is removed.

[PWR220d] The *Power Fail Interrupt* **shall** be de-asserted within 1.0ms after *Aviation Power* is restored.

Reference: HRD R00052090, R00052095, R00052100, R00052105

5.5.15 [PWR230] Fan Temp Thresholds

Test Method: Place the appliance in a temperature-controlled environment, powered off, and allow it to soak at +30°C for at least 10min. Power the appliance on and wait 1min. Begin reducing the ambient temperature towards a point below −10°C, and observe both the appliance internal temperature and the fan power control. Power the appliance off and allow it to soak for at least 10min after the ambient temperature reaches −10°C. Power the appliance on and wait 1min. Begin increasing the ambient temperature towards a point above +30°C, and observe both the appliance internal temperature and the fan power control.

Acceptance: [PWR230a] Within 10s after powering on at +30°C ambient temperature, the *Fan Power* output **shall** be enabled.

[PWR230b] Within 10s after the internal temperature sensors indicates 10°C while the temperature is falling, the *Fan Power* **shall** be disabled.

[PWR230a] Within 1min after powering on at −10°C ambient temperature, the *Fan Power* output **shall** remain disabled.

[PWR230c] Within 10s after the internal temperature sensors indicates 20°C while the temperature is rising, the *Fan Power* **shall** be enabled.

Reference: SRD R00491779, R00491785

5.5.16 [PWR240] Fan Output Control | Full

Test Method: Disconnect the appliance fan from the test cable. Set the *Fan Power* output to each indicated state and measure the voltage across a 100kΩ resistor:

Acceptance: [PWR240a] *Fan Power* On: The output voltage **shall** be +5.0 ± 0.5V.

[PWR240b] *Fan Power* Off: The output voltage **shall** be 0.0 ± 0.5V.

Reference: HRD R00052150, R00052160

5.5.17 [PWR245] Fan Output Control | Fast

Test Method: Set the *Fan Power* output to each indicated state and observe the behavior of the appliance external fan.
Note: The fan can be assumed running if the Fan Tach count is greater than 0.

Acceptance: [PWR245a] *Fan Power* On: The fan **shall** be running.

[PWR245b] *Fan Power* Off: The fan **shall not** be running.

Reference: Derived

5.5.18 [PWR250] Fan Output Power

Test Method: Connect a 1Ω resistor between the *Fan Power* output and *Ground*. Measure the voltage across the resistor while the *Fan Power* is enabled

Acceptance: [PWR250a] The measured voltage **shall** be at least 1V.

Reference: HRD R00052200

5.5.19 [PWR260] Fan Output Safety

Test Method: For the indicated pins, sequentially connect the respective rear connector interface pin in the requested configurations, holding at least 10m in each configuration:

- Leave the pin open-circuit (both *Fan Power* and *Fan Tach*)
- Short-circuit the pin to *Ground* (both *Fan Power* and *Fan Tach*)
- Short-circuit the pin to *Fan Power* (*Fan Tach* only)

Acceptance: [PWR260a] Procedures **[PWR240]** and **[PWR300]** **shall** pass after this procedure is completed.

Reference: HRD R00054040, R00054050, R00054060, R00054070, R00054080

5.5.20 [PWR270] GPS Backup Power

Test Method: If the appliance has an internal WAAS module, connect a GPS data source to the *WAAS Antenna* and allow the WAAS module to acquire a GPS fix (typically 5min). Using the test mode interface, record the difference between the UTC time that the appliance reports and the local PC time. Disconnect the *WAAS Antenna* and power the appliance off for at least 1min. Power the appliance on and allow the WAAS module to initialize. Using the test mode interface, again record the difference between the UTC time that the appliance reports and the local PC time.

Acceptance: [PWR270a] Before acquiring 3D fix a second time, the WAAS **shall** report the correct local time, within 1s.

Reference: HRD R00051060

5.5.21 [PWR280] GPS Antenna Bias

Test Method: If the appliance has an internal WAAS module, place a constant-current load between the *WAAS Antenna* connector and *Ground*. Set the load to sink 60mA, then measure the DC voltage at the GPS Antenna.

Acceptance: [PWR280a] The voltage **shall** be at least 4.30V.

Reference: HRD R00052230

5.5.22 [PWR290] RF Board Soft Start

Test Method: For each of the indicated power supplies, observe the voltage at the Main/RF connector as the appliance is powered on and off.

Acceptance: [PWR290a] *+12V Supply*: The transition time between 1.2V and 10.8V as the appliance powers on **shall** be at least 1.0ms.

[PWR290b] *+12V Supply*: The transition time between 10.8V and 1.2V as the appliance powers off **shall** be at least 1.0ms.

[PWR290c] *+6.0V Supply*: The transition time between 0.6V and 5.4V as the appliance powers on **shall** be at least 1.0ms.

[PWR290d] *+6.0V Supply*: The transition time between 5.4V and 0.6V as the appliance powers off **shall** be at least 1.0ms.

[PWR290e] *+5.0V Supply*: The transition time between 0.5V and 4.5V as the appliance powers on **shall** be at least 1.0ms.

[PWR290f] *+5.0V Supply*: The transition time between 4.5V and 0.5V as the appliance powers off **shall** be at least 1.0ms.

Reference: HRD R00052240

5.5.23 [PWR295] RF Board Interruption

Test Method: Remove the appliance cover. Set *Aviation Power* to the indicated voltage, and generate at least 5 interruptions of 240ms to 250ms in length that repeat at an interval of 2.90s to 3.00s. Observe the voltage of the indicated supply at the Main/RF connector 1.0s after *Aviation Power* is restored.

Acceptance: [PWR295a] 9.5V, *+5.0V Supply*: The voltage **shall** be 5.0 ± 0.25V.

[PWR295b] 9.5V, *+6.0V Supply*: The voltage **shall** be 6.0 ± 0.30V.

[PWR295c] 9.5V, *+12V Supply*: The voltage **shall** be 12.0 ± 0.60V.

[PWR295d] 33.0V, *+5.0V Supply*: The voltage **shall** be 5.0 ± 0.25V.

[PWR295e] 33.0V, *+6.0V Supply*: The voltage **shall** be 6.0 ± 0.30V.

[PWR295f] 33.0V, *+12V Supply*: The voltage **shall** be 12.0 ± 0.60V.

Reference: HRD R00164020, R00174050, R00184020, R00194020

5.5.24 [PWR300] Fan Tach. Thresholds

Test Method: Disconnect the appliance fan from the test cable. Input a continuous 6kHz signal with a high voltage of 0.4V, a low voltage of 0.2V, and a duty cycle of 50% into the *Fan Tach* input. Read the number of detected rising edges using the test mode interface.

Acceptance: [PWR300a] There **shall** be at least 100 rising edges per second.

Reference: HRD R00052250, R00052260, R00052270

5.6 DISCRETE

5.6.1 [DSC100] Discrete Input Configuration

Test Method: Read the *Discrete Input* configuration using the test mode interface for each of the following discrete input pins. The appliance **shall** provide the rear connector pin number, the input function, and the current status of the *Discrete Input*.

Acceptance:
- [DSC100a] *Discrete Input 1*
- [DSC100b] *Discrete Input 2*
- [DSC100c] *Discrete Input 3*
- [DSC100d] *Discrete Input 4*
- [DSC100e] *Discrete Input 5*
- [DSC100f] *Discrete Input 6*

Reference: SRD R00253590, R00253593, R00253597

5.6.2 [DSC110] Discrete Input Active

Test Method: Test each of the following *Discrete Input* configurations, using a low impedance voltage source less than 3.5V when “Active” is specified and greater than 6.5V when “inactive” is specified. The status of each Discrete Inputs read using the test mode interface for each configuration **shall** match the provided inputs.

Acceptance:

[DSC110a]	*Discrete Input 1*: Active	*Discrete Inputs 2*, *3*, *4*, *5*, and *6*: Inactive
[DSC110b]	*Discrete Input 2*: Active	*Discrete Inputs 1*, *3*, *4*, *5*, and *6*: Inactive
[DSC110c]	*Discrete Input 3*: Active	*Discrete Inputs 1*, *2*, *4*, *5*, and *6*: Inactive
[DSC110d]	*Discrete Input 4*: Active	*Discrete Inputs 1*, *2*, *3*, *5*, and *6*: Inactive
[DSC110e]	*Discrete Input 5*: Active	*Discrete Inputs 1*, *2*, *3*, *4*, and *6*: Inactive
[DSC110f]	*Discrete Input 6*: Active	*Discrete Inputs 1*, *2*, *3*, *4*, and *5*: Inactive

Reference: HRD R00062010, R00062020

5.6.3 [DSC120] Discrete Input Inactive

Test Method: Test each of the following *Discrete Input* configurations, using a low impedance voltage source less than 3.5V when “active” is specified and greater than 6.5V when “inactive” is specified. The status of each Discrete Inputs read using the test mode interface for each configuration **shall** match the provided inputs.

Acceptance:

[DSC120a]	*Discrete Input 1*: Inactive	*Discrete Inputs 2*, *3*, *4*, *5*, and *6*: Active
[DSC120b]	*Discrete Input 2*: Inactive	*Discrete Inputs 1*, *3*, *4*, *5*, and *6*: Active
[DSC120c]	*Discrete Input 3*: Inactive	*Discrete Inputs 1*, *2*, *4*, *5*, and *6*: Active
[DSC120d]	*Discrete Input 4*: Inactive	*Discrete Inputs 1*, *2*, *3*, *5*, and *6*: Active
[DSC120e]	*Discrete Input 5*: Inactive	*Discrete Inputs 1*, *2*, *3*, *4*, and *6*: Active
[DSC120f]	*Discrete Input 6*: Inactive	*Discrete Inputs 1*, *2*, *3*, *4*, and *5*: Active

Reference: HRD R00062010, R00062020

5.6.4 [DSC130] Discrete Input Thresholds

Test Method: Test the following networks connected to the *Discrete Inputs* as specified. Then read the status of Each *Discrete Input* using the test mode interface. The status for each *Discrete Input* **shall** agree with the designation of the input network.

- "Active A": Low impedance voltage source set to 3.7V.
- "Active B": 400Ω resistor to *Ground*.
- "Inactive A": Low impedance voltage source set to 6.2V.
- "Inactive B": 10kΩ resistor to *Ground*.

Acceptance:

[DSC130a] *Discrete Input 1*: Active A
[DSC130b] *Discrete Input 2*: Active A
[DSC130c] *Discrete Input 3*: Active A
[DSC130d] *Discrete Input 4*: Active A
[DSC130e] *Discrete Input 5*: Active A
[DSC130f] *Discrete Input 6*: Active A
[DSC130g] *Discrete Input 1*: Active B
[DSC130h] *Discrete Input 2*: Active B
[DSC130i] *Discrete Input 3*: Active B
[DSC130j] *Discrete Input 4*: Active B
[DSC130k] *Discrete Input 5*: Active B
[DSC130l] *Discrete Input 6*: Active B
[DSC130m] *Discrete Input 1*: Inactive A
[DSC130n] *Discrete Input 2*: Inactive A
[DSC130o] *Discrete Input 3*: Inactive A
[DSC130p] *Discrete Input 4*: Inactive A
[DSC130q] *Discrete Input 5*: Inactive A
[DSC130r] *Discrete Input 6*: Inactive A
[DSC130s] *Discrete Input 1*: Inactive B
[DSC130t] *Discrete Input 2*: Inactive B
[DSC130u] *Discrete Input 3*: Inactive B
[DSC130v] *Discrete Input 4*: Inactive B
[DSC130w] *Discrete Input 5*: Inactive B
[DSC130x] *Discrete Input 6*: Inactive B

Reference: HRD R00062010, R00062020

5.6.5 [DSC140] Discrete Input Default

Test Method: Remove all loads from the *Discrete Inputs*. Read the status of each *Discrete Input* using the test mode interface.

Acceptance: [DSC140a] *Discrete Input 1*: The input **shall** be Inactive.

[DSC140b] *Discrete Input 2*: The input **shall** be Inactive.

[DSC140c] *Discrete Input 3*: The input **shall** be Inactive.

[DSC140d] *Discrete Input 4*: The input **shall** be Inactive.

[DSC140e] *Discrete Input 5*: The input **shall** be Inactive.

[DSC140f] *Discrete Input 6*: The input **shall** be Inactive.

Reference: HRD R00063030

5.6.6 [DSC150] Discrete Input Safety

Test Method: For each of the *Discrete Inputs*:

- *Discrete Input 1*
- *Discrete Input 2*
- *Discrete Input 3*
- *Discrete Input 4*
- *Discrete Input 5*
- *Discrete Input 6*

Sequentially connect the respective rear connector interface pin in the following configurations, holding at least 10m in each:

- Leave the pin open-circuit
- Short-circuit the pin to *Aviation Power*
- Short-circuit the pin to *Ground*

Acceptance: [DSC150a] Procedure **[DSC130] shall** pass after this procedure is completed.

Reference: HRD R0064010, R0064020, R0064030

5.6.7 [DSC200] Discrete Output Configuration

Test Method: Read the *Discrete Output* configuration using the test mode interface for each of the following discrete output pins. The appliance **shall** list the rear connector pin number, the output function, and the current status of the *Discrete Input*.

Acceptance: [DSC200a] *Discrete Output 1*

[DSC200b] *Discrete Output 2*

[DSC200c] *Discrete Output 3*

[DSC200d] *Discrete Output 4*

Reference: SRD R00253611, R00253612, R00253613

5.6.8 [DSC210] Discrete Output Active

Test Method: Set each of the indicated *Discrete Output* configurations using the test mode interface and measure the voltage across a 10kΩ load resistor connected to *Aviation Power*. Each Discrete Output **shall** output the indicated state for each configuration, as defined by the following list:

- "Active": The voltage is less than 1.0V.
- "Inactive": The voltage is greater than 3.0V below *Aviation Power*.
- "Failed": Otherwise.

Acceptance:

[DSC210a]	*Discrete Output 1*: Active	*Discrete Outputs 2*, *3* and *4*: Inactive
[DSC210b]	*Discrete Output 2*: Active	*Discrete Outputs 1*, *3* and *4*: Inactive
[DSC210c]	*Discrete Output 3*: Active	*Discrete Outputs 1*, *2* and *4*: Inactive
[DSC210c]	*Discrete Output 4*: Active	*Discrete Outputs 1*, *2* and *3*: Inactive

Reference: HRD R00062070

5.6.9 [DSC220] Discrete Output Inactive

Test Method: Set each of the indicated *Discrete Output* configurations using the test mode interface and measure the voltage across a 10kΩ load resistor connected to *Aviation Power*. Each Discrete Output **shall** output the indicated state for each configuration, as defined by the following list:

- "Active": The voltage is less than 1.0V.
- "Inactive": The voltage is greater than 3.0V below *Aviation Power*.
- "Failed": Otherwise.

Acceptance:

[DSC220a]	*Discrete Output 1*: Inactive	*Discrete Outputs 2*, *3* and *4*: Active
[DSC220b]	*Discrete Output 2*: Inactive	*Discrete Outputs 1*, *3* and *4*: Active
[DSC220c]	*Discrete Output 3*: Inactive	*Discrete Outputs 1*, *2* and *4*: Active
[DSC220c]	*Discrete Output 4*: Inactive	*Discrete Outputs 1*, *2* and *3*: Active

Reference: HRD R00062070

5.6.10 [DSC230] Discrete Output Power | Full

Test Method: Attach an active-low power load to each of the appliance *Discrete Outputs*. Set all discrete outputs to inactive using the test mode interface, and configure each load to individually source at least 500mA. Finally enable all the discrete outputs simultaneously using the test mode interface and measure the output voltage between the output pin and *Ground* after at least 2s enabled time.

Acceptance:

[DSC230a]	*Discrete Output 1*: The voltage **shall** be less than 1.0V.
[DSC230b]	*Discrete Output 2*: The voltage **shall** be less than 1.0V.
[DSC230c]	*Discrete Output 3*: The voltage **shall** be less than 1.0V.
[DSC230c]	*Discrete Output 4*: The voltage **shall** be less than 1.0V.

Reference: HRD R00062050, R00062070

5.6.11 [DSC235] Discrete Output Power | Fast

Test Method: Attach an active-low power load to each of the appliance *Discrete Outputs*. Set all discrete outputs to inactive using the test mode interface, and configure each load to individually source at least 500mA. Finally enable all the discrete outputs simultaneously using the test mode interface and measure the output state of the output pin after at least 2s enabled time. An output can be considered active if the voltage at the output pin is less than 3.5V.

Acceptance: [DSC235a] *Discrete Output 1*: The output **shall** be active.

[DSC235b] *Discrete Output 2*: The output **shall** be active.

[DSC235c] *Discrete Output 3*: The output **shall** be active.

[DSC235c] *Discrete Output 4*: The output **shall** be active.

Reference: HRD R00062050

5.6.12 [DSC240] Discrete Output Interrupt

Test Method: Set each indicated *Discrete Output* to the indicated state using the test mode interface. Observe the voltage of the discrete output while generating a 240ms to 250ms long interruption on *Aviation Power*. In the Inactive state, connect the *Discrete Output* to an independent (non-interrupted) +28V supply. In the Active state, connect the *Discrete Output* to an independent +28V supply through a 500mA constant-current source.

Acceptance: [DSC240a] *Discrete Output 1*, Inactive: The voltage at the output **shall not** drop below 27.5V during the power interruption.

[DSC240b] *Discrete Output 1*, Active: The voltage at the output **shall not** rise above 1.0V during the power interruption.

[DSC240c] *Discrete Output 2*, Inactive: The voltage at the output **shall not** drop below 27.5V during the power interruption.

[DSC240d] *Discrete Output 2*, Active: The voltage at the output **shall not** rise above 1.0V during the power interruption.

[DSC240e] *Discrete Output 3*, Inactive: The voltage at the output **shall not** drop below 27.5V during the power interruption.

[DSC240f] *Discrete Output 3*, Active: The voltage at the output **shall not** rise above 1.0V during the power interruption.

[DSC240g] *Discrete Output 4*, Inactive: The voltage at the output **shall not** drop below 27.5V during the power interruption.

[DSC240h] *Discrete Output 4*, Active: The voltage at the output **shall not** rise above 1.0V during the power interruption.

Reference: HRD R00064120

5.6.13 [DSC250] Discrete Output Timing

Test Method: Connect each indicated Discrete Output to Aviation Power through a 50Ω resistor. Start by setting the Discrete Output to the first indicated state, then observe the voltage while setting it to the second indicated state. Measure the time required to move from 10% to 90% of the voltage swing during the transition period.

Acceptance:

[DSC250a] *Discrete Output 1*, Inactive→Active: The time **shall** be less than 10µs.

[DSC250b] *Discrete Output 1*, Active→Inactive: The time **shall** be less than 10µs.

[DSC250c] *Discrete Output 2*, Inactive→Active: The time **shall** be less than 10µs.

[DSC250d] *Discrete Output 2*, Active→Inactive: The time **shall** be less than 10µs.

[DSC250e] *Discrete Output 3*, Inactive→Active: The time **shall** be less than 10µs.

[DSC250f] *Discrete Output 3*, Active→Inactive: The time **shall** be less than 10µs.

[DSC250g] *Discrete Output 4*, Inactive→Active: The time **shall** be less than 10µs.

[DSC250h] *Discrete Output 4*, Active→Inactive: The time **shall** be less than 10µs.

Reference: HRD R00062080, R00062090

5.6.14 [DSC260] Discrete Output Impedance

Test Method: Power the appliance off. Connect an independent +40V supply through a 1MΩ resistor to each indicated discrete output, and measure the voltage between the resistor and the appliance. Continue to observe the voltage while powering the appliance on

Acceptance:

[DSC260a] *Discrete Output 1*: The voltage measured while the appliance is off **shall** be at least 30V.

[DSC260b] *Discrete Output 1*: The voltage measured when the appliance powers on **shall not** drop below 30V.

[DSC260c] *Discrete Output 2*: The voltage measured while the appliance is off **shall** be at least 30V.

[DSC260d] *Discrete Output 2*: The voltage measured when the appliance powers on **shall not** drop below 30V.

[DSC260e] *Discrete Output 3*: The voltage measured while the appliance is off **shall** be at least 30V.

[DSC260f] *Discrete Output 3*: The voltage measured when the appliance powers on **shall not** drop below 30V.

[DSC260g] *Discrete Output 4*: The voltage measured while the appliance is off **shall** be at least 30V.

[DSC260h] *Discrete Output 4*: The voltage measured when the appliance powers on **shall not** drop below 30V.

Reference: HRD R00062060, R00062150, R00063010

5.6.15 [DSC280] Discrete Output Safety

Test Method: For each of the *Discrete Outputs*, set the indicated output state using the test mode interface:

- *Discrete Output 1*, Active
- *Discrete Output 2*, Active
- *Discrete Output 3*, Active
- *Discrete Output 4*, Active
- *Discrete Output 1*, Inactive
- *Discrete Output 2*, Inactive
- *Discrete Output 3*, Inactive
- *Discrete Output 4*, Inactive

Sequentially connect the respective rear connector interface pin in the following configurations, holding at least 10m in each:

- Leave the pin open-circuit
- Short-circuit the pin to *Aviation Power*
- Short-circuit the pin to *Ground*

Note: Ensure the Aviation Power supply current limit is at least 5A.

Acceptance: [DSC280a] Procedure **[DSC210] shall** pass after this procedure is completed.

Reference: HRD R0064040, R0064050, R0064060

5.6.16 [DSC300] Suppressor Pulse | Full

Test Method: Observe the voltage at the *1090 Suppress* output driving a 300Ω load, in parallel with 1850pF. Capture a simultaneous waveform from the *1090 Suppress* output and the *UAT Antenna*, pre-triggered by at least 10μs on a detected *UAT Antenna* power greater than −20dBm and sufficient to capture the entire message period plus a trailing 10μs. Trigger the indicated ADS-B message transmission using the test mode interface.

Acceptance: [DSC300a] ADS-B Basic Message: The rising edge of *1090 Suppress* **shall** first cross the 1.0V threshold no sooner than 5μs before detected power first rises above −20dBm.

[DSC300b] ADS-B Basic Message: The output voltage *1090 Suppress* **shall** be greater than 18.0V for the entire duration of the message.

[DSC300c] ADS-B Basic Message: The falling edge of *1090 Suppress* **shall** last cross the 1.0V threshold no later than 5μs after the detected power first drops below −20dBm.

[DSC300d] ADS-B Long Message: The rising edge of *1090 Suppress* **shall** last cross the 1.0V threshold sooner than 5μs before detected power first rises above −20dBm.

[DSC300e] ADS-B Long Message: The output voltage on *1090 Suppress* **shall** be greater than 18.0V for the entire duration of the message.

[DSC300f] ADS-B Long Message: The falling edge of *1090 Suppress* **shall** first cross the 1.0V threshold no later than 5μs after the detected power first drops below −20dBm.

Reference: HRD R00062100, R00062110, R00062120, R00062130, R00063050

5.6.17 [DSC305] Suppressor Pulse | Fast

Test Method: Manually enable the *1090 Suppress* using the test mode interface and observe the voltage at the output.

Acceptance: [DSC305a] "Active": the voltage **shall** be greater than 6.5V.

[DSC305b] "Inactive": the voltage **shall** be less than 3.5V.

Reference: Derived

5.6.18 [DSC310] Suppressor Pulse Timing

Test Method: Trigger a Long ADS-B message transmission using the test mode interface. Observe the voltage at the *1090 Suppress* output when a 300Ω load is applied in parallel with 1850pF.

Acceptance: [DSC310a] The leading edge of the pulse **shall** rise at 20V/µs or faster.

[DSC310b] The trailing edge of the pulse **shall** fall at 10V/µs or faster.

Reference: HRD R00062160, R00062170

5.6.19 [DSC315] Suppressor Pulse Impedance

Test Method: Disable the *1090 Suppress* output using the test mode interface. Input a 70V peak square wave at 10.0kHz through a 20kΩ resistor, and measure the voltage at the output pin.

Acceptance: [DSC315a] The peak voltage **shall** be greater than 35.0V.

[DSC315b] The rising edge time, from 10% to 90%, **shall** be less than 1.3µs.

[DSC315c] The falling edge time, from 90% to 10%, **shall** be less than 1.3µs.

Reference: HRD R00062180

5.6.20 [DSC320] Suppressor Pulse Default

Test Method: Power the appliance off. Connect a 1kΩ load to the *1090 Suppress* output, and measure the voltage across the load. Power the appliance on, and continue to observe the voltage across the load.

Acceptance: [DSC320a] The voltage **shall** be less than 1.0V when the appliance is off.

[DSC320b] The voltage **shall** remain less than 1.0V until 100ms after the *Global Reset* is de-asserted.

Reference: HRD R00063020

5.6.21 [DSC330] Suppressor Pulse Safety

Test Method: Sequentially configure the *1090 Suppress* output state and rear connector interface pin as indicated, holding at least 10m in each configuration

- "Inactive": Leave the *1090 Suppress* pin open-circuit
- "Active": Leave the *1090 Suppress* pin open-circuit
- "Inactive": Short-circuit the *1090 Suppress* pin to *Aviation Power*
- "Active": Short-circuit the *1090 Suppress* pin to *Aviation Power*
- "Inactive": Short-circuit the *1090 Suppress* pin to *Ground*
- "Active": Short-circuit the *1090 Suppress* pin to *Ground*

Acceptance: [DSC330a] Procedure **[DSC300] shall** pass after this procedure is completed.

Reference: HRD R0064070, R0064080, R0064090

5.7 RS-232

5.7.1 [SER200] 232 Loopback

Test Method: Connect the *Transmit* and *Receive* signals for each of the following bidirectional ports and transmit at least 10 successive non-synchronous packets with varying contents through each port at the highest baud rate supported. Read the loopback status through the test mode interface as:

- "Pending", if the minimum number of test packets has not been transmitted;
- "Passing", if a bitwise identical packet was received in proper order for each transmitted packet
- "Failing", otherwise.

Note: Other rates will be tested during the CLD Validation & Verification process

Acceptance:

[SER200a] The status for *232 Port 1* **shall** be Passing.

[SER200b] The status for *232 Port 2* **shall** be Passing.

[SER200c] The status for *232 Port 3* **shall** be Passing.

[SER200d] The status for *232 Port 4* **shall** be Passing.

[SER200e] The status for *232 Port 5* **shall** be Passing.

Reference: SRD R00253580

5.7.2 [SER205] 232 Transmit Open

Test Method: Observe the voltage at the rear connector *Transmit* pin of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Leave the *Transmit* pin open-circuit for the duration of the test. Transmit hexadecimal character values 0x00, 0xA5, and 0xFF through the indicated port at the highest baud rate supported using the test mode interface.

Acceptance:

[SER205a] *232 Port 1*: The voltage measured **shall** be greater than −25V and less than +25V for the transmission duration.

[SER205b] *232 Port 2*: The voltage measured **shall** be greater than −25V and less than +25V for the transmission duration.

[SER205c] *232 Port 3*: The voltage measured **shall** be greater than −25V and less than +25V for the transmission duration.

[SER205d] *232 Port 4*: The voltage measured **shall** be greater than −25V and less than +25V for the transmission duration.

[SER205e] *232 Port 5*: The voltage measured **shall** be greater than −25V and less than +25V for the transmission duration.

Reference: HRD R00074040, R00074050

5.7.3 [SER210] 232 Transmit Levels

Test Method: Observe the voltage at the rear connector *Transmit* pin of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Place a load between the *Transmit* pin and *Ground* consisting of 3kΩ || 2.5nF. Transmit a single hexadecimal character value 0xA5 through indicated port at the highest baud rate supported using the test mode interface.

Note: Reference the transmitted bit sequence as "1101001010", LSB first.

Acceptance:

[SER210a] *232 Port 1*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during the port idle period before and after the transmission.

[SER210b] *232 Port 1*: The voltage measured **shall** be less than −5.0V and greater than −15.0V during each bit "1" in the bit sequence.

[SER210c] *232 Port 1*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during each bit "0" in the bit sequence.

[SER210d] *232 Port 1*: Each bit transition shall be unconditionally monotonic.

[SER210e] *232 Port 2*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during the port idle period before and after the transmission.

[SER210f] *232 Port 2*: The voltage measured **shall** be less than −5.0V and greater than −15.0V during each bit "1" in the bit sequence.

[SER210g] *232 Port 2*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during each bit "0" in the bit sequence.

[SER210h] *232 Port 2*: Each bit transition **shall** be unconditionally monotonic.

[SER210i] *232 Port 3*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during the port idle period before and after the transmission.

[SER210j] *232 Port 3*: The voltage measured **shall** be less than −5.0V and greater than −15.0V during each bit "1" in the bit sequence.

[SER210k] *232 Port 3*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during each bit "0" in the bit sequence.

[SER210l] *232 Port 3*: Each bit transition **shall** be unconditionally monotonic.

[SER210m] *232 Port 4*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during the port idle period before and after the transmission.

[SER210n] *232 Port 4*: The voltage measured **shall** be less than −5.0V and greater than −15.0V during each bit "1" in the bit sequence.

[SER210o] *232 Port 4*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during each bit "0" in the bit sequence.

[SER210p] *232 Port 4*: Each bit transition **shall** be unconditionally monotonic.

[SER210q] *232 Port 5*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during the port idle period before and after the transmission.

[SER210r] *232 Port 5*: The voltage measured **shall** be less than −5.0V and greater than −15.0V during each bit "1" in the bit sequence.

[SER210s] *232 Port 5*: The voltage measured **shall** be greater than +5.0V and less than +15.0V during each bit "0" in the bit sequence.

[SER210t] *232 Port 5*: Each bit transition **shall** be unconditionally monotonic.

Reference: HRD R00071050, R00071060, R00071070, R00071080, R00071090, R00072010, R00072020, R00072030

5.7.4 [SER215] 232 Transmit Timing

Test Method: Observe the voltage at the rear connector *Transmit* pin of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Place a load between the *Transmit* pin and *Ground* consisting of 3kΩ || 2.5nF. Transmit a single hexadecimal character value 0xA5 through indicated port at the highest baud rate supported using the test mode interface.

Note: Other rates will be tested during the CLD Validation & Verification process

Acceptance: [SER215a] *232 Port 1*: The time required to accomplish every state transition of *Transmit*, from "0" to "1" or "1" to "0", **shall** be less than 250ns.

[SER215b] *232 Port 1*: The maximum rate of voltage change for any state transition of *Transmit* **shall** be less than 120V/μs.

[SER215c] *232 Port 2*: The time required to accomplish every state transition of *Transmit*, from "0" to "1" or "1" to "0", **shall** be less than 250ns.

[SER215d] *232 Port 2*: The maximum rate of voltage change for any state transition of *Transmit* **shall** be less than 120V/μs.

[SER215e] *232 Port 3*: The time required to accomplish every state transition of *Transmit*, from "0" to "1" or "1" to "0", **shall** be less than 250ns.

[SER215f] *232 Port 3*: The maximum rate of voltage change for any state transition of *Transmit* **shall** be less than 120V/μs.

[SER215g] *232 Port 4*: The time required to accomplish every state transition of *Transmit*, from "0" to "1" or "1" to "0", **shall** be less than 250ns.

[SER215h] *232 Port 4*: The maximum rate of voltage change for any state transition of *Transmit* **shall** be less than 120V/μs.

[SER215i] *232 Port 5*: The time required to accomplish every state transition of *Transmit*, from "0" to "1" or "1" to "0", **shall** be less than 250ns.

[SER215j] *232 Port 5*: The maximum rate of voltage change for any state transition of *Transmit* **shall** be less than 120V/μs.

Reference: HRD R00072040, R00072050, R00072060

5.7.5 [SER220] 232 Receive Open Circuit

Test Method: Measure the voltage between the indicated rear connector *Receive* pin and *Ground*, with the *Receive* pin open-circuit.

Acceptance: [SER220a] *232 Port 1*: The measured voltage **shall** be 0.0 ± 0.5V

[SER220b] *232 Port 2*: The measured voltage **shall** be 0.0 ± 0.5V

[SER220c] *232 Port 3*: The measured voltage **shall** be 0.0 ± 0.5V

[SER220d] *232 Port 4*: The measured voltage **shall** be 0.0 ± 0.5V

[SER220e] *232 Port 5*: The measured voltage **shall** be 0.0 ± 0.5V

Reference: HRD R00072100

5.7.6 [SER225] 232 Receive Termination

Test Method: Connect the indicated low-impedance voltage source to the rear connector *Receive* pin of the indicated *232 Port*. Insert a 100Ω current-sense resistor inline between the voltage source and the appliance rear connector. Measure the voltage across the current-sense resistor in each configuration.

Acceptance:

[SER225a] *232 Port 1*, +15V: The voltage **shall** be 300 ± 50mV

[SER225b] *232 Port 1*, +5V: The voltage **shall** be 100 ± 16mV

[SER225c] *232 Port 1*, −15V: The voltage **shall** be −300 ± 50mV

[SER225d] *232 Port 1*, −5V: The voltage **shall** be −100 ± 16mV

[SER225e] *232 Port 2*, +15V: The voltage **shall** be 300 ± 50mV

[SER225f] *232 Port 2*, +5V: The voltage **shall** be 100 ± 16mV

[SER225g] *232 Port 2*, −15V: The voltage **shall** be −300 ± 50mV

[SER225h] *232 Port 2*, −5V: The voltage **shall** be −100 ± 16mV

[SER225i] *232 Port 3*, +15V: The voltage **shall** be 300 ± 50mV

[SER225j] *232 Port 3*, +5V: The voltage **shall** be 100 ± 16mV

[SER225k] *232 Port 3*, −15V: The voltage **shall** be −300 ± 50mV

[SER225l] *232 Port 3*, −5V: The voltage **shall** be −100 ± 16mV

[SER225m] *232 Port 4*, +15V: The voltage **shall** be 300 ± 50mV

[SER225n] *232 Port 4*, +5V: The voltage **shall** be 100 ± 16mV

[SER225o] *232 Port 4*, −15V: The voltage **shall** be −300 ± 50mV

[SER225p] *232 Port 4*, −5V: The voltage **shall** be −100 ± 16mV

[SER225q] *232 Port 5*, +15V: The voltage **shall** be 300 ± 50mV

[SER225r] *232 Port 5*, +5V: The voltage **shall** be 100 ± 16mV

[SER225s] *232 Port 5*, −15V: The voltage **shall** be −300 ± 50mV

[SER225t] *232 Port 5*, −5V: The voltage **shall** be −100 ± 16mV

Reference: HRD R00072090

5.7.7 [SER230] 232 Transmit Current

Test Method: Connect a 1Ω current sense resistor between the rear connector *Transmit* pin of the indicated port and *Ground*. Observe the voltage at the rear connector *Transmit* pin of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Transmit the hexadecimal character values 0x00, 0xA5, and 0xFF at the slowest baud rate supported using the test mode interface.

Acceptance:

[SER230a] *232 Port 1*: The voltage **shall** be between −95mV and 95mV.

[SER230b] *232 Port 2*: The voltage **shall** be between −95 mV and 95mV.

[SER230c] *232 Port 3*: The voltage **shall** be between −95 mV and 95mV.

[SER230d] *232 Port 4*: The voltage **shall** be between −95 mV and 95mV.

[SER230e] *232 Port 5*: The voltage **shall** be between −95 mV and 95mV.

Reference: HRD R00074030

5.7.8 [SER235] 232 Receive Threshold

Test Method: Clear the receive data queue and configure the indicated *232 Port* to the highest baud rate supported using the test mode interface. Sequentially apply a signal of the following characteristics to the rear connector *Receive* pin of the indicated port.

- The signal shall represent the symbol sequence “1000000000”, then “1101001010”, then “1111111110”, transmitted LSB first.
- The space between each symbol, and before the first symbol and after the last symbol, shall be represented by a string of at least 2 “0”s.
- Each “1” shall be signaled by driving *Receive* at $-V_{TX} \pm 0.2V$.
- Each “0” shall be signaled by driving *Receive* at $+V_{TX} \pm 0.2V$.
- Each bit time shall be within 1% of the nominal rate configured previously.
- Each transition shall be monotonic, from 10% to 90% in less than 250ns.

After applying the signal, read the received characters in hexadecimal form using the test mode interface. The characters read from the buffer **shall** be 0x00, 0xA5, 0xFF, then Empty.

Acceptance:
[SER235a] *232 Port 1*, V_{TX} = 2.0V.
[SER235b] *232 Port 2*, V_{TX} = 2.0V.
[SER235c] *232 Port 3*, V_{TX} = 2.0V.
[SER235d] *232 Port 4*, V_{TX} = 2.0V.
[SER235e] *232 Port 5*, V_{TX} = 2.0V.
[SER235f] *232 Port 1*, V_{TX} = 16.0V.
[SER235g] *232 Port 2*, V_{TX} = 16.0V.
[SER235h] *232 Port 3*, V_{TX} = 16.0V.
[SER235i] *232 Port 4*, V_{TX} = 16.0V.
[SER235j] *232 Port 5*, V_{TX} = 16.0V.

Reference: HRD R00071100, R00071110, R00071120, R00072070, R00072080

5.7.9 [SER245] 232 Transmit Idle

Test Method: Measure the voltage between the indicated rear connector *Transmit* pin and *Ground*, with the *Transmit* pin open-circuit.

Acceptance:
[SER245a] *232 Port 1*: The voltage **shall** be between −12V and −14.0V.
[SER245b] *232 Port 2*: The voltage **shall** be between −12V and −14.0V.
[SER245c] *232 Port 3*: The voltage **shall** be between −12V and −14.0V.
[SER245d] *232 Port 4*: The voltage **shall** be between −12V and −14.0V.
[SER245e] *232 Port 5*: The voltage **shall** be between −12V and −14.0V.

Reference: HRD R00073010

5.7.10 [SER250] 232 Receive Capacitance

Test Method: Connect a 1kΩ resistor in series with the *Receive* pin of the indicated port. Drive the resistor with a 50% duty cycle 50Hz square wave between the indicated voltages V_{LO} and V_{HI}. For both rising and falling edges of the input wave measure the time τ required to transition between the previous steady-state voltage and 63% of the following steady-state voltage.

Acceptance:

[SER250a] *232 Port 1*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 2ms.

[SER250b] *232 Port 2*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 2ms.

[SER250c] *232 Port 3*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 2ms.

[SER250d] *232 Port 4*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 2ms.

[SER250e] *232 Port 5*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 2ms.

[SER250f] *232 Port 1*, V_{LO} = +14.0V, V_{HI} = +16.0V: τ **shall** be less than 2ms.

[SER250g] *232 Port 2*, V_{LO} = +14.0V, V_{HI} = +16.0V: τ **shall** be less than 2ms.

[SER250h] *232 Port 3*, V_{LO} = +14.0V, V_{HI} = +16.0V: τ **shall** be less than 2ms.

[SER250i] *232 Port 4*, V_{LO} = +14.0V, V_{HI} = +16.0V: τ **shall** be less than 2ms.

[SER250j] *232 Port 5*, V_{LO} = +14.0V, V_{HI} = +16.0V: τ **shall** be less than 2ms.

[SER250k] *232 Port 1*, V_{LO} = −14.0V, V_{HI} = −16.0V: τ **shall** be less than 2ms.

[SER250l] *232 Port 2*, V_{LO} = −14.0V, V_{HI} = −16.0V: τ **shall** be less than 2ms.

[SER250m] *232 Port 3*, V_{LO} = −14.0V, V_{HI} = −16.0V: τ **shall** be less than 2ms.

[SER250n] *232 Port 4*, V_{LO} = −14.0V, V_{HI} = −16.0V: τ **shall** be less than 2ms.

[SER250o] *232 Port 5*, V_{LO} = −14.0V, V_{HI} = −16.0V: τ **shall** be less than 2ms.

Reference: HRD R00072095

5.7.11 [SER255] 232 Port Safety

Test Method: Run the following test procedure against each of the ports:

- *232 Port 1*
- *232 Port 2*
- *232 Port 3*
- *232 Port 4*
- *232 Port 5*

Connect the appliance rear connector interface pins in each of the following configurations. Hold each configuration place for at least 10min while continuously transmitting alternating hexadecimal values 0x00 and 0xFF on the test port at the slowest baud rate supported using the test mode interface.

- Leave both *Receive* and *Transmit* open-circuit
- Short-circuit *Transmit* to *Ground*, leave *Receive* open-circuit
- Short-circuit *Receive* to *Ground*, leave *Transmit* open-circuit
- Connect *Receive* to a low impedance +25V source, leave *Transmit* open-circuit
- Connect *Receive* to a low impedance −25V source, leave *Transmit* open-circuit
- Short-circuit both *Receive* and *Transmit* to *Ground*

Acceptance: [SER255a] Procedure **[SER200] shall** pass after this procedure is completed

Reference: HRD R00074010, R00074020, R00074060, R00074070, R00074080, R00074090

5.8 RS-422

5.8.1 [SER300] 422 Loopback

Test Method: Connect the *Transmit* and *Receive* signals for each of the following *422 Ports* and transmit at least 10 successive non-synchronous packets with varying contents through each port at the highest baud rate supported. Read the loopback status through the test mode interface as:

- "Pending", if the minimum number of test packets has not been transmitted;
- "Passing", if a bitwise identical packet was received in proper order for each transmitted packet
- "Failing", otherwise.

Note: Other rates will be tested during the CLD Validation & Verification process

Acceptance: [SER300a] The status for *422 Port 1* **shall** be Passing.

[SER300b] The status for *422 Port 2* **shall** be Passing.

Reference: SRD R00253584

5.8.2 [SER305] 422 Transmit Open

Test Method: Observe the voltage at the rear connector *Transmit A* and *Transmit B* pins of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Leave the *Transmit A* and *Transmit B* pins open-circuit for the duration of the test. Transmit the hexadecimal character values 0x00 and 0xFF through indicated port at the slowest baud rate supported using the test mode interface.

Acceptance: [SER305a] *422 Port 1*: The voltage measured on *Transmit A* **shall** be between −6V and +6V for the transmission duration.

[SER350b] *422 Port 1*: The voltage measured on *Transmit B* **shall** be between −6V and +6V for the transmission duration.

[SER305c] *422 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be between −10V and +10V for the transmission duration.

[SER305d] *422 Port 2*: The voltage measured on *Transmit A* **shall** be between −6V and +6V for the transmission duration.

[SER305e] *422 Port 2*: The voltage measured on *Transmit B* **shall** be between −6V and +6V for the transmission duration.

[SER305f] *422 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be between −10V and +10V for the transmission duration.

Reference: HRD R00084010, R00084020, R00084030

5.8.3 [SER310] 422 Transmit Levels

Test Method: Observe the voltage at the rear connector *Transmit A* and *Transmit B* pins of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Place a load between the *Transmit A* and *Transmit B* pins of 100 ± 1Ω. Transmit a single hexadecimal character value 0xA5 through indicated port at the highest baud rate supported using the test mode interface.

Note: Reference the transmitted bit sequence as "0101001011", LSB first.

Acceptance:

[SER310a] *422 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be greater than +2.0V before and after the transmission.

[SER310b] *422 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be greater than +2.0V during each "1" in the bit sequence.

[SER310c] *422 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be smaller than −2.0V during each "0" in the bit sequence.

[SER310d] *422 Port 1*: The difference between the magnitudes of the computed differential voltage for each "1" and the computed differential voltage for each "0" **shall** be between −0.4V and +0.4V.

[SER310e] *422 Port 1*: The computed common mode voltage of *Transmit A* and *Transmit B* **shall** be between −3.0V and +3.0V during each "1" in the bit sequence.

[SER310f] *422 Port 1*: The computed common mode voltage of *Transmit A* and *Transmit B* **shall** be between −3.0V and +3.0V during each "0" in the bit sequence.

[SER310g] *422 Port 1*: The difference between the magnitudes of the computed common mode voltage for each "1" and the computed common mode voltage for each "0" **shall** be between −0.4V and +0.4V.

[SER310h] *422 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be greater than +2.0V before and after the transmission.

[SER310i] *422 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be greater than +2.0V during each "1" in the bit sequence.

[SER310j] *422 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be smaller than −2.0V during each "0" in the bit sequence.

[SER310k] *422 Port 2*: The difference between the magnitudes of the computed differential voltage for each "1" and the computed differential voltage for each "0" **shall** be between −0.4V and +0.4V.

[SER310l] *422 Port 2*: The computed common mode voltage of *Transmit A* and *Transmit B* **shall** be between −3.0V and +3.0V during each "1" in the bit sequence.

[SER310m] *422 Port 2*: The computed common mode voltage of *Transmit A* and *Transmit B* **shall** be between −3.0V and +3.0V during each "0" in the bit sequence.

[SER310n] *422 Port 2*: The difference between the magnitudes of the computed common mode voltage for each "1" and the computed common mode voltage for each "0" **shall** be between −0.4V and +0.4V.

Reference: HRD R00081050, R00081060, R00081070, R00081080, R00081090, R00082020, R00082030, R00082040, R00082050, R00082060, R00082070

5.8.4 [SER315] 422 Transmit Timing

Test Method: Observe the voltage at the rear connector *Transmit A* and *Transmit B* pins of the indicated port after the first edge of the start bit crosses of *Ground*, through the last edge of the stop bit at the end of the transmission sequence. Place a load between the *Transmit A* and *Transmit B* pins of 100 ± 1Ω. Transmit a single hexadecimal character value 0xA5 through indicated port at the highest baud rate supported using the test mode interface.

Note: Other rates will be tested during the CLD Validation & Verification process

Acceptance: [SER315a] *422 Port 1*: The time required to accomplish every state transition measured from *Transmit A* to *Transmit B*, during "0" to "1" or "1" to "0", **shall** be less than 10% of the bit time of the selected nominal data rate, measured from the 10% to 90% thresholds of the differential steady state voltage.

[SER315b] *422 Port 1*: During the time required to accomplish every state transition, from the 10% to 90% thresholds of the differential steady state voltage, the differential voltage change **shall** be monotonically increasing or decreasing.

[SER315c] *422 Port 1*: After a state transition, crosses the 90% threshold of the differential steady state voltage, the voltage change **shall** not vary more than 10% from the full differential steady state voltage.

[SER315d] *422 Port 2*: The time required to accomplish every state transition measured from *Transmit A* to *Transmit B*, during "0" to "1" or "1" to "0", **shall** be less than 10% of the bit time of the selected nominal data rate, measured from the 10% to 90% thresholds of the differential steady state voltage.

[SER315e] *422 Port 2*: During the time required to accomplish every bit transition, from the 10% to 90% thresholds of the differential steady state voltage, the differential voltage change **shall** be monotonically increasing or decreasing.

[SER315f] *422 Port 2*: After a bit transition crosses the 90% threshold of the final steady state, the differential voltage **shall** not vary more than 10% until the beginning of the next bit transition.

Reference: HRD R00082120, R00082130, R00082140

5.8.5 [SER320] 422 Transmit Impedance

Test Method: For each port indicated, connect a R_L = 100Ω ± 1% load between the rear connector *Transmit A* and *Transmit B* pins. Disable any character transmission using the test mode interface and measure the DC voltage that develops across the resistor as V_L. Replace the load with R_H 1kΩ ± 1% resistor and measure the DC voltage as V_H. Compute the transmit impedance R_O of the port as:

$$R_O = \frac{R_L R_H (V_H - V_L)}{V_L R_H - V_H R_L}$$

Acceptance: [SER320a] *422 Port 1*: The impedance **shall** be less than 100Ω.

[SER320b] *422 Port 2*: The impedance **shall** be less than 100Ω.

Reference: HRD R00082010

5.8.6 [SER325] 422 Receive Threshold

Test Method: Clear the receive data queue and configure the indicated port to the highest baud rate supported using the test mode interface. If indicated, insert a series resistance (R_S) between each signal driver and the corresponding rear connector input pin. For each of the indicated ports, apply a signal to the rear connector input that meets the following criteria based on the indicated common mode voltage (V_{CM}) and peak differential voltage (V_{PP}) parameters.

- The signal shall represent the symbol sequence “0000000001”, then “0101001011”, then “0111111111”, transmitted LSB first.
- The space between each symbol, and before the first symbol and after the last symbol, shall be represented by a string of at least 2 “1”s.
- Each “1” shall be signaled by driving *Receive A* at (V_{CM} + V_{PP} / 2) ± 0.05V, and simultaneously driving *Receive B* at (V_{CM} − V_{PP} / 2) ± 0.05V.
- Each “0” shall be signaled by driving Receive A at (V_{CM} − V_{PP} / 2) ± 0.05V, and simultaneously driving *Receive B* at (V_{CM} + V_{PP} / 2) ± 0.05V.
- Each bit time shall be within 1% of the nominal rate configured previously.
- Each bit transition, measured differentially from *Receive A* to *Receive B*, shall be monotonic from 10% to 90% in less than 250ns.

After applying the signal, read the received characters in hexadecimal form using the test mode interface. The characters read from the buffer **shall** be 0x00, 0xA5, 0xFF, then Empty.

Acceptance:

[SER325a] *422 Port 1*, V_{CM} = 0.0V, V_{PP} = 0.3V.

[SER325b] *422 Port 1*, V_{CM} = 0.0V, V_{PP} = 12.0V.

[SER325c] *422 Port 1*, V_{CM} = +7.0V, V_{PP} = 0.3V.

[SER325d] *422 Port 1*, V_{CM} = −7.0V, V_{PP} = 0.3V.

[SER325e] *422 Port 1*, V_{CM} = +7.0V, V_{PP} = 0.5V, R_S = 500Ω ± 1.

[SER325f] *422 Port 1*, V_{CM} = −7.0V, V_{PP} = 0.5V, R_S = 500Ω ± 1.

[SER325g] *422 Port 2*, V_{CM} = 0.0V, V_{PP} = 0.3V.

[SER325h] *422 Port 2*, V_{CM} = 0.0V, V_{PP} = 12.0V.

[SER325i] *422 Port 2*, V_{CM} = +7.0V, V_{PP} = 0.3V.

[SER325j] *422 Port 2*, V_{CM} = −7.0V, V_{PP} = 0.3V.

[SER325k] *422 Port 2*, V_{CM} = +7.0V, V_{PP} = 0.5V, R_S = 500Ω ± 1.

[SER325l] *422 Port 2*, V_{CM} = −7.0V, V_{PP} = 0.5V, R_S = 500Ω ± 1.

Reference: HRD R00081100, R00081110, R00081120, R00082190, R00082200, R00082210, R00082220, R00082230, R00082240, R00082250, R00082260, R00084110, R00084120

5.8.7 [SER330] 422 Receive Termination

Test Method: Put the appliance in the indicated power state; for appliance power off, wait at least 1min for the internal circuits to discharge. Measure the resistance between the indicated terminal and **Ground**.

Acceptance:
[SER330a] Power On, *422 Port 1 Transmit A*: Resistance **shall** be at least 4kΩ
[SER330b] Power On, *422 Port 1 Transmit B*: Resistance **shall** be at least 4kΩ
[SER330c] Power On, *422 Port 2 Transmit A*: Resistance **shall** be at least 4kΩ
[SER330d] Power On, *422 Port 2 Transmit B*: Resistance **shall** be at least 4kΩ
[SER330e] Power Off, *422 Port 1 Transmit A*: Resistance **shall** be at least 4kΩ
[SER330f] Power Off, *422 Port 1 Transmit B*: Resistance **shall** be at least 4kΩ
[SER330g] Power Off, *422 Port 2 Transmit A*: Resistance **shall** be at least 4kΩ
[SER330h] Power Off, *422 Port 2 Transmit B*: Resistance **shall** be at least 4kΩ

Reference: HRD R00082150, R00082160, R00082170, R00082180

5.8.8 [SER335] 422 Transmit Power Off

Test Method: Power the appliance off, wait at least 1min for the internal circuitry to discharge. Apply the indicated voltages from low-impedance voltage sources to the indicated terminals, each through a 250Ω current-sense resistor. Measure the voltage that develops across each current-sense resistor.

Acceptance:
[SER335a] *422 Port 1*, *Transmit A* = +0.25V, *Transmit B* = −0.25V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335b] *422 Port 1*, *Transmit A* = +6.00V, *Transmit B* = −6.00V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335c] *422 Port 1*, *Transmit A* = −0.25V, *Transmit B* = +0.25V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335d] *422 Port 1*, *Transmit A* = −6.00V, *Transmit B* = +6.00V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335e] *422 Port 2*, *Transmit A* = +0.25V, *Transmit B* = −0.25V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335f] *422 Port 2*, *Transmit A* = +6.00V, *Transmit B* = −6.00V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335g] *422 Port 2*, *Transmit A* = −0.25V, *Transmit B* = +0.25V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

[SER335h] *422 Port 2*, *Transmit A* = −6.00V, *Transmit B* = +6.00V:
Voltage across the *Transmit A* resistor **shall** be between −25mV and +25mV, and voltage across the *Transmit B* resistor **shall** be between −25mV and +25mV.

Reference: HRD R00082080, R00082090, R00082100, R00082110

5.8.9 [SER340] 422 Receive Open Circuit

Test Method: Measure the voltage between the indicated rear connector pin and *Ground*, with the indicated *422 Port* open-circuit.

Acceptance: [SER340a] *422 Port 1*, *Receive A*: The measured voltage **shall** be 2.75 ± 0.20V

[SER340b] *422 Port 1*, *Receive B*: The measured voltage **shall** be 2.25 ± 0.20V

[SER340c] *422 Port 2*, *Receive A*: The measured voltage **shall** be 2.75 ± 0.20V

[SER340d] *422 Port 2*, *Receive B*: The measured voltage **shall** be 2.25 ± 0.20V

Reference: HRD R00082270, R00082280

5.8.10 [SER345] 422 Transmit Idle

Test Method: Measure the voltage between the indicated rear connector pin and *Ground*, with the indicated *422 Port* open-circuit and inactive.

Acceptance: [SER345a] *422 Port 1*, *Transmit A*: The measured voltage **shall** be 2.75 ± 0.20V

[SER345b] *422 Port 1*, *Transmit B*: The measured voltage **shall** be 2.25 ± 0.20V

[SER345c] *422 Port 2*, *Transmit A*: The measured voltage **shall** be 2.75 ± 0.20V

[SER345d] *422 Port 2*, *Transmit B*: The measured voltage **shall** be 2.25 ± 0.20V

Reference: HRD R00083010

5.8.11 [SER350] 422 Transmit Current

Test Method: Connect a 1Ω current sense resistor between the rear connector *Transmit A* pin of the indicated port and *Ground*, and a second 1Ω current sense resistor between *Transmit B* of the indicated port and *Ground*. Connect an oscilloscope to both the *Transmit A* and *Transmit B* pins at the rear connector and configure it to trigger on a falling edge crossing of the differential common mode, capturing the entire transmission sequence plus at least 10μs of the leading and trailing steady state. Transmit the hexadecimal character values 0x00 and 0xFF at the slowest baud rate supported using the test mode interface.

Acceptance: [SER350a] *422 Port 1*: The voltage measured between *Transmit A* and *Ground* **shall** be −135mV to 135mV.

[SER350b] *422 Port 1*: The voltage measured between *Transmit B* and *Ground* **shall** be −135mV to 135mV.

[SER350c] *422 Port 2*: The voltage measured between *Transmit A* and *Ground* **shall** be −135mV to 135mV.

[SER350d] *422 Port 2*: The voltage measured between *Transmit B* and *Ground* **shall** be −135mV to 135mV.

Reference: HRD R00084090, R00084100

5.8.12 [SER360] 422 Port Safety

Test Method: Run the following test procedure against each of the ports:

- *422 Port 1*
- *422 Port 2*

Connect the appliance rear connector interface pins in each of the following configurations. Hold each configuration place for at least 10m while continuously transmitting alternating hexadecimal values 0x00 and 0xFF on the test port at the slowest baud rate supported using the test mode interface.

- Leave both *Transmit A* and *Transmit B* open-circuit
- Short-circuit *Transmit A* to *Transmit B* , but not to *Ground*
- Short-circuit *Transmit A* to *Ground*, leave *Transmit B* open-circuit
- Short-circuit *Transmit B* to *Ground*, leave *Transmit A* open-circuit
- Short-circuit both *Transmit A* and *Transmit B* to *Ground*
- Leave both *Receive A* and *Receive B* open-circuit
- Short-circuit *Receive A* to *Receive B*, but not to *Ground*
- Short-circuit *Receive A* to *Ground*, leave *Receive B* open-circuit
- Short-circuit *Receive B* to *Ground*, leave *Receive A* open-circuit
- Short-circuit both *Receive A* and *Receive B* to *Ground*

Acceptance: [SER360a] Procedure **[SER300] shall** pass after this procedure is completed

Reference: HRD R00084040, R00084050, R00084060, R00084070, R00084080, R00084130, R00084140, R00084150, R00084160, R00084170

5.9 ARINC 429

5.9.1 [SER100] 429 Loopback

Test Method: Connect each of the following ports as indicated and transmit at least 10 labels with varying contents through each port at the indicated speed. Read the loopback status using the test mode interface as:

- "Pending", if the minimum number of test packets has not been transmitted;
- "Passing", if a bitwise identical packet was received in proper order for each transmitted packet
- "Failing", otherwise.

Acceptance: [SER100a] Low Speed: When *429 Transmit Port 1* is connected to *429 Receive Port 1*, the status of *429 Receive Port 1* **shall** be Passing.

[SER100b] Low Speed: When *429 Transmit Port 2* is connected to *429 Receive Port 2*, the status of *429 Receive Port 2* **shall** be Passing.

[SER100c] Low Speed: When *429 Transmit Port 2* is connected to *429 Receive Port 3*, the status of *429 Receive Port 3* **shall** be Passing.

[SER100d] High Speed: When *429 Transmit Port 1* is connected to *429 Receive Port 1*, the status of *429 Receive Port 1* **shall** be Passing.

[SER100e] High Speed: When *429 Transmit Port 2* is connected to *429 Receive Port 2*, the status of *429 Receive Port 2* **shall** be Passing.

[SER100f] High Speed: When *429 Transmit Port 2* is connected to *429 Receive Port 3*, the status of *429 Receive Port 3* **shall** be Passing.

Reference: Derived

5.9.2 [SER110] 429 Transmit Levels

Test Method: Observe the voltage at the rear connector *Transmit A* and *Transmit B* pins of the indicated port after the first edge of the first bit crosses of *Ground*, through the last edge of the last bit at the end of the transmission sequence. Place a load between the *Transmit A* and *Transmit B* pins of 1kΩ ± 1%. Transmit the 32-bit label 0xF83C38CA out the indicated port at high speed using the test mode interface.

Acceptance:

[SER110a] *429 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be +9.0V to +11.0V whenever a logic "high" is driven.

[SER110b] *429 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be −9.0V to −11.0V whenever a logic "low" is driven.

[SER110c] *429 Port 1*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be −0.5V to +0.5V whenever a logic "null" is driven.

[SER110d] *429 Port 1*: The computed differential voltage between *Transmit A* and *Ground* **shall** be +4.5V to +5.5V whenever a logic "high" is driven.

[SER110e] *429 Port 1*: The computed differential voltage between *Transmit A* and *Ground* **shall** be −4.5V to −5.5V whenever a logic "low" is driven.

[SER110f] *429 Port 1*: The computed differential voltage between *Transmit A* and *Ground* **shall** be −0.25V to +0.25V whenever a logic "null" is driven.

[SER110g] *429 Port 1*: The computed differential voltage between *Transmit B* and *Ground* **shall** be −4.5V to −5.5V whenever a logic "high" is driven.

[SER110h] *429 Port 1*: The computed differential voltage between *Transmit B* and *Ground* **shall** be +4.5V to +5.5V whenever a logic "low" is driven.

[SER110i] *429 Port 1*: The computed differential voltage between *Transmit B* and *Ground* **shall** be −0.25V to +0.25V whenever a logic "null" is driven.

[SER110j] *429 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be +9.0V to +11.0V whenever a logic "high" is driven.

[SER110k] *429 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be −9.0V to −11.0V whenever a logic "low" is driven.

[SER110l] *429 Port 2*: The computed differential voltage between *Transmit A* and *Transmit B* **shall** be −0.5V to +0.5V whenever a logic "null" is driven.

[SER110m] *429 Port 2*: The computed differential voltage between *Transmit A* and *Ground* **shall** be +4.5V to +5.5V whenever a logic "high" is driven.

[SER110n] *429 Port 2*: The computed differential voltage between *Transmit A* and *Ground* **shall** be −4.5V to −5.5V whenever a logic "low" is driven.

[SER110o] *429 Port 2*: The computed differential voltage between *Transmit A* and *Ground* **shall** be −0.25V to +0.25V whenever a logic "null" is driven.

[SER110p] *429 Port 2*: The computed differential voltage between *Transmit B* and *Ground* **shall** be −4.5V to −5.5V whenever a logic "high" is driven.

[SER110q] *429 Port 2*: The computed differential voltage between *Transmit B* and *Ground* **shall** be +4.5V to +5.5V whenever a logic "low" is driven.

[SER110r] *429 Port 2*: The computed differential voltage between *Transmit B* and *Ground* **shall** be −0.25V to +0.25V whenever a logic "null" is driven.

Reference: HRD R00092130, R00092140, R00092150, R00092160, R00092170, R00092180, R00092190, R00092200, R00092210

5.9.3 [SER115] 429 Transmit Logic

Test Method: Transmit the 32-bit label 0xF83C38CA out the indicated *429 Transmit* port at high speed using the test mode interface. Assume the data is transmitted LSB first.

Acceptance: [SER115a] *429 Port 1*: Every "1" in the transmitted label shall correspond to a bit period with a logic high followed by a logic null.

[SER115b] *429 Port 1*: Every "0" in the transmitted label shall correspond to a bit period with a logic low followed by a logic null.

[SER115c] *429 Port 1*: Every "1" in the transmitted label shall correspond to a bit period with a logic high followed by a logic null.

[SER115d] *429 Port 1*: Every "0" in the transmitted label shall correspond to a bit period with a logic low followed by a logic null.

Reference: HRD R00091070, R00091080, R00091090

5.9.4 [SER125] 429 Transmit High Speed

Test Method: Observe the voltage at the rear connector *Transmit A* and *Transmit B* pins of the indicated port after the first edge of the first bit crosses of *Ground*, through the last edge of the last bit at the end of the transmission sequence. Leave an open-circuit load between the *Transmit A* and *Transmit B* rear connector pins. Transmit the 32-bit label 0xF83C38CA out the indicated port at high speed using the test mode interface.

Acceptance: [SER125a] *429 Port 1*: The time between the start of bit 0 and the start of bit 31 in the transmission **shall** be 310 ± 3.1μs.

[SER125b] *429 Port 1*: The time of each bit period, measured from the start of the bit to the start of the next bit, **shall** be 10μs ± 250ns.

[SER125c] *429 Port 1*: The time of each active period, measured from the start of the bit to the start of the transition to "null", **shall** be 5μs ± 250ns.

[SER125d] *429 Port 1*: The rise time of transition from logic "null" to logic "high or from logic "low" to logic "null" **shall** be 1.5 ± 0.5μs, measured from 10% to 90% of the differential steady state outputs.

[SER125e] *429 Port 1*: The fall time of transition from logic "high" to logic "null" or from logic "null" to logic "low" **shall** be 1.5 ± 0.5μs, measured from 10% to 90% of the differential steady state outputs.

[SER125f] *429 Port 2*: The time between the start of bit 0 and the start of bit 31 in the transmission **shall** be 310 ± 3.1μs.

[SER125g] *429 Port 2*: The time of each bit period, measured from the start of the bit to the start of the next bit, **shall** be 10μs ± 250ns.

[SER125h] *429 Port 2*: The time of each active period, measured from the start of the bit to the start of the transition to "null", **shall** be 5μs ± 250ns.

[SER125i] *429 Port 2*: The rise time of transition from logic "null" to logic "high or from logic "low" to logic "null" **shall** be 1.5 ± 0.5μs, measured from 10% to 90% of the differential steady state outputs.

[SER125j] *429 Port 2*: The fall time of transition from logic "high" to logic "null" or from logic "null" to logic "low" **shall** be 1.5 ± 0.5μs, measured from 10% to 90% of the differential steady state outputs.

Reference: HRD R00091050, R00092220, R00092240, R00092260, R00092280, R00092290

5.9.5 [SER130] 429 Transmit Low Speed

Test Method: Observe the voltage at the rear connector *Transmit A* and *Transmit B* pins of the indicated port after the first edge of the first bit crosses of *Ground*, through the last edge of the last bit at the end of the transmission sequence. Leave an open-circuit load between the *Transmit A* and *Transmit B* rear connector pins. Transmit the 32-bit label 0xF83C38CA out the indicated port at low speed using the test mode interface.

Acceptance: [SER130a] *429 Port 1*: The time T_W between the start of bit 0 and the start of bit 31 in the transmission **shall** be 2.14ms to 2.58ms. Compute the bit reference time $T_Z = (T_W / 31)$.

[SER130b] *429 Port 1*: The time T_B of each bit period, measured from the start of the bit to the start of the next bit, **shall** be $T_Z \pm 2.5\%$.

[SER130c] *429 Port 1*: The time of each active period, measured from the start of the bit to the start of the transition to "null", **shall** be $(T_Z / 2) \pm 5\%$.

[SER130d] *429 Port 1*: The rise time of transition from logic "null" to logic "high or from logic "low" to logic "null" **shall** be 10 ± 5μs, measured from 10% to 90% of the differential steady state outputs.

[SER130e] *429 Port 1*: The fall time of transition from logic "high" to logic "null" or from logic "null" to logic "low" **shall** be 10 ± 5μs, measured from 10% to 90% of the differential steady state outputs.

[SER130f] *429 Port 2*: The time T_W between the start of bit 0 and the start of bit 31 in the transmission **shall** be 2.14ms to 2.58ms. Compute the bit reference time $T_Z = (T_W / 31)$.

[SER130g] *429 Port 2*: The time T_B of each bit period, measured from the start of the bit to the start of the next bit, **shall** be $T_Z \pm 2.5\%$.

[SER130h] *429 Port 2*: The time of each active period, measured from the start of the bit to the start of the transition to "null", **shall** be $(T_Z / 2) \pm 5\%$.

[SER130i] *429 Port 2*: The rise time of transition from logic "null" to logic "high or from logic "low" to logic "null" **shall** be 10 ± 5μs, measured from 10% to 90% of the differential steady state outputs.

[SER130j] *429 Port 2*: The fall time of transition from logic "high" to logic "null" or from logic "null" to logic "low" **shall** be 10 ± 5μs, measured from 10% to 90% of the differential steady state outputs.

Reference: HRD R00091050, R00092230, R00092250, R00092270, R00092300, R00092310

5.9.6 [SER135] 429 Transmit Idle

Test Method: Measure the voltage between the indicated rear connector pin and *Ground*, with the indicated *429 Port* open-circuit.

Acceptance: [SER135a] *429 Port 1*, *Transmit A*: The measured voltage **shall** be 0.0 ± 0.2V.

[SER135b] *429 Port 1*, *Transmit B*: The measured voltage **shall** be 0.0 ± 0.2V.

[SER135c] *429 Port 2*, *Transmit A*: The measured voltage **shall** be 0.0 ± 0.2V.

[SER135d] *429 Port 2*, *Transmit B*: The measured voltage **shall** be 0.0 ± 0.2V.

Reference: HRD R00093010

5.9.7 [SER145] 429 Transmit Impedance

Test Method: For each indicated 429 Transmit port, connect R_L = 100Ω ± 1% load between the rear connector *Transmit A* and *Transmit B* pins. Place the output into the state indicated using the test mode interface and. Measure the DC voltage that develops across R_L as V_L. Replace R_L with R_H = 1kΩ ± 1% resistor and measure the DC voltage as V_H. Compute the transmit impedance R_O of the port as:

$$R_O = \frac{R_L R_H (V_H - V_L)}{V_L R_H - V_H R_L}$$

Acceptance:
- [SER145a] *429 Port 1*, Null: The impedance **shall** be 70Ω to 80Ω.
- [SER145b] *429 Port 1*, Low: The impedance **shall** be 70Ω to 80Ω.
- [SER145c] *429 Port 1*, High: The impedance **shall** be 70Ω to 80Ω.
- [SER145d] *429 Port 2*, Null: The impedance **shall** be 70Ω to 80Ω.
- [SER145e] *429 Port 2*, Low: The impedance **shall** be 70Ω to 80Ω.
- [SER145f] *429 Port 2*, High: The impedance **shall** be 70Ω to 80Ω.

Reference: HRD R00092100, R00092110, R00092120

5.9.8 [SER150] 429 Receive Open Circuit

Test Method: Leave the indicated *429 Receive* port open-circuit. Measure the indicated voltage.

Acceptance:
- [SER150a] Between *429 Port 1 Receive A* and *Receive B* **shall** be 0.0 ± 0.50V.
- [SER150b] Between *429 Port 2 Receive A* and *Receive B* **shall** be 0.0 ± 0.50V.
- [SER150c] Between *429 Port 3 Receive A* and *Receive B* **shall** be 0.0 ± 0.50V.

Reference: HRD R00093020

5.9.9 [SER155] 429 Receive Termination

Test Method: Put the appliance in the indicated power state; for appliance power off, wait at least 1min for the internal circuits to discharge. The measured resistance between the indicated terminals **shall** meet the tolerance indicated.

Acceptance:

[SER155a] Power On, *429 Port 1*, *Receive A* to *Receive B*: At least 12kΩ.

[SER155b] Power On, *429 Port 1*, *Receive A* to *Ground*: At least 12kΩ.

[SER155c] Power On, *429 Port 1*, *Receive B* to *Ground*: At least 12kΩ.

[SER155d] Power On, *429 Port 2*, *Receive A* to *Receive B*: At least 12kΩ.

[SER155e] Power On, *429 Port 2*, *Receive A* to *Ground*: At least 12kΩ.

[SER155f] Power On, *429 Port 2*, *Receive B* to *Ground*: At least 12kΩ.

[SER155g] Power On, *429 Port 3*, *Receive A* to *Receive B*: At least 12kΩ.

[SER155h] Power On, *429 Port 3*, *Receive A* to *Ground*: At least 12kΩ.

[SER155i] Power On, *429 Port 3*, *Receive B* to *Ground*: At least 12kΩ.

[SER155j] Power Off, *429 Port 1*, *Receive A* to *Receive B*: At least 12kΩ.

[SER155k] Power Off, *429 Port 1*, *Receive A* to *Ground*: At least 12kΩ.

[SER155l] Power Off, *429 Port 1*, *Receive B* to *Ground*: At least 12kΩ.

[SER155m] Power Off, *429 Port 2*, *Receive A* to *Receive B*: At least 12kΩ.

[SER155n] Power Off, *429 Port 2*, *Receive A* to *Ground*: At least 12kΩ.

[SER155o] Power Off, *429 Port 2*, *Receive B* to *Ground*: At least 12kΩ.

[SER155p] Power Off, *429 Port 3*, *Receive A* to *Receive B*: At least 12kΩ.

[SER155q] Power Off, *429 Port 3*, *Receive A* to *Ground*: At least 12kΩ.

[SER155r] Power Off, *429 Port 3*, *Receive B* to *Ground*: At least 12kΩ.

Reference: HRD R00092010, R00092020, R00092030

5.9.10 [SER160] 429 Receive High Speed

Test Method: Clear the receive data queue and configure the indicated *429 Receive* port to high speed using the test mode interface. Apply a signal with the following characteristics to the rear connector input of each indicated port.

- The signal representing the symbol sequence shall be "021202120202121202020212121202020202121212120202020202121212121212".
- Each symbol time shall last $\tau \pm 1\%$.
- Each "1" shall be signaled by driving *Receive A* at $+V_S \pm 0.1V$, and simultaneously driving *Receive B* at $-V_S \pm 0.1V$.
- Each "0" shall be signaled by driving *Receive A* at $-V_S \pm 0.1V$, and simultaneously driving *Receive B* at $+V_S \pm 0.1V$.
- Each "2" shall be signaled by driving *Receive A* at $-V_N \pm 0.1V$, and simultaneously driving *Receive B* at $+V_N \pm 0.1V$.
- Each transition shall be monotonic from 10% to 90% in $1.5 \pm 0.5\mu s$.

After applying the signal, read the received label in hexadecimal form using the test mode interface. The label **shall** be 0x531C3C1F.

Acceptance:

[SER160a] *429 Receive 1*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 4.8\mu s$.

[SER160b] *429 Receive 1*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 4.8\mu s$.

[SER160c] *429 Receive 1*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 4.8\mu s$.

[SER160d] *429 Receive 1*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 4.8\mu s$.

[SER160e] *429 Receive 2*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 4.8\mu s$.

[SER160f] *429 Receive 2*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 4.8\mu s$.

[SER160g] *429 Receive 2*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 4.8\mu s$.

[SER160h] *429 Receive 2*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 4.8\mu s$.

[SER160i] *429 Receive 3*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 4.8\mu s$.

[SER160j] *429 Receive 3*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 4.8\mu s$.

[SER160k] *429 Receive 3*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 4.8\mu s$.

[SER160l] *429 Receive 3*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 4.8\mu s$.

[SER160m] *429 Receive 1*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 5.2\mu s$.

[SER160n] *429 Receive 1*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 5.2\mu s$.

[SER160o] *429 Receive 1*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 5.2\mu s$.

[SER160p] *429 Receive 1*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 5.2\mu s$.

[SER160q] *429 Receive 2*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 5.2\mu s$.

[SER160r] *429 Receive 2*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 5.2\mu s$.

[SER160s] *429 Receive 2*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 5.2\mu s$.

[SER160t] *429 Receive 2*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 5.2\mu s$.

[SER160u] *429 Receive 3*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 5.2\mu s$.

[SER160v] *429 Receive 3*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 5.2\mu s$.

[SER160w] *429 Receive 3*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 5.2\mu s$.

[SER160x] *429 Receive 3*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 5.2\mu s$.

Reference: HRD R00091060, R00091100, R00091110, R00091120, R00092070, R00092080, R00092090, R00092320

5.9.11 [SER165] 429 Receive Low Speed

Test Method: Clear the receive data queue and configure the indicated *429 Receive* port to low speed using the test mode interface. Apply a signal with the following characteristics to the rear connector input of each indicated port.

- The signal representing the symbol sequence shall be "021202120202121202020212121202020202121212120202020202121212121212".
- Each symbol time shall last $\tau \pm 1\%$.
- Each "1" shall be signaled by driving *Receive A* at $+V_S \pm 0.1V$, and simultaneously driving *Receive B* at $-V_S \pm 0.1V$.
- Each "0" shall be signaled by driving *Receive A* at $-V_S \pm 0.1V$, and simultaneously driving *Receive B* at $+V_S \pm 0.1V$.
- Each "2" shall be signaled by driving *Receive A* at $-V_N \pm 0.1V$, and simultaneously driving *Receive B* at $+V_N \pm 0.1V$.
- Each transition shall be monotonic from 10% to 90% in $1.5 \pm 0.5\mu s$.

After applying the signal, read the received label in hexadecimal form using the test mode interface. The label **shall** be 0x531C3C1F.

Acceptance:

[SER165a] *429 Receive 1*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 51\mu s$.
[SER165b] *429 Receive 1*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 51\mu s$.
[SER165c] *429 Receive 1*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 51\mu s$.
[SER165d] *429 Receive 1*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 51\mu s$.
[SER165e] *429 Receive 2*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 51u\mu s$.
[SER165f] *429 Receive 2*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 51\mu s$.
[SER165g] *429 Receive 2*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 51\mu s$.
[SER165h] *429 Receive 2*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 51\mu s$.
[SER165i] *429 Receive 3*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 51u\mu s$.
[SER165j] *429 Receive 3*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 51\mu s$.
[SER165k] *429 Receive 3*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 51\mu s$.
[SER165l] *429 Receive 3*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 51\mu s$.
[SER165m] *429 Receive 1*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 3.2\mu s$.
[SER165n] *429 Receive 1*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 3.2\mu s$.
[SER165o] *429 Receive 1*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 3.2\mu s$.
[SER165p] *429 Receive 1*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 3.2\mu s$.
[SER165q] *429 Receive 2*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 3.2\mu s$.
[SER165r] *429 Receive 2*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 3.2\mu s$.
[SER165s] *429 Receive 2*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 3.2\mu s$.
[SER165t] *429 Receive 2*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 3.2\mu s$.
[SER165u] *429 Receive 3*, $V_S = 6.0V$, $V_N = 0.0V$, $\tau = 3.2\mu s$.
[SER165v] *429 Receive 3*, $V_S = 14.0V$, $V_N = 0.0V$, $\tau = 3.2\mu s$.
[SER165w] *429 Receive 3*, $V_S = 6.0V$, $V_N = 3.0V$, $\tau = 3.2\mu s$.
[SER165x] *429 Receive 3*, $V_S = 14.0V$, $V_N = 3.0V$, $\tau = 3.2\mu s$.

Reference: HRD R00091060, R00091100, R00091110, R00091120, R00092070, R00092080, R00092090, R00092330

5.9.12 [SER170] 429 Receive Capacitance

Test Method: Connect a 10kΩ resistor in series between the indicated pins. Drive the resistor with a 50% duty cycle 200Hz square wave between the indicated voltages V_{LO} and V_{HI}. For both rising and falling edges of the input wave measure the time τ required to transition between the previous steady-state voltage and 63% of the following steady-state voltage.

Acceptance: [SER170a] *429 Port 1 Receive A*, *Ground*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170b] *429 Port 1 Receive B*, *Ground*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170c] *429 Port 1 Receive A*, *Receive B*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170d] *429 Port 2 Receive A*, *Ground*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170e] *429 Port 2 Receive B*, *Ground*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170f] *429 Port 2 Receive A*, *Receive B*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170g] *429 Port 3 Receive A*, *Ground*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170h] *429 Port 3 Receive B*, *Ground*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

[SER170i] *429 Port 3 Receive A*, *Receive B*, V_{LO} = −1.0V, V_{HI} = +1.0V: τ **shall** be less than 5µs.

Reference: HRD R00092040, R00092050, R00092060

5.9.13 [SER175] 429 Receive Overdrive

Test Method: Run the test procedure against each of these ports:

- *429 Port 1 Receive*
- *429 Port 2 Receive*
- *429 Port 3 Receive*

Connect the appliance rear connector interface pins in each of the following configurations. Hold each configuration place for at least 10m while continuously transmitting 429 labels on the test port using the test mode interface.

- Connect *Receive A* to a low-impedance +29VDC source
- Connect *Receive A* to a low-impedance −29VDC source
- Connect *Receive A* to a low-impedance 30VAC RMS source
- Connect *Receive B* to a low-impedance +29VDC source
- Connect *Receive B* to a low-impedance −29VDC source
- Connect *Receive B* to a low-impedance 30VAC RMS source

Acceptance: [SER175a] Procedure **[SER100] shall** pass after this procedure is completed

Reference: HRD R00094090, R00094100, R00094110

5.9.14 [SER180] 429 Receive Safety

Test Method: Run the test procedure against each of these ports:

- *429 Port 1 Receive*
- *429 Port 2 Receive*
- *429 Port 3 Receive*

Connect the appliance rear connector interface pins in each of the following configurations. Hold each configuration place for at least 10m while continuously transmitting 429 labels on the test port using the test mode interface.

- Leave both *Receive A* and *Receive B* open-circuit
- Short-circuit *Receive A* to *Receive B*, but not to *Ground*
- Short-circuit *Receive A* to *Ground*, leave *Receive B* open-circuit
- Short-circuit *Receive B* to *Ground*, leave *Receive A* open-circuit
- Short-circuit both *Receive A* and *Receive B* to *Ground*

Acceptance: [SER180a] Procedure **[SER100] shall** pass after this procedure is completed

Reference: HRD R00094120, R00094130, R00094140, R00094150, R00094160

5.9.15 [SER185] 429 Transmit Safety

Test Method: Run the test procedure against each of these ports in the indicated configuration:

- *429 Port 1 Transmit*, Low Speed
- *429 Port 1 Transmit*, High Speed
- *429 Port 2 Transmit*, Low Speed
- *429 Port 2 Transmit*, High Speed

Connect the appliance rear connector interface pins in each of the following configurations. Hold each configuration place for at least 10m while continuously transmitting 429 labels on the test port using the test mode interface.

- Leave both *Transmit A* and *Transmit B* open-circuit
- Short-circuit *Transmit A* to *Transmit B*, but not to *Ground*
- Short-circuit *Transmit A* to *Ground*, leave *Transmit B* open-circuit
- Short-circuit *Transmit B* to *Ground*, leave *Transmit A* open-circuit
- Short-circuit both *Transmit A* and *Transmit B* to *Ground*

Acceptance: [SER185a] Procedure **[SER100] shall** pass after this procedure is completed

Reference: HRD R00094040, R00094050, R00094060, R00094070, R00094080

5.10 ETHERNET

5.10.1 [ETH100] Ethernet Loopback

Test Method: Connect the *Transmit* and *Receive* signals as indicated and transmit at least 10 successive non-synchronous packets with varying contents through each port at the highest supported speed. Read the loopback status using the test mode interface as:

- "Pending", if the minimum number of test packets has not been transmitted;
- "Passing", if a bitwise identical packet was received in proper order for each transmitted packet
- "Failing", otherwise.

Acceptance: [ETH100a] The status of *Ethernet 1 Receive* when *Ethernet 2 Transmit* is connected to *Ethernet 1 Receive* **shall** be Passing.

[ETH100b] The status of *Ethernet 2 Receive* when *Ethernet 1 Transmit* is connected to *Ethernet 2 Receive* **shall** be Passing.

Reference: SRD R00253663

5.10.2 [ETH110] Ethernet Speed

Test Method: Observe the differential *Transmit* signals of the indicated ports. Measure the time between successive bits in a transmission.

Acceptance: [ETH100a] *Ethernet 1*: The bit time shall be 100 ± 1µs.

[ETH100b] *Ethernet 2*: The bit time shall be 100 ± 1µs.

Reference: HRD R00103030

5.11 I2C

5.11.1 [IIC100] I2C Device Status

Test Method: Read the status of each of the following I2C devices on the bus by sending a valid read or write command to each one.

Acceptance: [IIC100a] *Audio Codec*: The test **shall** pass if the device acknowledges the command with an expected response.

[IIC100b] *Internal EEPROM*: If I802 is populated on the *Main Board*, the test **shall** pass if the device acknowledges the command with an expected response.

[IIC100c] *Config Module*: The test **shall** pass if the device acknowledges the command with an expected response.

[IIC100d] *Digital Potentiometer*: The test **shall** pass if the device acknowledges the command with an expected response.

Reference: SRD R00230109

5.12 USB

5.12.1 [USB100] USB Connection

Test Method: Connect the appliance device USB port to a USB 2.0 compliant host port on a PC running Windows® 2000 or later.

Acceptance: [USB100a] The USB device shall be recognized by the Windows® Device Manager as “GDL88”.

Reference: HRD R00121040

5.13 AUDIO

5.13.1 [AUD100] Audio Output Test

Test Method: Enable the appliance audio test mode output using the test mode interface. Place a 500Ω load between the *Audio High* and *Audio Low* output pins on the connector. Measure the signal across this load.

Acceptance: [AUD100a] The amplitude of the signal **shall** be greater than 6.00V RMS.

[AUD100b] The frequency of the signal **shall** be 1kHz ± 2%.

[AUD100c] The distortion of the signal **shall** be less than 10%.

Reference: HRD R00132010, R00132020; SRD R00255417

5.13.2 [AUD110] Audio Attenuation

Test Method: Remove the appliance main board cover and connect a frequency generator in place of *Codec Output*. Disable the codec using the test mode interface. Set the generator to output a sine wave of constant amplitude and vary the frequency between 20Hz and 20kHz. Measure the RMS voltage amplitude of the differential output across a 500Ω load placed between *Audio High* and *Audio Low* on the appliance rear connector for at least 3 points per decade.

Acceptance: [AUD110a] The difference between the highest RMS amplitude measured and the lowest RMS amplitude measured **shall** be no more than 1% of the highest.

Reference: HRD R00132030

5.13.3 [AUD120] Audio Current Limit

Test Method: Connect a 1Ω resistor in each indicated configuration and measure the voltage across the terminals while in the appliance audio test mode.

Acceptance: [AUD120a] Between *Audio High* and *Ground*: The maximum voltage **shall** be no more than 120mV.

[AUD120b] Between *Audio Low* and *Ground*: The maximum voltage **shall** be no more than 120mV.

[AUD120c] Between *Audio High* and *Audio Low*: The maximum voltage **shall** be no more than 120mV.

Reference: HRD R00134010, R00134020

5.13.4 [AUD130] Audio Safety

Test Method: Enable the appliance audio test mode at maximum output power using the test mode interface. Sequentially connect the rear interface pins in the following configurations and hold at least 10m each:

- Leave both *Audio High* and *Audio Low* open-circuit
- Short-circuit *Audio High* to *Ground*; leave *Audio Low* open-circuit
- Short-circuit *Audio Low* to *Ground*; leave *Audio High* open-circuit
- Short-circuit both *Audio Low* and *Audio High* to *Ground*
- Short-circuit *Audio Low* and *Audio High* together but not to *Ground*

Acceptance: [AUD130a] Procedure **[AUD100] shall** pass after this procedure is completed.

Reference: HRD R00134030, R00134040, R00134050, R00134060, R00134070

5.14 PPS

5.14.1 [PPS100] PPS Input Open Circuit

Test Method: Set the PPS direction of the indicated port to input using the test mode interface. Measure the voltage on PPS High and PPS Low of the indicated port when both pins are open-circuit.

Acceptance:
[PPS100a] *PPS Port 1*: The voltage on *PPS Low* **shall** be 1.36V.
[PPS100b] *PPS Port 1*: The voltage on *PPS Low* **shall** be 1.14V.
[PPS100c] *PPS Port 2*: The voltage on *PPS Low* **shall** be 1.36V.
[PPS100d] *PPS Port 2*: The voltage on *PPS Low* **shall** be 1.14V.

Reference: HRD R00143020

5.14.2 [PPS110] PPS Differential Input | Full

Test Method: Set the PPS direction of the indicated port to input using the test mode interface. Generate 10 differential pulses that meet the following characteristics for each indicated V_{CM}, repeating the signal every 1.0s

- *PPS High* is (V_{CM} + 0.05V) ± 0.01V for 1ms, (V_{CM} − 0.05V) ± 0.01V thereafter.
- *PPS Low* is (V_{CM} − 0.05V) ± 0.01V for 1ms, (V_{CM} + 0.05V) ± 0.01V thereafter.
- The rising edge and falling edges of the pulse, measured differentially between *PPS High* and *PPS Low*, shall be monotonic transitions between $-0.9 \cdot V_{SS}$ and $0.9 \cdot V_{SS}$ in less than 200ns, where V_{SS} is the previous steady-state differential.
- Pulse width, between crossings of $0.9 \cdot V_{SS}$, shall be 1.0 ± 0.01ms.

While inputting the pulses, observe the voltage of the indicated internal *PPS Input* signal as it is input to the FPGA.

Acceptance:
[PPS110a] *PPS Port 1*, V_{CM} = 0.0V: *PPS Input 1* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110b] *PPS Port 1*, V_{CM} = 2.5V: *PPS Input 1* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110c] *PPS Port 1*, V_{CM} = 5.0V: *PPS Input 1* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110d] *PPS Port 1*, V_{CM} = −5.0V: *PPS Input 1* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110e] *PPS Port 2*, V_{CM} = 0.0V: *PPS Input 2* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110f] *PPS Port 2*, V_{CM} = 2.5V: *PPS Input 2* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110g] *PPS Port 2*, V_{CM} = 5.0V: *PPS Input 2* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.
[PPS110h] *PPS Port 2*, V_{CM} = −5.0V: *PPS Input 2* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.

Reference: HRD R00141030, R00141040, R00142060, R00142070, R00142080, R00142090

5.14.3 [PPS115] PPS Differential Input | Fast

Test Method: Set the PPS direction of the indicated port to input and read the PPS count using the test mode interface. Generate at least 10 PPS differential pulses, repeating every 1.0s, such that *PPS High* is 5.0V and *PPS Low* is 0.0V during the pulse, and vice versa between pulses

Acceptance: [PPS115a] *PPS Port 1*: The port **shall** detect a valid PPS signal.

[PPS115b] *PPS Port 2*: The port **shall** detect a valid PPS signal.

Reference: HRD R00141030, R00141040

5.14.4 [PPS120] PPS Differential Input Inactive

Test Method: Set the PPS direction of the indicated port to input using the test mode interface. Generate 10 differential pulses that meet the following characteristics for each indicated V_{CM}, repeating the signal every 1.0s

- *PPS High* is (V_{CM} − 0.15V) ± 0.01V for 1ms, (V_{CM} − 1.05V) ± 0.01V thereafter.
- *PPS Low* is (V_{CM} − 0.05V) ± 0.01V for 1ms, (V_{CM} + 0.05V) ± 0.01V thereafter.
- The rising edge and falling edges of the pulse, measured differentially between *PPS High* and *PPS Low*, shall be monotonic transitions between $-0.9 \cdot V_{SS}$ and $0.9 \cdot V_{SS}$ in less than 200ns, where V_{SS} is the previous steady-state differential.
- Pulse width, between crossings of $0.9 \cdot V_{SS}$, shall be 1.0 ± 0.01ms.

While inputting the pulses, observe the voltage of the indicated internal *PPS Input* signal as it is input to the FPGA.

Acceptance: [PPS120a] *PPS Port 1*, V_{CM} = 0.0V: *PPS Input 1* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120b] *PPS Port 1*, V_{CM} = 2.5V: *PPS Input 1* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120c] *PPS Port 1*, V_{CM} = 5.0V: *PPS Input 1* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120d] *PPS Port 1*, V_{CM} = −5.0V: *PPS Input 1* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120e] *PPS Port 2*, V_{CM} = 0.0V: *PPS Input 2* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120f] *PPS Port 2*, V_{CM} = 2.5V: *PPS Input 2* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120g] *PPS Port 2*, V_{CM} = 5.0V: *PPS Input 2* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS120h] *PPS Port 2*, V_{CM} = −5.0V: *PPS Input 2* **shall** be 0.0 ± 0.5V during the entire test period.

Reference: HRD R00142060, R00142070, R00142080, R00142100

5.14.5 [PPS130] PPS Single-Ended Input | Full

Test Method: Set the PPS direction of the indicated port to input using the test mode interface. Let *PPS Low* be open-circuit. Generate 10 differential pulses that meet the following characteristics, repeating the signal every 1.0s.

- *PPS High* shall be V_{HI} = 2.9 ± 0.1V for 1ms, V_{LO} = 2.1 ± 0.1V thereafter.
- The rising edge and falling edges of the pulse shall be monotonic transitions between (V_{LO} + 0.1·V_{SS}) and (V_{LO} + 0.9·V_{SS}) in less than 200ns, where V_{SS} is the actual V_{HI} − V_{LO}.
- Pulse width, between crossings of (V_{LO} + 0.9·V_{SS}), **shall** be 1.0 ± 0.01ms.

While inputting the pulses, observe the voltage of the indicated internal *PPS Input* signal as it is input to the FPGA.

Acceptance: [PPS130a] *PPS Port 1*: *PPS Input 1* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.

[PPS130b] *PPS Port 2*: *PPS Input 2* **shall** be 3.0 ± 0.5V during the 1ms pulse period, 0.5 ± 0.5V otherwise.

Reference: HRD R00141030, R00141040, R00142110

5.14.6 [PPS135] PPS Single-Ended Input | Fast

Test Method: Set the PPS direction of the indicated port to input and read the PPS count using the test mode interface. Let *PPS Low* be open-circuit. Generate at least 10 pulses on *PPS High*, repeating every 1.0s, driving 5.0V during each 1.0ms long pulse and 0.0V between pulses.

Acceptance: [PPS135a] *PPS Port 1*: The port **shall** detect a valid PPS signal.

[PPS135b] *PPS Port 2*: The port **shall** detect a valid PPS signal.

Reference: HRD R00141030, R00141040

5.14.7 [PPS140] PPS Single-Ended Inactive

Test Method: Set the PPS direction of the indicated port to input using the test mode interface. Let *PPS Low* be open-circuit. Generate at least 10 pulses on *PPS High*, repeating every 1.0s, driving 2.2V during each 1.0ms long pulse and 0.0V between pulses. While inputting the pulses, observe the voltage of the indicated internal *PPS Input* signal as it is input to the FPGA

Acceptance: [PPS140a] *PPS Port 1*: *PPS Input 1* **shall** be 0.0 ± 0.5V during the entire test period.

[PPS140b] *PPS Port 2*: *PPS Input 2* **shall** be 0.0 ± 0.5V during the entire test period.

Reference: HRD R00142120

5.14.8 [PPS150] PPS Output Pulse

Test Method: If an internal WAAS module is installed, set the PPS direction of the indicated port to output using the test mode interface, and wait until the GPS mode is "3D fix". Observe *PPS High* and *PPS Low* across a 1kΩ differential load. Let V_{SE} be 5.0V.

Acceptance:

[PPS150a] *PPS Port 1*: *PPS High* **shall** be between $0.9 \cdot V_{SE}$ and $1.1 \cdot V_{SE}$ during the entire PPS pulse time.

[PPS150b] *PPS Port 1*: *PPS Low* **shall** be between $0.9 \cdot V_{SE}$ and $1.1 \cdot V_{SE}$ whenever a PPS pulse is not being generated.

[PPS150c] *PPS Port 1*: *PPS High* **shall** be between $-0.1 \cdot V_{SE}$ and $0.1 \cdot V_{SE}$ whenever a PPS pulse is not being generated.

[PPS150d] *PPS Port 1*: *PPS High* **shall** be between $-0.1 \cdot V_{SE}$ and $0.1 \cdot V_{SE}$ during the entire PPS pulse time .

[PPS150e] *PPS Port 1*: The differential rising edge between *PPS High* and *PPS Low*, from 10% to 90%, **shall** be monotonic and less than 200ns.

[PPS150f] *PPS Port 1*: The differential falling edge between *PPS High* and *PPS Low*, from 90% to 10%, **shall** be monotonic and less than 200ns.

[PPS150g] *PPS Port 1*: The pulse length when *PPS High* is higher than *PPS Low*, measured 90% of the rising edge to the falling edge, **shall** be 1.0 ± 0.01ms.

[PPS150h] *PPS Port 2*: *PPS High* **shall** be between $0.9 \cdot V_{SE}$ and $1.1 \cdot V_{SE}$ during the entire PPS pulse time.

[PPS150i] *PPS Port 2*: *PPS Low* **shall** be between $0.9 \cdot V_{SE}$ and $1.1 \cdot V_{SE}$ whenever a PPS pulse is not being generated.

[PPS150j] *PPS Port 2*: *PPS High* **shall** be between $-0.1 \cdot V_{SE}$ and $0.1 \cdot V_{SE}$ whenever a PPS pulse is not being generated.

[PPS150k] *PPS Port 2 PPS High* **shall** be between $-0.1 \cdot V_{SE}$ and $0.1 \cdot V_{SE}$ during the entire PPS pulse time .

[PPS150l] *PPS Port 2*: The differential rising edge between *PPS High* and *PPS Low*, from 10% to 90%, **shall** be monotonic and less than 200ns.

[PPS150m] *PPS Port 2*: The differential falling edge between *PPS High* and *PPS Low*, from 90% to 10%, **shall** be monotonic and less than 200ns.

[PPS150n] *PPS Port 2*: The pulse length when *PPS High* is higher than *PPS Low*, measured 90% of the rising edge to the falling edge, **shall** be 1.0 ± 0.01ms.

Reference: HRD R00141030, R00142030, R00142040, R00142050, R00143010

5.14.9 [PPS160] PPS Output Timing

Test Method: If an internal WAAS module is installed, set the PPS direction of the indicated port to output using the test mode interface, and wait until the GPS fix mode is "3D fix". Observe the differential voltage between *PPS High* to *PPS Low*.

Acceptance: [PPS160a] *PPS Port 1*: The time between two successive rising edges **shall** be 1.0s ± 275ns.

[PPS160b] *PPS Port 1*: The absolute error between the rising edge and the true UTC epoch shall be less than 275ns.

[PPS160c] *PPS Port 2*: The time between two successive rising edges **shall** be 1.0s ± 275ns.

[PPS160d] *PPS Port 2*: The absolute error between the rising edge and the true UTC epoch shall be less than 275ns.

Reference: HRD R00142010, R00142130

5.14.10 [PPS200] PPS Current Limit

Test Method: Set the indicated PPS port to the indicated mode using the test mode interface, and connect a 1Ω resistor across the indicated terminals. For each test, the maximum voltage measured across the resistor **shall** be no more than 120mV.

Acceptance: [PPS200a] *PPS Port 1*, output mode, between *PPS High* and *Ground*.

[PPS200b] *PPS Port 1*, output mode, between *PPS Low* and *Ground*.

[PPS200c] *PPS Port 1*, output mode, between *PPS High* and *PPS Low*.

[PPS200d] *PPS Port 1*, input mode, between *PPS High* and *Ground*.

[PPS200e] *PPS Port 1*, input mode, between *PPS Low* and *Ground*.

[PPS200f] *PPS Port 1*, input mode, between *PPS High* and *PPS Low*.

[PPS200g] *PPS Port 2*, output mode, between *PPS High* and *Ground*.

[PPS200h] *PPS Port 2*, output mode, between *PPS Low* and *Ground*.

[PPS200i] *PPS Port 2*, output mode, between *PPS High* and *PPS Low*.

[PPS200j] *PPS Port 2*, input mode, between *PPS High* and *Ground*.

[PPS200k] *PPS Port 2*, input mode, between *PPS Low* and *Ground*.

[PPS200l] *PPS Port 2*, input mode, between *PPS High* and *PPS Low*.

Reference: HRD R00144010, R00144020

5.14.11 [PPS210] PPS Port Safety

Test Method: Set the indicated PPS port mode as indicated using the test mode interface. Sequentially connect the appliance rear connector interface pins according to each of the following configurations, and hold at least 10m each.

- Leave both *PPS High* and *PPS Low* open-circuit
- Short-circuit *PPS High* to *Ground*, leave *PPS Low* open-circuit
- Short-circuit *PPS Low* to *Ground*, leave *PPS Low* open-circuit
- Short-circuit both *PPS Low* and *PPS Low* to *Ground*

Acceptance: [PPS210a] *PPS Port 1*, output mode: Procedure **[PPS150] shall** pass after all configurations are completed

[PPS210b] *PPS Port 1*, input mode: Procedures **[PPS110]** and **[PPS130] shall** pass after all configurations are completed

[PPS210c] *PPS Port 2*, output mode: Procedure **[PPS150] shall** pass after all configurations are completed

[PPS210d] *PPS Port 2*, input mode: Procedures **[PPS110]** and **[PPS130] shall** pass after all configurations are completed

Reference: HRD R00144030, R00144040, R00144050, R00144060, R00144070

5.15 RESERVED

5.16 978 UAT TX

5.16.1 [UAT100] UAT Tx Carrier Frequency

Test Method: Perform the test described in DO-282B §2.4.2.1.

Acceptance: [UAT100a] The transmission frequency **shall** be 978MHz ± 20ppm.

Reference: HRD R00162030

5.16.2 [UAT110] UAT Tx Modulation Type

Test Method: Perform the test described in DO-282B §2.4.2.3.

Acceptance: [UAT110a] Each data "1' shall be modulated onto the carrier with an upward frequency shift of 312.5kHz.

[UAT110b] Each data "0' shall be modulated onto the carrier with a downward frequency shift of 312.5kHz.

[UAT110c] The modulation index shall be +0.6.

Reference: HRD R00161030, R00163010, R00163020, R00163030

5.16.3 [UAT120] UAT Tx Modulation Distortion

Test Method: Perform the test described in DO-282B §2.4.2.4.

Acceptance: [UAT120a] The minimum vertical opening of the eye diagram of the transmitted signal (measured at the optimum sampling points) **shall** be no less than 560kHz when measured over an entire Long ADS-B message containing pseudorandom payload data.

[UAT120b] The minimum horizontal opening of the eye diagram of the transmitted signal (measured at 978MHz) shall be no less than 0.624μs when measured over an entire Long ADS-B message containing pseudorandom payload data.

Reference: HRD R00162040, R00162050, R00162060

5.16.4 [UAT130] UAT Tx Output Power | Full

Test Method: Perform the test described in DO-282B §2.4.2.5 for each antenna port.

Acceptance: [UAT130a] Prior to 8 bits before the reference time, the average RF output power **shall not** exceed −80dBm.

[UAT130b] Between 8 and 6 bit periods prior to the reference time, the RF output power **shall** remain below 24dBm.

[UAT130c] During the active state, defined as beginning at the reference time and continuing for the duration of the message (420 bit periods for the Long ADS-B message) the RF power **shall** remain between 45 and 46.75dBm.

[UAT130d] The RF power **shall not** exceed 46.75dBm at any time during the ADS-B message transmission interval.

[UAT130e] Within 6 bit periods after the end of the active state, the average RF output power **shall** be below 24dBm.

[UAT130f] Within 8 bit periods after the end of the active state the average RF output power **shall** be less than −80dBm.

[UAT130g] The power measured at the inactive antenna port **shall** be less than 20dB below the power at the active UAT Antenna port.

[UAT130h] The *Power Detect* of the inactive antenna port **shall not** be asserted during the test.

[UAT130i] The *Power Detect* of the selected antenna port **shall** be asserted during the test.

[UAT140j] The FSK modulation of the transmitter output **shall** correspond to the expected message contents.

Reference: HRD R00162010, R00162020, R00162070, R00162080, R00162090, R00162100, R00162110, R00162120, R00162130

5.16.5 [UAT135] UAT Tx Output Power | Fast

Test Method: Perform the test described in DO-282B §2.4.2.5 for each antenna port.

Acceptance: [UAT135a] During the active state, defined as beginning at the reference time and continuing for the duration of the message (420 bit periods for the Long ADS-B message) the RF power **shall** remain between 45 and 46.75dBm.

[UAT135b] The RF power **shall not** exceed 46.75dBm at any time during the ADS-B message transmission interval.

[UAT135c] The power measured at the inactive antenna port **shall** be less than 20dB below the power at the active UAT Antenna port.

[UAT135d] The *Power Detect* of the inactive antenna port **shall not** be asserted during the test.

[UAT135e] The *Power Detect* of the selected antenna port **shall** be asserted during the test.

[UAT135f] The FSK modulation of the transmitter output **shall** correspond to the expected message contents.

Reference: HRD R00162010, R00162020, R00162070, R00162100, R00162110

5.16.6 [UAT150] UAT Tx In-Band Spectrum

Test Method: Perform the test described in DO-282B §2.4.2.6.

Acceptance: [UAT150a] The average spectrum of a UAT message transmission modulated with pseudorandom payload data **shall** fall within the limits specified in DO-282 Table 2-3 when measured in a 100kHz bandwidth. (The transmit in-band spectrum is specified for ±3.25MHz.)

Reference: HRD R00162140

5.16.7 [UAT160] UAT Tx Out-of-Band Emissions

Test Method: Perform the test described in DO-282B §2.4.2.7 over the frequency range 0Hz to 9.67GHz.

Acceptance: [UAT160a] All out-of-band emissions **shall** be less than 60dB below the maximum measured output.

Reference: HRD R00162150

5.16.8 [UAT170] UAT Tx Transmission Cycle

Test Method: Perform the test described in DO-282B §2.4.6.1.3. When testing Airborne mode, start verifying the following steps after the appliance transmits payload "A" from the *Top Antenna*.

Acceptance:

[UAT170a] Step 2: Message 2 **shall** be payload "B" from the *Top Antenna*.

[UAT170b] Step 2: Message 3 **shall** be payload "C" from the *Bottom Antenna*.

[UAT170c] Step 2: Message 4 **shall** be payload "D" from the *Bottom Antenna*.

[UAT170d] Step 2: Message 5 **shall** be payload "D" from the *Top Antenna*.

[UAT170e] Step 2: Message 6 **shall** be payload "A" from the *Top Antenna*.

[UAT170f] Step 2: Message 7 **shall** be payload "B" from the *Bottom Antenna*.

[UAT170g] Step 2: Message 8 **shall** be payload "C" from the *Bottom Antenna*.

[UAT170h] Step 2: Message 9 **shall** be payload "C" from the *Top Antenna*.

[UAT170i] Step 2: Message 10 **shall** be payload "D" from the *Top Antenna*.

[UAT170j] Step 2: Message 11 **shall** be payload "A" from the *Bottom Antenna*.

[UAT170k] Step 2: Message 12 **shall** be payload "B" from the *Bottom Antenna*.

[UAT170l] Step 2: Message 13 **shall** be payload "B" from the *Top Antenna*.

[UAT170m] Step 2: Message 14 **shall** be payload "C" from the *Top Antenna*.

[UAT170n] Step 2: Message 15 **shall** be payload "D" from the *Bottom Antenna*.

[UAT170o] Step 2: Message 16 **shall** be payload "A" from the *Bottom Antenna*.

[UAT170p] Step 2: Message 17 **shall** be payload "A" from the *Top Antenna*.

[UAT170q] Step 4: All messages shall be transmitted from the *Bottom Antenna*.

Reference: HRD R00163070, R00163080

5.16.9 [UAT190] UAT Tx MSO Timing Tolerance

Test Method: Perform the test described in DO-282B §2.4.6.2.2 using the indicated PPS source.

Acceptance: [UAT190a] Step 3, WAAS Engine, MSO 752: The optimum sampling point of the first bit **shall** occur 194034.56 ± 0.50µs after the PPS epoch.

[UAT190b] Step 3, WAAS Engine, MSO 2352: The optimum sampling point of the first bit **shall** occur 594034.56 ± 0.50µs after the PPS epoch.

[UAT190c] Step 3, WAAS Engine, MSO 3951: The optimum sampling point of the first bit **shall** occur 993784.56 ± 0.50µs after the PPS epoch.

[UAT190d] Step 3, *PPS Input 1*, MSO 752: The optimum sampling point of the first bit **shall** occur 194034.56 ± 0.50µs after the PPS epoch.

[UAT190e] Step 3, *PPS Input 1*, MSO 2352: The optimum sampling point of the first bit **shall** occur 594034.56 ± 0.50µs after the PPS epoch.

[UAT190f] Step 3, *PPS Input 1*, MSO 3951: The optimum sampling point of the first bit **shall** occur 993784.56 ± 0.50µs after the PPS epoch.

[UAT190g] Step 3, *PPS Input 2*, MSO 752: The optimum sampling point of the first bit **shall** occur 194034.56 ± 0.50µs after the PPS epoch.

[UAT190h] Step 3, *PPS Input 2*, MSO 2352: The optimum sampling point of the first bit **shall** occur 594034.56 ± 0.50µs after the PPS epoch.

[UAT190i] Step 3, *PPS Input 2*, MSO 3951: The optimum sampling point of the first bit **shall** occur 993784.56 ± 0.50µs after the PPS epoch.

Reference: HRD R00162160, R00162170

5.16.10 [UAT200] UAT Tx Turnaround Time | Full

Test Method: Transmit 50 successive Long ADS-B messages “A” into the indicated antenna port, starting 25ms before the PPS epoch with an interval of 500µs. Transmit 50 successive Long ADS-B messages “B”, with contents differing from “A”, into the same antenna port starting 450µs after the PPS epoch, with an interval of 500µs. Command the appliance to transmit a long ADS-B message at the PPS epoch

Acceptance: [UAR200a] A long ADS-B message shall be transmitted.

[UAR200b] At least 46 of Long ADS-B messages “A” shall be received.

[UAR200c] At least 46 of Long ADS-B messages “B” shall be received.

Reference: HRD R00162180, R00162200

5.16.11 [UAT205] UAT Tx Turnaround Time | Fast

Test Method: Perform the test described in DO-282B §2.4.11.1.

Acceptance: [UAR200a] Step 3: Long ADS-B message A shall be received.

[UAR200b] Step 3: Long ADS-B message B shall be received.

[UAR200c] Step 3: A Long ADS-B message shall be transmitted.

Reference: HRD R00162180, R00162200

5.16.12 [UAT220] UAT Tx Antenna Safety

Test Method: Remove the appliance cover and disconnect both antennas. Select the indicated antenna port and command the appliance to transmit a Long ADS-B message.

Acceptance: [UAT220a] *Top Antenna*: The *Top Antenna Test* signal **shall** indicate a failure condition.

[UAT220b] *Top Antenna*: The transmitter *RF Amplifier Enable* **shall not** be asserted during the transmission.

[UAT220c] *Bottom Antenna*: The *Bottom Antenna Test* signal **shall** indicate a failure condition.

[UAT220d] *Bottom Antenna*: The transmitter *RF Amplifier Enable* **shall not** be asserted during the transmission.

Reference: HRD R00153110

5.17 978 UAT RX

5.17.1 [UAR100] UAT Rx Switching Diversity | Full

Test Method: Perform the test described in DO-282B §2.4.8.1.2.

Acceptance: [UAR100aa] Step 1: Exactly 50 each of message “A” and “B” **shall** be received.

[UAR100ab] Step 2, 0ms: Exactly 100 message “B” **shall** be received.

[UAR100ac] Step 2, 50ms: Exactly 100 message “B” **shall** be received.

[UAR100ad] Step 2, 100ms: Exactly 100 message “B” **shall** be received.

[UAR100ae] Step 2, 150ms: Exactly 100 message “B” **shall** be received.

[UAR100af] Step 2, 185.58ms: Exactly 100 message “B” **shall** be received.

[UAR100ag] Step 3: At least one of the two messages **shall** be received for each indicated message start time.

[UAR100ah] Step 4: At least one of the two messages **shall** be received for each indicated message start time.

[UAR100ai] Step 5, 190.42ms: Exactly 79 messages **shall** be received.

[UAR100aj] Step 5, 190.82ms: Exactly 79 messages **shall** be received.

[UAR100ak] Step 5, 191.22ms: Exactly 79 messages **shall** be received.

[UAR100al] Step 5, 191.62ms: Exactly 79 messages **shall** be received.

[UAR100am] Step 5, 192.02ms: Exactly 79 messages **shall** be received.

[UAR100an] Step 5, 192.42ms: Exactly 79 messages **shall** be received.

[UAR100ao] Step 5, 192.82ms: Exactly 79 messages **shall** be received.

[UAR100ap] Step 5, 193.22ms: Exactly 79 messages **shall** be received.

[UAR100aq] Step 5, 193.62ms: Exactly 79 messages **shall** be received.

[UAR100ar] Step 5, 194.02ms: Exactly 79 messages **shall** be received.

[UAR100as] Step 5, 194.42ms: Exactly 79 messages **shall** be received.

[UAR100at] Step 5, 194.82ms: Exactly 79 messages **shall** be received.

[UAR100au] Step 5, 195.22ms: Exactly 79 messages **shall** be received.

[UAR100av] Step 5, 195.62ms: Exactly 79 messages **shall** be received.

[UAR100aw] Step 5, 196.02ms: Exactly 79 messages **shall** be received.

[UAR100ax] Step 5, 196.42ms: Exactly 79 messages **shall** be received.

[UAR100ay] Step 5, 196.82ms: Exactly 79 messages **shall** be received.

[UAR100az] Step 5, 197.22ms: Exactly 79 messages **shall** be received.

[UAR100ba] Step 5, 197.62ms: Exactly 79 messages **shall** be received.

[UAR100bb] Step 5, 198.02ms: Exactly 79 messages **shall** be received.

[UAR100bc] Step 5, 198.42ms: Exactly 79 messages **shall** be received.

[UAR100bd] Step 5, 198.82ms: Exactly 79 messages **shall** be received.

[UAR100be] Step 5, 199.22ms: Exactly 79 messages **shall** be received.

[UAR100bf] Step 5, 199.62ms: Exactly 79 messages **shall** be received.

[UAR100bg] Step 5, 200.02ms: Exactly 79 messages **shall** be received.

[UAR100bh] Step 5, 200.42ms: Exactly 79 messages **shall** be received.

[UAR100bi] Step 5, 200.82ms: Exactly 79 messages **shall** be received.
[UAR100bj] Step 5, 201.22ms: Exactly 79 messages **shall** be received.
[UAR100bk] Step 5, 201.62ms: Exactly 79 messages **shall** be received.
[UAR100bl] Step 5, 202.02ms: Exactly 79 messages **shall** be received.
[UAR100bm] Step 5, 202.42ms: Exactly 79 messages **shall** be received.
[UAR100bn] Step 5, 202.82ms: Exactly 79 messages **shall** be received.
[UAR100bo] Step 5, 203.22ms: Exactly 79 messages **shall** be received.
[UAR100bp] Step 5, 203.62ms: Exactly 79 messages **shall** be received.
[UAR100bq] Step 5, 204.02ms: Exactly 79 messages **shall** be received.
[UAR100br] Step 5, 204.42ms: Exactly 79 messages **shall** be received.
[UAR100bs] Step 5, 204.82ms: Exactly 79 messages **shall** be received.
[UAR100bt] Step 5, 205.22ms: Exactly 79 messages **shall** be received.
[UAR100bu] Step 5, 205.62ms: Exactly 79 messages **shall** be received.
[UAR100bv] Step 5, 206.02ms: Exactly 79 messages **shall** be received.
[UAR100bw] Step 5, 206.42ms: Exactly 79 messages **shall** be received.
[UAR100bx] Step 5, 206.82ms: Exactly 79 messages **shall** be received.
[UAR100by] Step 5, 207.22ms: Exactly 79 messages **shall** be received.
[UAR100bz] Step 5, 207.58ms: Exactly 79 messages **shall** be received.
[UAR100ca] Step 6, 190.42ms: Exactly 79 messages **shall** be received.
[UAR100cb] Step 6, 190.82ms: Exactly 79 messages **shall** be received.
[UAR100cc] Step 6, 191.22ms: Exactly 79 messages **shall** be received.
[UAR100cd] Step 6, 191.62ms: Exactly 79 messages **shall** be received.
[UAR100ce] Step 6, 192.02ms: Exactly 79 messages **shall** be received.
[UAR100cf] Step 6, 192.42ms: Exactly 79 messages **shall** be received.
[UAR100cg] Step 6, 192.82ms: Exactly 79 messages **shall** be received.
[UAR100ch] Step 6, 193.22ms: Exactly 79 messages **shall** be received.
[UAR100ci] Step 6, 193.62ms: Exactly 79 messages **shall** be received.
[UAR100cj] Step 6, 194.02ms: Exactly 79 messages **shall** be received.
[UAR100ck] Step 6, 194.42ms: Exactly 79 messages **shall** be received.
[UAR100cl] Step 6, 194.82ms: Exactly 79 messages **shall** be received.
[UAR100cm] Step 6, 195.22ms: Exactly 79 messages **shall** be received.
[UAR100cn] Step 6, 195.62ms: Exactly 79 messages **shall** be received.
[UAR100co] Step 6, 196.02ms: Exactly 79 messages **shall** be received.
[UAR100cp] Step 6, 196.42ms: Exactly 79 messages **shall** be received.
[UAR100cq] Step 6, 196.82ms: Exactly 79 messages **shall** be received.
[UAR100cr] Step 6, 197.22ms: Exactly 79 messages **shall** be received.
[UAR100cs] Step 6, 197.62ms: Exactly 79 messages **shall** be received.
[UAR100ct] Step 6, 198.02ms: Exactly 79 messages **shall** be received.
[UAR100cu] Step 6, 198.42ms: Exactly 79 messages **shall** be received.
[UAR100cv] Step 6, 198.82ms: Exactly 79 messages **shall** be received.

[UAR100cw] Step 6, 199.22ms: Exactly 79 messages **shall** be received.
[UAR100cx] Step 6, 199.62ms: Exactly 79 messages **shall** be received.
[UAR100cy] Step 6, 200.02ms: Exactly 79 messages **shall** be received.
[UAR100cz] Step 6, 200.42ms: Exactly 79 messages **shall** be received.
[UAR100ca] Step 6, 200.82ms: Exactly 79 messages **shall** be received.
[UAR100cb] Step 6, 201.22ms: Exactly 79 messages **shall** be received.
[UAR100dc] Step 6, 201.62ms: Exactly 79 messages **shall** be received.
[UAR100dd] Step 6, 202.02ms: Exactly 79 messages **shall** be received.
[UAR100de] Step 6, 202.42ms: Exactly 79 messages **shall** be received.
[UAR100df] Step 6, 202.82ms: Exactly 79 messages **shall** be received.
[UAR100dg] Step 6, 203.22ms: Exactly 79 messages **shall** be received.
[UAR100dh] Step 6, 203.62ms: Exactly 79 messages **shall** be received.
[UAR100di] Step 6, 204.02ms: Exactly 79 messages **shall** be received.
[UAR100dj] Step 6, 204.42ms: Exactly 79 messages **shall** be received.
[UAR100dk] Step 6, 204.82ms: Exactly 79 messages **shall** be received.
[UAR100dl] Step 6, 205.22ms: Exactly 79 messages **shall** be received.
[UAR100dm] Step 6, 205.62ms: Exactly 79 messages **shall** be received.
[UAR100dn] Step 6, 206.02ms: Exactly 79 messages **shall** be received.
[UAR100do] Step 6, 206.42ms: Exactly 79 messages **shall** be received.
[UAR100dp] Step 6, 206.82ms: Exactly 79 messages **shall** be received.
[UAR100dq] Step 6, 207.22ms: Exactly 79 messages **shall** be received.
[UAR100dr] Step 6, 207.58ms: Exactly 79 messages **shall** be received.
[UAR100ds] Step 7: Exactly 100 messages **shall** be received.

Reference: HRD R00172010, R00172020, R00173110, R00173120, R00173130

5.17.2 [UAR105] UAT Rx Switching Diversity | Fast

Test Method: Select the indicated antenna using the test mode interface. Input at least 100 Long ADS-B messages at −70dBm into the OTHER antenna port.

Acceptance: [UAR105a] *Top Antenna*: No more than 10% of messages **shall** be received.

[UAR105b] *Bottom Antenna*: No more than 10% of messages **shall** be received.

Reference: Derived

5.17.3 [UAR106] UAT Rx Switching Interval | Fast

Test Method: Synchronously input 100 messages into the Top Antenna and Bottom Antenna at −30dB, with differing contents for each antenna. Start inputting the messages 25ms before the PPS epoch, and space them 500µs apart. Ensure that the selected antenna changes within ±2ms of the PPS epoch.

Acceptance: [UAR106a] At least 98 messages **shall** be received.

Reference: Derived

5.17.4 [UAR110] UAT Rx Long Message | Full

Test Method: Perform the test described in DO-282B §2.4.8.2.1.1.

Acceptance: [UAR110a] Step 2: The RF signal level **shall** be less than −96dBm.

[UAR110b] Step 4: The RF signal level **shall** be less than −96dBm.

Reference: HRD R00172030, R00172040

5.17.5 [UAR115] UAT Rx Long Message | Fast

Test Method: Perform the test described in DO-282B §2.4.8.2.1.1. In steps 2 and 4, the input power level should be tested at −96dBm only.

Acceptance: [UAR115a] Step 2: At least 90% of the messages **shall** be received.

[UAR115b] Step 4: At least 90% of the messages **shall** be received.

Reference: HRD R00172030, R00172040

5.17.6 [UAR120] UAT Rx Basic Message | Full

Test Method: Perform the test described in DO-282B §2.4.8.2.1.2.

Acceptance: [UAR120a] Step 2: The RF signal level **shall** be less than −97dBm.

[UAR120b] Step 4: The RF signal level **shall** be less than −97dBm.

Reference: HRD R00172050, R00172060

5.17.7 [UAR125] UAT Rx Basic Message | Fast

Test Method: Perform the test described in DO-282B §2.4.8.2.1.2. In steps 2 and 4, the input power level should be tested at −97dBm only.

Acceptance: [UAR125a] Step 2: At least 90% of the messages **shall** be received.

[UAR125b] Step 4: At least 90% of the messages **shall** be received.

Reference: HRD R00172050, R00172060

5.17.8 [UAR130] UAT Rx Uplink Message | Full

Test Method: Perform the test described in DO-282B §2.4.8.2.1.3.

Acceptance: [UAR130a] Step 2: The RF signal level **shall** be less than −94dBm.

[UAR130b] Step 4: The RF signal level **shall** be less than −94dBm.

Reference: HRD R00172070, R00172080

5.17.9 [UAR135] UAT Rx Uplink Message | Fast

Test Method: Perform the test described in DO-282B §2.4.8.2.1.3. In steps 2 and 4, the input power level should be tested at −94dBm only.

Acceptance: [UAR135a] Step 2: At least 90% of the messages **shall** be received.

[UAR135b] Step 4: At least 90% of the messages **shall** be received.

Reference: HRD R00172070, R00172080

5.17.10 [UAR140] UAT Rx Dynamic Range | Full

Test Method: Perform the test described in DO-282B §2.4.8.2.2.

Acceptance:
- [UAR140a] Step 2: The RF signal level “M” shall be less than −93dBm.
- [UAR140b] Step 3, M+10dBm: At least 99% of the messages **shall** be received.
- [UAR140c] Step 3, M+20dBm: At least 99% of the messages **shall** be received.
- [UAR140d] Step 3, M+30dBm: At least 99% of the messages **shall** be received.
- [UAR140e] Step 3, M+40dBm: At least 99% of the messages **shall** be received.
- [UAR140f] Step 3, M+50dBm: At least 99% of the messages **shall** be received.
- [UAR140g] Step 3, M+60dBm: At least 99% of the messages **shall** be received.
- [UAR140h] Step 3, M+70dBm: At least 99% of the messages **shall** be received.
- [UAR140i] Step 3, M+80dBm: At least 99% of the messages **shall** be received.
- [UAR140j] Step 3, −3dBm: At least 99% of the messages **shall** be received.

Reference: HRD R00172090

5.17.11 [UAR145] UAT Rx Dynamic Range | Fast

Test Method: Perform the test described in DO-282B §2.4.8.2.2, except for step 2. In step 3, only check the indicated power levels.

Acceptance:
- [UAR145a] Step 3, −93dBm: At least 99% of the messages **shall** be received.
- [UAR145f] Step 3, −48dBm: At least 99% of the messages **shall** be received.
- [UAR145j] Step 3, −3dBm: At least 99% of the messages **shall** be received.

Reference: HRD R00172090

5.17.12 [UAR150] UAT Rx Receiver Selectivity

Test Method: Perform the test described in DO-282B §2.4.8.2.3.

Acceptance:
- [UAR150a] Step 5, −1.0MHz: At least 90% of the messages **shall** be received.
- [UAR150b] Step 5, +1.0MHz: At least 90% of the messages **shall** be received.
- [UAR150c] Step 5, −2.0MHz: At least 90% of the messages **shall** be received.
- [UAR150d] Step 5, +2.0MHz: At least 90% of the messages **shall** be received.
- [UAR150e] Step 5, −10MHz: At least 90% of the messages **shall** be received.
- [UAR150f] Step 5, +10MHz: At least 90% of the messages **shall** be received.

Reference: HRD R00172100

5.17.13 [UAR160] UAT Rx Pulsed Interference

Test Method: Perform the test described in DO-282B §2.4.8.2.4.

Acceptance:

[UAR160aa] Step 5, 980MHz: At least 99% of the messages **shall** be received.

[UAR160ab] Step 5, 981MHz: At least 99% of the messages **shall** be received.

[UAR160ac] Step 5, 982MHz: At least 99% of the messages **shall** be received.

[UAR160ad] Step 5, 983MHz: At least 99% of the messages **shall** be received.

[UAR160ae] Step 5, 984MHz: At least 99% of the messages **shall** be received.

[UAR160af] Step 5, 985MHz: At least 99% of the messages **shall** be received.

[UAR160ag] Step 5, 990MHz: At least 99% of the messages **shall** be received.

[UAR160ah] Step 5, 1040MHz: At least 99% of the messages **shall** be received.

[UAR160ai] Step 5, 1090MHz: At least 99% of the messages **shall** be received.

[UAR160aj] Step 5, 1140MHz: At least 99% of the messages **shall** be received.

[UAR160ak] Step 5, 1190MHz: At least 99% of the messages **shall** be received.

[UAR160al] Step 5, 1215MHz: At least 99% of the messages **shall** be received.

[UAR160am] Step 6, 980MHz: At least 99% of the messages **shall** be received.

[UAR160an] Step 6, 981MHz: At least 99% of the messages **shall** be received.

[UAR160ao] Step 6, 982MHz: At least 99% of the messages **shall** be received.

[UAR160ap] Step 6, 983MHz: At least 99% of the messages **shall** be received.

[UAR160aq] Step 6, 984MHz: At least 99% of the messages **shall** be received.

[UAR160ar] Step 6, 985MHz: At least 99% of the messages **shall** be received.

[UAR160as] Step 6, 990MHz: At least 99% of the messages **shall** be received.

[UAR160at] Step 6, 1040MHz: At least 99% of the messages **shall** be received.

[UAR160au] Step 6, 1090MHz: At least 99% of the messages **shall** be received.

[UAR160av] Step 6, 1140MHz: At least 99% of the messages **shall** be received.

[UAR160aw] Step 6, 1190MHz: At least 99% of the messages **shall** be received.

[UAR160ax] Step 6, 1215MHz: At least 99% of the messages **shall** be received.

[UAR160ay] Step 7a, -90dBm: At least 90% of the messages **shall** be received.

[UAR160az] Step 7a, -89dBm: At least 90% of the messages **shall** be received.

[UAR160ba] Step 7a, -88dBm: At least 90% of the messages **shall** be received.

[UAR160bb] Step 7a, -83dBm: At least 90% of the messages **shall** be received.

[UAR160bc] Step 7a, -73dBm: At least 90% of the messages **shall** be received.

[UAR160bd] Step 7a, -63dBm: At least 90% of the messages **shall** be received.

[UAR160be] Step 7a, -53dBm: At least 90% of the messages **shall** be received.

[UAR160bf] Step 7a, -43dBm: At least 90% of the messages **shall** be received.

[UAR160bg] Step 7a, -33dBm: At least 90% of the messages **shall** be received.

[UAR160bh] Step 7a, -23dBm: At least 90% of the messages **shall** be received.

[UAR160bi] Step 7a, -13dBm: At least 90% of the messages **shall** be received.

[UAR160bj] Step 7b, -89dBm: At least 90% of the messages **shall** be received.

[UAR160bk] Step 7b, -88dBm: At least 90% of the messages **shall** be received.

[UAR160bl] Step 7b, -83dBm: At least 90% of the messages **shall** be received.

[UAR160bm] Step 7b, -73dBm: At least 90% of the messages **shall** be received.

[UAR160bn] Step 7b, -63dBm: At least 90% of the messages **shall** be received.

[UAR160bo] Step 7b, -53dBm: At least 90% of the messages **shall** be received.

[UAR160bp] Step 7b, -43dBm: At least 90% of the messages **shall** be received.

[UAR160bq] Step 7b, -33dBm: At least 90% of the messages **shall** be received.

[UAR160br] Step 7b, -23dBm: At least 90% of the messages **shall** be received.

[UAR160bs] Step 7b, -13dBm: At least 90% of the messages **shall** be received.

[UAR160bt] Step 9: At least 90% of the messages **shall** be received.

Reference: HRD R00172110, R00172120, R00172130, R00172140, R00174020, R00174030, R00174040

5.17.14 [UAR170] UAT Rx Overlapping Messages

Test Method: Perform the test described in DO-282B §2.4.8.2.5.

Acceptance: [UAR170a] Step 1: At least 90% of the message 2 **shall** be received.

[UAR170b] Step 2a: At least 90% of the message 2 **shall** be received.

[UAR170c] Step 2b: At least 90% of the message 1 **shall** be received.

Reference: HRD R00172150

5.17.15 [UAR180] UAT Rx Trigger Processing Rate

Test Method: Perform the test described in DO-282B §2.4.8.2.7.

Acceptance: [UAR180a] At least 400 messages/s with address 0x000001 **shall** be received.

[UAR180b] At least 300 messages/s with address 0x000002 **shall** be received.

Reference: HRD R00172180

5.17.16 [UAR190] UAT Rx Capacity for Reception

Test Method: Perform the test described in DO-282B §2.4.10.2.

Acceptance: [UAR190a] Step 3: All messages **shall** be received with the intended payload.

Reference: HRD R00173330, R00173340

5.17.17 [UAR210] UAT Rx Self Test | Full

Test Method: Perform at least 100 UAT receiver self-tests, and observe the spectral output.

Acceptance: [UAR210a] The total output power at the antenna port **shall not** exceed −40dBm, integrated across 6.5MHz of bandwidth.

[UAT215b] Each UAT self-test **shall** be successfully completed.

Reference: HRD R00161060, R00171120, R00173320

5.17.18 [UAR215] UAT Rx Self Test | Fast

Test Method: Command the appliance to perform a UAT self-test.

Acceptance: [UAT215a] The UAT self-test **shall** be successfully completed.

Reference: HRD R00161060, R00171120

5.18 1090 RX

5.18.1 [EXS100] 1090 In Band Acceptance | Full

Test Method: Perform the test described in DO-260B §2.4.4.3.1.1.1.

Acceptance: [EXS100a] Step 2: The measured MTL **shall** be less than −82dBm.

Reference: HRD R00181090, R00182010

5.18.2 [EXS105] 1090 In-Band Acceptance | Fast

Test Method: Perform the test described in DO-260B §2.4.4.3.1.1.1. In step 2, set the initial input power level at −79dBm. In step 3, test at 1089, 1090 and 1091MHz.

Acceptance: [EXS105a] The measured MTL **shall** be less than −82dBm.

Reference: HRD R00181090, R00182010

5.18.3 [EXS110] 1090 Dynamic Range | Full

Test Method: Perform the test described in DO-260B §2.4.4.3.1.1.2, excepting Step 4.

Acceptance: [EXS110a] At least 99% of the messages **shall** be received.

Reference: HRD R00181090, R00182020

5.18.4 [EXS115] 1090 Dynamic Range | Fast

Test Method: Perform the test described in DO-260B §2.4.4.3.1.1.2, excepting Step 4. In step 3, test at −79dBm -43dBm, and 0dBm (instead of increasing in 10dB increments).

Acceptance: [EXS115a] At least 99% of the messages **shall** be received.

Reference: HRD R00181090, R00182020

5.18.5 [EXS120] 1090 Re-Trigger Capability | Full

Test Method: Perform the test described in DO-260B §2.4.4.3.1.2.

Acceptance: [EXS120a] At least 49% of the messages **shall** be received.

Reference: HRD R00181090, R00183010

5.18.6 [EXS125] 1090 Re-Trigger Capability | Fast

Test Method: Input a valid 1090 message at −24dBm. Read the perceived signal level using the test mode interface. Repeat with a valid 1090 message at −16dBm. Compute the difference between the two perceived signal levels, in counts. Read the 1090 ADC calibration value, and multiply by 0.40 to compute the retriggering threshold

Acceptance: [EXS125a] The difference shall be greater than the retriggering threshold.

Reference: HRD R00181090, R00183010

5.18.7 [EXS126] 1090 ADC Calibration

Test Method: Read the 1090 ADC calibration value using the test mode interface.

Acceptance: [EXS126a] The value shall be between 86 and 108.

Reference: HRD R00182140

5.18.8 [EXS130] 1090 Out-of-Band Rejection | Full

Test Method: Perform the test described in DO-260B §2.4.4.3.2.

Acceptance:
- [EXS130a] Input B: At least 90% of the messages **shall** be received.
- [EXS130b] Input C: At least 90% of the messages **shall** be received.
- [EXS130c] Input D: At least 90% of the messages **shall** be received.
- [EXS130d] Input E: At least 90% of the messages **shall** be received.
- [EXS130e] Input F: At least 90% of the messages **shall** be received.
- [EXS130f] Input G: At least 90% of the messages **shall** be received.
- [EXS130g] Input H: At least 90% of the messages **shall** be received.
- [EXS130h] Input I: At least 90% of the messages **shall** be received.

Reference: HRD R00181090, R00182030

5.18.9 [EXS135] 1090 Out-of-Band Rejection | Fast

Test Method: Perform the test described in DO-260B §2.4.4.3.2. If the appliance is designated GDL88D, test the antenna port with the lowest loss.

Acceptance:
- [EXS135a] Input B: At least 90% of the messages **shall** be received.
- [EXS135d] Input E: At least 90% of the messages **shall** be received.
- [EXS135e] Input F: At least 90% of the messages **shall** be received.
- [EXS135h] Input I: At least 90% of the messages **shall** be received.

Reference: HRD R00181090, R00182030

5.18.10 [EXS140] 1090 Four Pulse Preamble | Full

Test Method: Perform the test described in DO-260B §2.4.4.4.2.2.

Acceptance:

[EXS140aa] Step 1: At least 90% of the messages **shall** be received.

[EXS140ab] Step 2: At least 90% of the messages **shall** be received.

[EXS140ac] Step 3: At least 90% of the messages **shall** be received.

[EXS140ad] Step 4: At least 90% of the messages **shall** be received.

[EXS140ae] Step 5: At least 90% of the messages **shall** be received.

[EXS140af] Step 6: At least 90% of the messages **shall** be received.

[EXS140ag] Step 7: At least 90% of the messages **shall** be received.

[EXS140ah] Step 8: At least 90% of the messages **shall** be received.

[EXS140ai] Step 9: At least 90% of the messages **shall** be received.

[EXS140aj] Step 10: At least 90% of the messages **shall** be received.

[EXS140ak] Step 11: At least 90% of the messages **shall** be received.

[EXS140al] Step 12: At least 90% of the messages **shall** be received.

[EXS140am] Step 13: At least 90% of the messages **shall** be received.

[EXS140an] Step 14: At least 90% of the messages **shall** be received.

[EXS140ao] Step 15: At least 90% of the messages **shall** be received.

[EXS140ap] Step 16: At least 90% of the messages **shall** be received.

[EXS140aq] Step 17: At most 10% of the messages **shall** be received.

[EXS140ar] Step 18: At most 10% of the messages **shall** be received.

[EXS140as] Step 19: At most 10% of the messages **shall** be received.

[EXS140at] Step 20: At most 10% of the messages **shall** be received.

[EXS140au] Step 21: At most 10% of the messages **shall** be received.

[EXS140av] Step 22: At most 10% of the messages **shall** be received.

[EXS140aw] Step 23: At most 10% of the messages **shall** be received.

[EXS140ax] Step 24: At most 10% of the messages **shall** be received.

[EXS140ay] Step 25: At most 10% of the messages **shall** be received.

[EXS140az] Step 26: At most 10% of the messages **shall** be received.

[EXS140ba] Step 27: At most 10% of the messages **shall** be received.

[EXS140bb] Step 28: At most 10% of the messages **shall** be received.

[EXS140bc] Step 29: At most 10% of the messages **shall** be received.

[EXS140bd] Step 30: At most 10% of the messages **shall** be received.

[EXS140be] Step 31: At most 10% of the messages **shall** be received.

[EXS140bf] Step 32: At most 10% of the messages **shall** be received.

[EXS140bg] Step 33: At most 10% of the messages **shall** be received.

[EXS140bh] Step 34: At most 10% of the messages **shall** be received.

[EXS140bi] Step 35: At most 10% of the messages **shall** be received.

[EXS140bj] Step 36: At most 10% of the messages **shall** be received.

[EXS140bk] Step 37: At most 10% of the messages **shall** be received.

[EXS140bl] Step 38: At most 10% of the messages **shall** be received.

[EXS140bm] Step 39: At most 10% of the messages **shall** be received.
[EXS140bn] Step 40: At most 10% of the messages **shall** be received.
[EXS140bo] Step 41: At most 10% of the messages **shall** be received.
[EXS140bp] Step 42: At most 10% of the messages **shall** be received.
[EXS140bq] Step 43: At most 10% of the messages **shall** be received.
[EXS140br] Step 44: At most 10% of the messages **shall** be received.
[EXS140bs] Step 45: At most 10% of the messages **shall** be received.
[EXS140bt] Step 46: At most 10% of the messages **shall** be received.
[EXS140bu] Step 47: At most 10% of the messages **shall** be received.
[EXS140bv] Step 48: At most 10% of the messages **shall** be received.
[EXS140bw] Step 49: At most 10% of the messages **shall** be received.
[EXS140bx] Step 50: At most 10% of the messages **shall** be received.
[EXS140by] Step 51: At most 10% of the messages **shall** be received.
[EXS140bz] Step 52: At most 10% of the messages **shall** be received.

Reference: HRD R00181050, R00181090, R00182040, R00182050, R00182060, R00183020, R00183030

5.18.11 [EXS145] 1090 Four Pulse Preamble | Fast

Test Method: Perform the test described in DO-260B §2.3.2.4.6.2.

Acceptance: [EXS145a] Step 1: At least 90% of the messages **shall** be received.
[EXS145b] Step 2: At least 90% of the messages **shall** be received.
[EXS145c] Step 3: At least 90% of the messages **shall** be received.
[EXS145d] Step 4: At least 90% of the messages **shall** be received.
[EXS145e] Step 5: At most 10% of the messages **shall** be received.
[EXS145f] Step 6: At most 10% of the messages **shall** be received.
[EXS145g] Step 7: At most 10% of the messages **shall** be received.
[EXS145h] Step 8: At most 10% of the messages **shall** be received.
[EXS145i] Step 5: At most 10% of the messages **shall** be received.
[EXS145j] Step 6: At most 10% of the messages **shall** be received.
[EXS145k] Step 7: At most 10% of the messages **shall** be received.
[EXS145l] Step 8: At most 10% of the messages **shall** be received.

Reference: HRD R00181050, R00181090, R00182040, R00182050, R00182060, R00183020, R00183030

5.18.12 [EXS160] 1090 Preamble Validation

Test Method: Perform the test described in DO-260B §2.4.4.4.2.3.

Acceptance: [EXS160a] Step 1: At most 10% of the messages **shall** be received.
[EXS160b] Step 2: At most 10% of the messages **shall** be received.
[EXS160c] Step 3: At most 10% of the messages **shall** be received.
[EXS160d] Step 4: At most 10% of the messages **shall** be received.
[EXS160e] Step 5: At most 10% of the messages **shall** be received.
[EXS160f] Step 6: At most 10% of the messages **shall** be received.
[EXS160g] Step 7: At most 10% of the messages **shall** be received.
[EXS160h] Step 8: At most 10% of the messages **shall** be received.
[EXS160i] Step 9: At most 10% of the messages **shall** be received.
[EXS160j] Step 10: At most 10% of the messages **shall** be received.
[EXS160k] Step 11: At least 90% of the messages **shall** be received.
[EXS150l] Step 12: At least 90% of the messages **shall** be received.

Reference: HRD R00181050, R00181090, R00183020, R00183030

5.18.13 [EXS170] Data Block Acceptance

Test Method: Perform the test described in DO-260B §2.4.4.3.4.7.3.

Acceptance: [EXS170a] Step 1: All ADS-B messages **shall** be correctly received.
[EXS170b] Step 2: All ADS-B messages **shall** be correctly received.
[EXS170c] Step 3: No ADS-B messages **shall** be received.

Reference: HRD R00181090, R00183120

5.18.14 [EXS180] 1090 Mode A/C Fruit Tests | Full

Test Method: Perform the test described in DO-260B §2.4.4.4.2.4.

Acceptance: [EXS180a] Step 2: At least 89% of the messages **shall** be received.
[EXS180b] Step 3: At least 64% of the messages **shall** be received.
[EXS180c] Step 4: At least 53% of the messages **shall** be received.

Reference: HRD R00181050, R00181090

5.18.15 [EXS185] 1090 Mode A/C Fruit Tests | Fast

Test Method: Perform the test described in DO-260B §2.3.2.4.8.1.

Acceptance: [EXS185a] Step 1: At least 53% of the messages **shall** be received.

Reference: HRD R00181050, R00181090

5.18.16 [EXS190] 1090 Mode S Fruit Tests | Full

Test Method: Perform the test described in DO-260B §2.4.4.4.2.5.

Acceptance: [EXS190a] Step 1: At least 95% of the messages **shall** be received.

[EXS190b] Step 2a (+0dB): At least 0% of the messages **shall** be received.

[EXS190c] Step 2b (+4dB): At least 56% of the messages **shall** be received.

[EXS190d] Step 2c (+8dB): At least 99% of the messages **shall** be received.

[EXS190e] Step 2d (+12dB): At least 99% of the messages **shall** be received.

Reference: HRD R00181050, R00181090

5.18.17 [EXS195] 1090 Mode S Fruit Tests | Fast

Test Method: Perform the test described in DO-260B §2.3.2.4.8.2.

Acceptance: [EXS195a] Step 2a (+0dBm): Any number of messages **shall** be received.

[EXS195b] Step 2b (+8dB): At least 99% of the messages **shall** be received.

Reference: HRD R00181050, R00181090

5.18.18 [EXS200] 1090 Re-Trigger Performance | Full

Test Method: Perform the test described in DO-260B §2.4.4.4.2.6.

Acceptance: [EXS200a] Step 1: At least 95% of the messages **shall** be received.

[EXS200b] Step 2a (+4dB): At least 12% of the messages **shall** be received.

[EXS200c] Step 2b (+8dB): At least 70% of the messages **shall** be received.

[EXS200d] Step 2c (+12dB): At least 91% of the messages **shall** be received.

[EXS200e] Step 3a (+4dB): At least 0% of the messages **shall** be received.

[EXS200f] Step 3b (+8dB): At least 49% of the messages **shall** be received.

[EXS200g] Step 3c (+12dB): At least 87% of the messages **shall** be received.

Reference: HRD R00181050, R00181090

5.18.19 [EXS205] 1090 Re-Trigger Performance | Fast

Test Method: Perform the test described in DO-260B §2.3.2.4.8.3.

Acceptance: [EXS205a] Step 2a (+4dB): At least 12% of the messages **shall** be received.

[EXS205b] Step 2b (+12dB): At least 91% of the messages **shall** be received.

Reference: HRD R00181050, R00181090

5.18.20 [EXS210] 1090 Self-Test | Full

Test Method: Perform the test described in DO-260B §2.4.11.4.

Acceptance: [EXS210a] Step 1: All of the messages **shall** be received.

[EXS210b] Step 2a: *Discrete Output 2* **shall** assert within 1.0s of failure.

[EXS210c] Step 2b: *Discrete Output 2* **shall** remain asserted as long as the failure continues to be induced.

[EXS210d] Step 3: *Discrete Output 2* **shall** de-assert within 2.0s after removing the induced failure.

[EXS210e] Step 4: Emissions at 1030MHz during the self test **shall** remain below −55dBm measured at both antenna ports.

Reference: HRD R00181080, R00183080

5.18.21 [EXS215] 1090 Self-Test | Fast

Test Method: Command the appliance to perform a 1090 self-test using the test mode interface.

Acceptance: [EXS215a] The 1090 self-test **shall** be successfully completed.

Reference: HRD R00181080, R00183080

5.18.22 [EXS240] 1090 Switching Loss

Test Method: With the alternate antenna initially selected and terminated with 50Ω to ground, input a continuous 1090MHz unmodulated signal at MTL+3dB into the target antenna. Using the test-mode interface, initiate an antenna switching sequence and measure the time between the assertion of the antenna switch line and the time that the 1090MHz signal level reaches the receiver MTL measured at the RF front end.

Acceptance: [EXS240a] With *Top Antenna* initially selected and *Bottom Antenna* as the target, the measured time **shall** be less than 3.5μs.

[EXS240b] With *Bottom Antenna* initially selected and *Top Antenna* as the target, the measured time **shall** be less than 3.5μs.

Reference: HRD R00182090

5.19 INTERROGATOR

5.19.1 [INT100] Interrogator Operation

Test Method: Command the appliance to initiate an interrogation using the test mode interface. Set the Interrogator receiver to "always active" using the test mode interface. Input a 0dBm transponder reply (arbitrary squawk code) to the *Bottom Antenna* port.

Acceptance: [INT100a] The power output at the *Bottom Antenna* port **shall** be −29 ± 2dBm.

[INT100b] The interrogator **shall** recognize the correct squawk code.

Reference: HRD R00191010

5.19.2 [INT110] Interrogator Output Power

Test Method: Command the appliance to initiate an interrogation using the test mode interface. Observe the signal at the *Bottom Antenna* port.

Acceptance: [INT110a] The maximum power of the interrogator **shall** be −29 ± 2dBm.

[INT110b] The maximum absolute difference between the maximum power of the first pulse and second pulses of the interrogation **shall** be 1dB.

[INT110c] The maximum power in the period before the interrogator becomes active **shall** be less than −55dBm.

[INT110d] The maximum power between the two interrogation pulses **shall** be less than −55dBm.

[INT110e] The maximum power in the period after the interrogator becomes inactive **shall** be less than −55dBm.

Reference: HRD R00192040, R00192050, R00192070

5.19.3 [INT120] Interrogator Output Timing

Test Method: Command the appliance to initiate an interrogation using the test mode interface. Observe the signal at the *Bottom Antenna* port.

Acceptance: [INT120a] The interrogator **shall** output 2 distinct pulses.

[INT120b] The length of the first pulse **shall** be 0.8 ± 0.1µs.

[INT120c] The length of the second pulse **shall** be 0.8 ± 0.1µs.

[INT120d] The time between the rising edge of the first pulse and the rising edge of the second pulse **shall** be 8.0 ± 0.2µs.

Reference: HRD R00192060

5.19.4 [INT130] Interrogator Output Frequency

Test Method: Command the appliance to initiate an interrogation using the test mode interface. Observe the signal at the *Bottom Antenna* port.

Acceptance: [INT130a] The transmission center frequency **shall** be 1030MHz ± 20kHz.

Reference: HRD R00192030

5.19.5 [INT140] Interrogator Input Antenna

Test Method: Command the appliance to initiate an interrogation using the test mode interface. Within 10.5 ± 0.5µs after the output power is greater than −35dBm at the *Bottom Antenna* port, input a −15dBm transponder reply (arbitrary squawk code) to the *Bottom Antenna* port. Command the appliance to initiate a second interrogation using the test mode interface. Within 10.5 ± 0.5µs after the output power is greater than −35dBm at the *Bottom Antenna* port, input a −15dBm transponder reply identical to the first to the *Top Antenna* port.

Acceptance: [INT140a] The interrogator **shall** recognize the correct squawk code from the first interrogation sequence.

[INT140b] The interrogator **shall not** recognize any squawk code from the second interrogation sequence.

Reference: HRD R00193040

5.19.6 [INT150] Interrogator Input Power

Test Method: Command the appliance to initiate an interrogation using the test mode interface three times. Each time, within 10.5 ± 0.5µs after the output power is greater than −35dBm at the *Bottom Antenna* port, input a transponder reply at the indicated power (arbitrary squawk code) to the *Bottom Antenna* port. After the second interrogation sequence, set the interrogator receive threshold to ignore replies below −20dBm.

Acceptance: [INT150a] +24dBm: The interrogator **shall** recognize the correct squawk code from the first interrogation sequence.

[INT150b] −30dBm: The interrogator **shall** recognize the correct squawk code from the second interrogation sequence.

[INT150c] −30dBm: The interrogator **shall not** recognize any squawk code from the third interrogation sequence.

Reference: HRD R00192110, R00193030

5.19.7 [INT160] Interrogator Retry

Test Method: Command the appliance to initiate 10 interrogations using the test mode interface. Within ±0.5µs of the indicated delay after the output power is first greater than −35dBm at the *Bottom Antenna* port, input a transponder reply at -5dBm (arbitrary squawk code) to the *Bottom Antenna* port.

Acceptance: [INT160a] 5.0µs after the first interrogation commences: The interrogator **shall not** recognize any squawk code, and **shall** initiate 9 subsequent interrogations within 5ms.

[INT160b] 9.3µs after the first interrogation commences: The interrogator **shall** recognize the correct squawk code, and **shall not** interrogate again.

[INT160c] 13.3µs after the first interrogation commences: The interrogator **shall** recognize the correct squawk code, and **shall not** interrogate again.

[INT160d] 5.0µs after the second interrogation commences: The interrogator **shall not** recognize any squawk code, and **shall** initiate 8 subsequent interrogations within 5ms.

[INT160e] 11.3µs after the third interrogation commences: The interrogator **shall** recognize the correct squawk code, and **shall not** interrogate again.

[INT160e] 11.3µs after the ninth interrogation commences: The interrogator **shall** recognize the correct squawk code, and **shall not** interrogate again.

Reference: HRD R00192080, R00192090, R00193010

6. PRODUCTION TEST TABLE

TEST	TEST NAME	NOTES	PRODUCTION			TSO	ENV	ENG
			HOT	COLD	FINAL			
[GEN100]	Appliance Serial Number				X		X	X
[GEN110]	Appliance Version Numbers				X		X	X
[GEN120]	Internal Temperature		X	X	X			X
[GEN130]	Assembly Code				X		X	X
[GEN140]	Hardware Revisions				X		X	X
[GEN150]	GPS Information				X		X	X
[GEN160]	Operating History		X	X	X		X	X
[GEN170]	Temperature Reset				X			X
[GEN180]	Clock Accuracy		X	X	X		X	X
[GEN210]	Processor RAM		X	X	X		X	X
[GEN230]	Configuration Module		X	X	X		X	X
[GEN240]	Global Reset Startup							X
[GEN250]	Watchdog Timer | Full							X
[GEN255]	Watchdog Timer | Fast				X		X	
[GEN260]	Watchdog Timer Input							X
[GEN270]	Watchdog Power Input							X
[GEN280]	Antenna Self-Test							X
[MEC100]	Appliance Weight							X
[MEC110]	Appliance Dimensions							X
[MEC120]	Remote Rack Width							X
[MEC130]	Modular Rack Width							X
[PWR100]	Aviation Power Range		X	X	X			X
[PWR110]	Power On Time							X
[PWR120]	Power Consumption		X	X	X			X
[PWR140]	Power Interrupt | Full							X
[PWR145]	Power Interrupt | Fast		X	X	X			X
[PWR150]	Internal Supply Voltages		X	X	X		X	X
[PWR160]	Internal Current Limit							X
[PWR170]	Battery Current	*WAAS Only*						X
[PWR180]	Battery Safety	*WAAS Only*						X
[PWR190]	Battery Charging	*WAAS Only*						X
[PWR200]	Power Supply Sync							X
[PWR210]	Remote Power Control | Full							X
[PWR215]	Remote Power Control | Fast		X	X	X			
[PWR220]	Power Fail Interrupt							X
[PWR230]	Fan Temp Thresholds							X
[PWR240]	Fan Output Control | Full							X
[PWR245]	Fan Output Control | Fast		X	X	X		X	
[PWR250]	Fan Output Power							X
[PWR260]	Fan Output Safety							X

TEST	TEST NAME	NOTES	PRODUCTION			TSO	ENV	ENG
			HOT	COLD	FINAL			
[PWR270]	GPS Backup Power				X			X
[PWR280]	GPS Antenna Bias				X			X
[PWR290]	RF Board Soft Start							X
[PWR300]	Fan Tach. Thresholds							X
[DSC100]	Discrete Input Configuration							X
[DSC110]	Discrete Input Active		X	X	X		X	X
[DSC120]	Discrete Input Inactive		X	X	X		X	X
[DSC130]	Discrete Input Threshold							X
[DSC140]	Discrete Input Default							X
[DSC150]	Discrete Input Safety							X
[DSC200]	Discrete Output Configuration							X
[DSC210]	Discrete Output Active		X	X	X		X	X
[DSC220]	Discrete Output Inactive		X	X	X		X	X
[DSC230]	Discrete Output Power | Full							X
[DSC235]	Discrete Output Power | Fast		X	X	X		X	X
[DSC240]	Discrete Output Interruption							X
[DSC250]	Discrete Output Timing							X
[DSC260]	Discrete Output Impedance							X
[DSC280]	Discrete Output Safety							X
[DSC300]	Suppressor Pulse | Full							X
[DSC305]	Suppressor Pulse | Fast		X	X	X		X	
[DSC310]	Suppressor Pulse Timing							X
[DSC315]	Suppressor Pulse Impedance							X
[DSC320]	Suppressor Pulse Default							X
[DSC330]	Suppressor Pulse Safety							X
[SER200]	232 Loopback		X	X	X		X	X
[SER205]	232 Transmit Open							X
[SER210]	232 Transmit Levels							X
[SER215]	232 Transmit Timing							X
[SER220]	232 Receive Open Circuit							X
[SER225]	232 Receive Termination							X
[SER230]	232 Transmit Current							X
[SER235]	232 Receive Threshold							X
[SER245]	232 Transmit Idle							X
[SER250]	232 Receive Capacitance							X
[SER255]	232 Port Safety							X
[SER300]	422 Loopback		X	X	X		X	X
[SER305]	422 Transmit Open							X
[SER310]	422 Transmit Levels							X
[SER315]	422 Transmit Timing							X
[SER320]	422 Transmit Impedance							X
[SER325]	422 Receive Threshold							X
[SER330]	422 Receive Termination							X

TEST	TEST NAME	NOTES	PRODUCTION			TSO	ENV	ENG
			HOT	COLD	FINAL			
[SER335]	422 Transmit Power Off							X
[SER340]	422 Transmit Open Circuit							X
[SER345]	422 Transmit Idle							X
[SER350]	422 Transmit Current							X
[SER360]	422 Port Safety							X
[SER100]	429 Loopback		X	X	X		X	X
[SER110]	429 Transmit Levels							X
[SER115]	429 Transmit Logic							X
[SER125]	429 Transmit High Speed							X
[SER130]	429 Transmit Low Speed							X
[SER135]	429 Transmit Idle							X
[SER145]	429 Transmit Impedance							X
[SER150]	429 Receive Open Circuit							X
[SER155]	429 Receive Termination							X
[SER160]	429 Receive High Speed							X
[SER165]	429 Receive Low Speed							X
[SER170]	429 Receive Capacitance							X
[SER175]	429 Receive Overdrive							X
[SER180]	429 Receive Safety							X
[SER185]	429 Transmit Safety							X
[ETH100]	Ethernet Loopback		X	X	X		X	X
[ETH110]	Ethernet Speed							X
[IIC100]	I2C Device Status		X	X	X		X	X
[USB100]	USB Connection				X			X
[AUD100]	Audio Output Test		X	X	X		X	X
[AUD110]	Audio Attenuation							X
[AUD120]	Audio Current Limit							X
[AUD130]	Audio Safety							X
[PPS100]	PPS Input Open Circuit							X
[PPS110]	PPS Differential Input | Full							X
[PPS115]	PPS Differential Input | Fast		X	X	X		X	
[PPS120]	PPS Differential Input Inactive							X
[PPS130]	PPS Single-Ended Input | Full							X
[PPS135]	PPS Single-Ended Input | Fast		X	X	X		X	
[PPS140]	PPS Single-Ended Input Inactive							X
[PPS150]	PPS Output Pulse							X
[PPS160]	PPS Output Timing		X	X	X		X	X
[PPS200]	PPS Current Limit							X
[PPS210]	PPS Port Safety							X
[UAT100]	UAT Tx Carrier Frequency		X	X	X	X	X	X
[UAT110]	UAT Tx Modulation Type					X	X	X
[UAT120]	UAT Tx Modulation Distortion		X	X	X	X	X	X
[UAT130]	UAT Tx Output Power | Full					X		X

TEST	TEST NAME	NOTES	PRODUCTION			TSO	ENV	ENG
			HOT	COLD	FINAL			
[UAT135]	UAT Tx Output Power | Fast		X	X	X		X	
[UAT150]	UAT Tx In-Band Spectrum		X	X	X	X	X	X
[UAT160]	UAT Tx Out-of-Band Emissions					X		X
[UAT170]	UAT Tx Message Cycle					X	X	X
[UAT190]	UAT Tx MSO Timing Tolerance					X	X	X
[UAT200]	UAT Tx Turnaround Time | Full					X		X
[UAT205]	UAT Tx Turnaround Time | Fast					X		X
[UAT220]	UAT Tx Antenna Safety					X		X
[UAR100]	UAT Rx Switching Diversity | Full	*GDL88D Only*				X		X
[UAR105]	UAT Rx Switching Diversity | Fast	*GDL88D Only*	X	X	X		X	
[UAR106]	UAT Rx Switching Interval | Fast	*GDL88D Only*					X	
[UAR110]	UAT Rx Long Message | Full					X		X
[UAR115]	UAT Rx Long Message | Fast		X	X	X		X	
[UAR120]	UAT Rx Basic Message | Full					X		X
[UAR125]	UAT Rx Basic Message | Fast		X	X	X		X	
[UAR130]	UAT Rx Uplink Message | Full					X		X
[UAR135]	UAT Rx Uplink Message | Fast		X	X	X		X	
[UAR140]	UAT Rx Dynamic Range | Full					X		X
[UAR145]	UAT Rx Dynamic Range | Fast		X	X	X		X	
[UAR150]	UAT Rx Receiver Selectivity		X	X	X	X	X	X
[UAR160]	UAT Rx Pulsed Interference					X		X
[UAR170]	UAT Rx Overlapping Messages					X		X
[UAR180]	UAT Rx Trigger Processing Rate					X		X
[UAR190]	UAT Rx Capacity for Reception					X		X
[UAR210]	UAT Tx/Rx Self-Test | Full					X		X
[UAR215]	UAT Tx/Rx Self-Test | Fast		X	X	X		X	X
[EXS100]	1090 In-Band Acceptance | Full					X		X
[EXS105]	1090 In-Band Acceptance | Fast		X	X	X		X	
[EXS110]	1090 Dynamic Range | Full					X		X
[EXS115]	1090 Dynamic Range | Fast		X	X	X		X	
[EXS120]	1090 Re-Trigger Capability | Full					X		X
[EXS125]	1090 Re-Trigger Capability | Fast		X	X	X		X	
[EXS126]	1090 ADC Calibration				X		X	
[EXS130]	1090 Out-of-Band Rejection | Full					X		X
[EXS135]	1090 Out-of-Band Rejection | Fast		X	X	X		X	
[EXS140]	1090 Four Pulse Preamble | Full					X		X
[EXS145]	1090 Four Pulse Preamble | Fast						X	
[EXS160]	1090 Preamble Validation					X		X
[EXS170]	1090 Data Block Acceptance					X	X	X
[EXS180]	1090 Mode A/C Fruit Tests | Full					X		X
[EXS185]	1090 Mode A/C Fruit Tests | Fast						X	
[EXS190]	1090 Mode S Fruit Tests | Full					X		X
[EXS195]	1090 Mode S Fruit Tests | Fast						X	

TEST	TEST NAME	NOTES	PRODUCTION			TSO	ENV	ENG
			HOT	COLD	FINAL			
[EXS200]	1090 Re-Trigger Perform… | Full					X		X
[EXS205]	1090 Re-Trigger Perform… | Fast						X	
[EXS210]	1090 Self Test | Full					X		X
[EXS215]	1090 Self Test | Fast		X	X	X		X	
[EXS240]	1090 Switching Loss	*GDL88D Only*				X		X
[INT100]	Interrogator Operation		X	X	X		X	X
[INT110]	Interrogator Output Power						X	X
[INT120]	Interrogator Output Timing						X	X
[INT130]	Interrogator Output Frequency		X	X	X		X	X
[INT140]	Interrogator Input Antenna	*GDL88D Only*						X
[INT150]	Interrogator Input Power							X
[INT160]	Interrogator Retry							X