CIRCUIT DESCRIPTION

4.1 Receiver

1) RF section
An incoming signal is fed to pre-selector, BPF-101/103, and amplified by Q101/Q102, and then fed to post-selector BPF-102/104. The outputs of the RF section(s) feed the balanced mixer, consisting of T101, T102, D107 and D108, which produces 48.5MHz by injection from the 1st local oscillator signal provided by the RX VCO.

2) IF & Audio Sections
The output signal from the balanced mixer is fed to the crystal filters XF101, and then amplified by Q103. This signal is fed to crystal filters XF102 A & B and amplified by Q113. The signal is fed to 2nd processor IC (IC106). The 2nd local crystal oscillator signal is fed to IC106 to produce the 2nd (Low IF) signal of 455 KHz. IC106 amplifies and detects the 455 Low IF 2nd local signal to produce an audio signal. Then, the audio signal is fed to the low-pass filter inclusive in IC107, and fed to audio processor IC (IC3) located on the Logic Unit. IC3 provides band-pass and de-emphasis functions and passes the processed audio to IC16, line amplifier and IC22, Audio PA. IC16 provides internal repeat audio and external "0 dBm" audio for interfacing external devices. IC22 provides audio to the speaker jack.

3) RX VCO Section
The oscillator circuit formed by Q301 and associated components produces the 1st local signal (Rx frequency minus 48.5MHz). The frequency of the oscillator is controlled by a signal input from the PLL, (see below) which is applied to varactors D303/304. The 1st local signal is amplified by buffer amplifier Q302, and again IC301 and Q303. The output signal is fed to the balanced mixer in the receiver RF section. A sample of the frequency is also sent to the PLL.

4) RX PLL Section
The PLL IC101 contains a pre-scaler and frequency dividers to divide both the VCO frequency and the local TCVXO, 12.0 MHz to a common reference frequency. These signals are compared by a phase detector to produce a VCO control signal. This control signal is fed to the charge pump, consisting of Q108, Q109 and Q110, and fed to the LPF IC103 and on to the VCO. The supply voltage of the charge pump is multiplied by IC102 (approx. 15V) to achieve greater C/N ratio. The frequency dividers are controlled by data from the Logic Unit to determine receiver operating frequency.

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4.2 Transmitter

1) TX VCO section
The oscillator circuit formed by Q301 and associated components produces the final carrier signal. The frequency of the oscillator is controlled by a signal input from the PLL, (see below) which is applied to varactors D303/304. The oscillator signal is amplified by buffer amplifier Q302, and again IC301 and Q303. The output signal is fed to the TX (driver) Unit for further amplification. A sample of the frequency is also sent to the PLL. The modulation is applied to varactors D301 and D302.

2) TX PLL section
The PLL IC101 contains a pre-scaler and frequency dividers to divide both the VCO frequency and the local TCVXO, 12.0 MHz to a common reference frequency (5 to 15 KHz.). These signalsare compared by a phase detector to produce a VCO control signal. This control signal is fed to

the charge pump, consisting of Q206, Q207 and Q208, and fed to the LPF IC207 and on to the VCO. The supply voltage of the charge pump is multiplied by IC208 (approx. 15V) to achieve greater C/N ratio. The frequency dividers are controlled by data from the Logic Unit to determine transmitter operating frequency

3) Modulator Section
The modulation signal is fed to both VCO and the reference oscillator (TCVXO). This permits a very flat modulation characteristic against low frequency (DC). This permits operation with digital signals such as Digital Coded Squelch and POCSAG Paging Terminals.

4) TX Unit (Driver) Section
The VCO signal is amplified by Q215 to the proper level to drive the PA Module.

5) PA Section
The signal from driver stage is fed to PM501 to achieve 30W output power. The signal is then fed to a balanced line to detect forward and reverse power, then on to the LPF to eliminate harmonics spurious frequencies. An APC (Automatic Power Control) circuit stabilizes the output power at the set level. The circuit also protects the PA from excess reverse power caused by mis-match of the antenna. An alarm circuit signals if output power drops below a preset level or when SWR exceeds a preset level. All parameters are adjustable.

4.3 Logic Unit

1) Microcomputer (CPU)
CPU, IC1, uPD78F0058, an 8-bit processor, has 60K flash memory and 2K RAM inside. This CPU controls all functions of KG506. A flash memory permits ON-BOARD-UP-GRADE when new software is released.

2) EE ROM section
IC7 is the 64kbit EEROM. This IC contains all channel parameters.

3) Audio processor section
An IC2 is for TX and IC3 is for RX audio processor. These IC's control all audio processing and encode/decode CTCSS tones commanded by the CPU. These IC's are also contain a 2400bps MODEM to enable use of MPT1327 trunking protocols by using external MPT control software.

4) LED display section (front panel of radio)
The LED's indicate each mode of operation of the KG506 as follows:
POWER, BUSY, TRANSMIT, ALARM, REPEATER.

5) Audio amplifier section
An IC22 provides 5 W audio power to drive 8 ohm external speaker.

4.4 Control Interface Connector

A 25 position D-sub connector for remote control is provided on the front panel of KG506.
The functions of each pin are as follows;
1 CH 0, 1 apply 1 to 6 bits of binary input to pins 1 thru 6 to select 64 channels,
2 CH 1, 2 Pin 1 is LSB.
3 CH 2, 4
4 CH 3, 8
5 CH 4, 16
6 CH 5, 32

7 GROUND Ground
8 RSSI Receive Signal Strength Indication, 0 to 5 V DC
9 DISC. OUT Discriminator audio output, low level
10 SQ. CONT. To external Squelch control, 10K pot to ground
11 BUSY Goes to 5V logic high when squelch is opened by signal
12 MUTE When pulled low, mutes RX and Repeat audio
13 MOD-1 Microphone modulation input
14 GROUND Ground
15 PTT Pull low to transmit
16 MOD-2 Digital modulation input, DC sensitive
17 SIMPLEX Provides logic output during simplex operation
18 ERROR Provides “flashing” high/low if error/alarm is present
19 DECODE Logic low upon decoding 5-tone or DTMF code
20 RX AUD-1 With pin 21, provides balanced “0 dBm” audio
21 RX AUD-2 With pin 20, provides balanced “0 dBm” audio
22 TX OUT Indicates error in PA, low power or high SWR
23 EXT. POW SW Connect to ground through external POWER switch
24 VOLUME To external volume control, 10 K pot to ground
25 +12V (nom) Switched 12 VDC to external accessories
CN1 Mini phone jack Balanced Speaker output both sides above ground.