RangeLAN2 6330 Micro Design-in Module
Product Specification

This Product Specification lists the technical specifications supported by Proxim to supply the 6330 Micro Design-in Module to OEMs. Terms and Conditions of sale to OEM customers are addressed in a Volume Purchase Agreement between the parties, which takes precedence over this document.

PRELIMINARY

I. PRODUCT STRUCTURE

1. The RangeLAN2 6330 Micro Design-in Module is composed of a board as specified, shipped with appropriate packaging and documentation, and software in object code form. The 6330 board has a MMCX antenna connector, which is used to attach an OEM-designed antenna to the card, and a 40-pin digital connector supplying an ISA electrical interface to the host device. This document uses the generic Product Number "6330" to refer to all variations of the product.

2. By separate agreement, OEMs may purchase:
   - antennas or portions of Proxim-designed antennas
   - software drivers licensed in source code form
   - OEM Developer Kits.

3. Antenna Connector: The 6330 has an MMCX antenna connector (see Outline Drawing), which allows OEMs to supply their own antenna for specific applications. All OEM products (i.e. all combinations of antenna, host, and 6330 Module) require separate FCC or other regulatory approvals.

   Proxim has designed several antennas, sub-assemblies of which may be useful to OEMs wishing to design their own antenna. Purchase or license of these sub-assemblies is not within the scope of this document.

4. A suffix to the Product Number specifies the hardware base of the product. The -02 products are suitable for FCC or ETSI certification; the -JP products are suitable for MKK Japan certification. The -05 product is physically the same as the -02 product but is configured to the U.S. frequency band prior to shipping.

5. Certifications with FCC and other regulatory agencies are the responsibility of the OEM partner.

6. Several software drivers are available from Proxim in object code form for the 6330. Some of these can be licensed in Source Code form. See **IX. SOFTWARE** section below.

II. GENERAL

1. Frequency Range:	2.4 - 2.4835 GHz for U.S., varies for other countries.
2. Radio Type:	Spread Spectrum, Frequency Hopping
3. Data Rate:	1.6 Mbps (main), 800 Kbps (backoff).
4. Modulation Type:	4FSK (main), BFSK (backoff). The modulation is automatically controlled by the 6330. It can also be configured by the OEM's software driver.
5. Compliance:	The 6330-02 and -05 products are FCC Parts 15.209 and 15.247 compliant. They are also compliant with ETSI ETS 300.328 and CE EMC-EEC 89/336. The 6330-JP product is MKK compliant under RDR STD 33.
6. Compatibility:	Fully interoperable with all RangeLAN2 products.
7. Roaming:	Supports roaming among all WLIF Access Points.

III. FREQUENCY GENERATION

1. Frequencies/Sequence:	79, 43, 23 depending on country configuration
2. Hopping Channels:	15

IV. TRANSMITTER

1. Output Power:	+20 dBm EIRP with 2 dBi gain antenna (nominal US, maximum ETSI/Japan)
2. Channel Spacing:	1 MHz
3. Output Spectrum:	±0.5 MHz: <-20 dBc typical ±4.0 MHz: <-50 dBc typical
4. Spurious Emissions:	Harmonics: <-50 dBm (ETSI & FCC)

<-20 dBm (Japan)

V. RECEIVER

1. Sensitivity:	at 1.6 Mbps: -77 dBm typical at 800 Kbps: -85 dBm typical
2. Maximum Input Power:	Performance range: <-5 dBm Survivability range: +5 dBm
3. Channel Rejection:	±3 MHz: -45 dBc typical ±10 MHz: -50 dBc typical

VI. MECHANICAL

1. RF Connector:	The RF Connector is an MMCX connector that is mounted on the edge of the 6330 card. A similar MMCX connector is available from Amphenol (Part Number 908-22100). Mating connector is Amphenol 908-43200 or 908-43300. This is a right angle cable connector. The MMCX connector tolerates multiple insertions (500 or more insertion cycles) and thus allows antennas to be occasionally removed for transport, storage, or replacement.
2. Digital connector:	The digital connector is a 40-pin vertical mate connector mounted near the edge of the card, AMP part number 177986-1.
3. Weight:	The weight of the 6330 Module is less than 20 grams.

VII. INTERFACE PIN DESCRIPTION

PIN	*INPUT/OUTPUT*	*DESCRIPTION*
GND	I	Ground

CD_LED	O	This signal is an optional output which when low indicates that the 6330 board is receiving a RangeLAN2 signal on the RF network. This signal can be used to drive an external LED (See Note #5).
AEN	I	The AEN signal is a standard ISA bus signal which signals when a DMA transfer is occurring on the bus. When this signal is high, the external computer is executing a DMA transfer. This is necessary to prevent unwanted IOReads and IOWrites during DMA reads and DMA writes, since during a DMA transfer, only the DACK, IOREAD#, and IOWRITE# signals must be active (See Note #2).
T/RX_LED	O	This signal is an optional output which when high, indicates that the 6330 board is in transmit mode. This signal can be used to drive an external LED (See Note #5).
RSSI	O	This is an analog Received Signal Strength Indication signal. Is should be left open if it is not being used. In most applications, this signal is digitized internally in the 6330 board, and the digital value is passed up via software to the host with the packet that the measurement corresponds to.
SD[15:0]	I/O	The SD[7:0] signals make up the low byte of the ISA compatible data bus. These signals are normally inputs to the 6330, but during IO READ operations from addresses within the 6330 address space, these signals become outputs. The SD[15:8] signals make up the high byte of the ISA compatible data bus. These signals are normally inputs to the 6330 board, but during IOREAD operations from addresses within the 6330 address space, these signals become outputs. These signals are strictly optional when the product is embedded into an ISA system. The 6330 card can be configured to operate in either 8 or 16 bit data modes. See Note #1.
CS#	I	This is an active low chip select input to the 6330. This signal is used in conjunction with the SA[2:0] address bus to decode addresses within the 6330. The 6330 requires an address space of 8 I/O registers, but these can be located on any 8 byte boundary through the use of the CS# input. For example, the CS# signal could be configured to go active on any address within the range of

		270H to 277H. This would result in a base address of 270H which corresponds to the case of SA[2:0] = 0H (see Note #2).
IOREAD#	I	This is the active, low, IOREAD# signal that is used on the PC/ISA bus to read data from an external I/O mapped register onto the data bus. The 6330 board will drive SD[15:0] while IOREAD# is being asserted (See Note #2).
IOWRITE#	I	This is the active low IOWRITE# signal that is used on the PC/ISA bus to write the data bus into an I/O mapped register. The rising edge of IOWRITE# is used to latch the value on the data bus into a register that is being addressed on the 6330 board (see Note #2).
INTR	O	This is the interrupt signal from the 6330 board. The signal is ISA bus compatible. It is active low and is an inverted pulse approximately 1ms in duration. It is used to interrupt the host computer when the 6330 board requires servicing (See Note #3).
IOCHRDY	O	The IOCHRDY signal is sometimes referred to as BUSRDY or WAIT. This signal is used to lengthen an IOREAD or IOWRITE signal when the 6330 board cannot respond quickly enough. This signal will not be held low for longer than 4µsec, and is an open drain output capable of sinking 24mA of current (see Note #4).
SA[2:0]	I	SA[2:0] are intended to be tied to the three low order address bits on the ISA bus. These address lines are used to decode between one of eight registers that are selected by the CS# input (See Note #2). The 6330 uses only 5 registers and all of them can be specified using an even address value (SA<0> = 0).
I/OCS16	O	This signal is used by the 6330 board to indicate that the I/O address which is being selected is a 16-bit address. If the host machine is set up to operate in 8 bit mode only, the 6330 can be configured for 8 bit operation, and this signal will not be used. This signal is an open drain output which is capable of sinking 24mA (See Note #4).
VDD	I	All VDD inputs to the 6330 digital connector are tied together on the board. These inputs supply all of the power for the Radio Transceiver and the RF Network Controller.

NOTE #1: BI-DIRECTIONAL INPUTS / OUTPUTS

SD[15:0]

Vil = 0 - 0.8V
Vih = 2.0V
Iin = ±10 µA Maximum
Iol = 4mA Minimum at Vol = 0.4V
Ioh = 2mA Minimum at Voh = VDD-0.5V
Cin = 10.0pF typical

NOTE: The data bus is not internally pulled-up in the 6330 card. It should be pulled-up (or down) externally to achieve specified power consumption figures.

NOTE #2: SIGNAL INPUTS

IOWRITE#, IOREAD#, SA[2:0], CS#, and AEN

Vil = 0 - 0.8V
Vih = 2.0V
Iin = ±10 µA Maximum
Cin = 10.0pF typical

NOTE #3: INTR OUTPUT

Iol = 24 mA Minimum at Vol = 0.4V (Interrupt asserted)
[NOTE: *INTR has a 10K Pullup Resistor to VDD on the 6300 (but not on the 6330) to bring the signal high when an interrupt is not being asserted.)]*

NOTE #4: IOCHRDY and IOIS16 OPEN DRAIN OUTPUTS

Iol = 24mA Minimum at Vol = 0.4V (Signals asserted)

NOTE #5: LED OUTPUTS

Iol = 4mA Minimum at Vol = 0.4V
Ioh = 2mA Maximum at Voh = VDD-0.5V
[NOTE: The 6330 has lines to drive two LEDs. Proxim typically drives the LEDs with a 1.8 Kohm resistor. This results in slightly more than 2mA of LED drive. For LEDs which are being driven by a high signal, the 6330 output will be approximately 0.5V below the power supply when the LED is turned on. For LEDs which are being driven by a low signal, the 6330's output will be approximately 0.2V.

[NOTE: On branded products, Proxim typically uses Yellow and Green LEDs. When the Yellow LED is lit, it means that the card is transmitting. When the Green LED is lit, it indicates that the PC Card detects another RangeLAN2 unit that is transmitting.]

VIII. ISA BUS TIMINGS

Read and Write Operations

This section describes the process for reading and writing to the OEM module. Both operations are performed as I/O Accesses by the host. Differences between 8-bit transfers and 16-bit transfers are discussed. These read and write operations are consistent with the ISA bus specification.

Host Write Operation to 6330 OEM Module

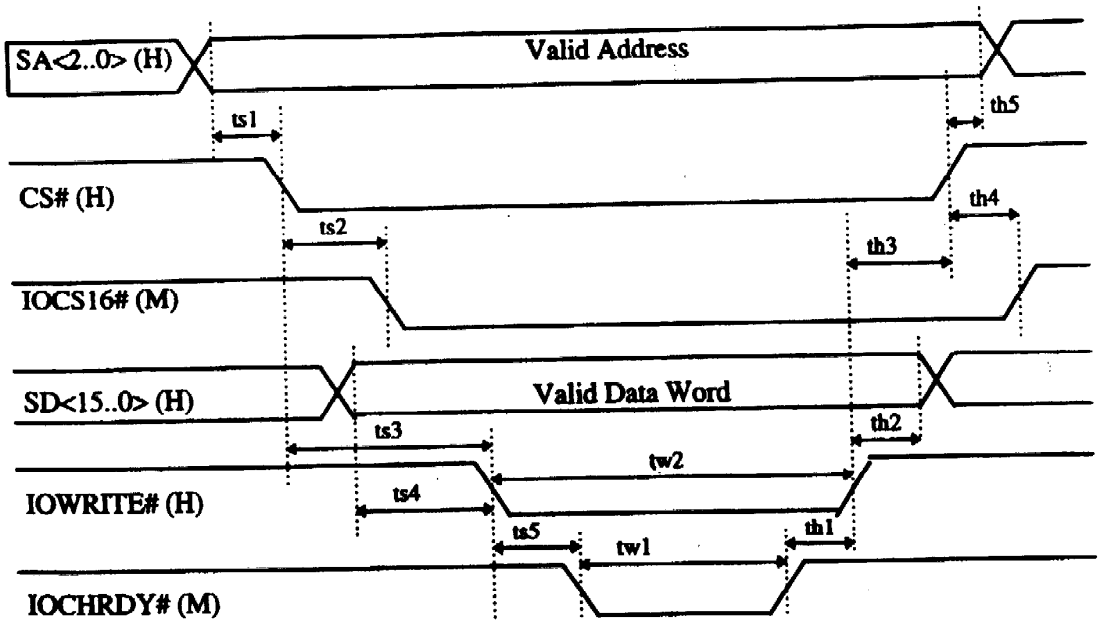
This operation occurs when the host needs to write either an 8-bit or 16-bit data word to one of the OEM module's 8 registers. The process is detailed below and shown in **Figure 1** for 16-bit transfers and **Figure 2** for 8-bit transfers. Signals controlled by the host are designated with a (H), while (M) denotes module signals.

The host applies the OEM I/O register select address bits SA<2..0> along with the Chip Select CS# to the OEM module. The module will respond by setting the IOCS16# if the address selected is a 16-bit address. If IOCS16# is not asserted then an 8-bit operation will occur. Timing of the IOCS16# signal is dependent upon both the address A<2..0> and the CS# being asserted.

The host places the data word on to the databus, either SD<15..0> for 16-bit data or SD<7..0> for 8-bit. The host also drives IOWRITE# active (to the LOW state) to set up a write to the module. The module will assert IOCHRDY# as necessary to tell the host to lengthen the IOWRITE# signal if the module can not complete the operation quickly enough. The length of the IOCHRDY# signal may vary from one write operation to another, but it will not exceed the maximum duration specified.

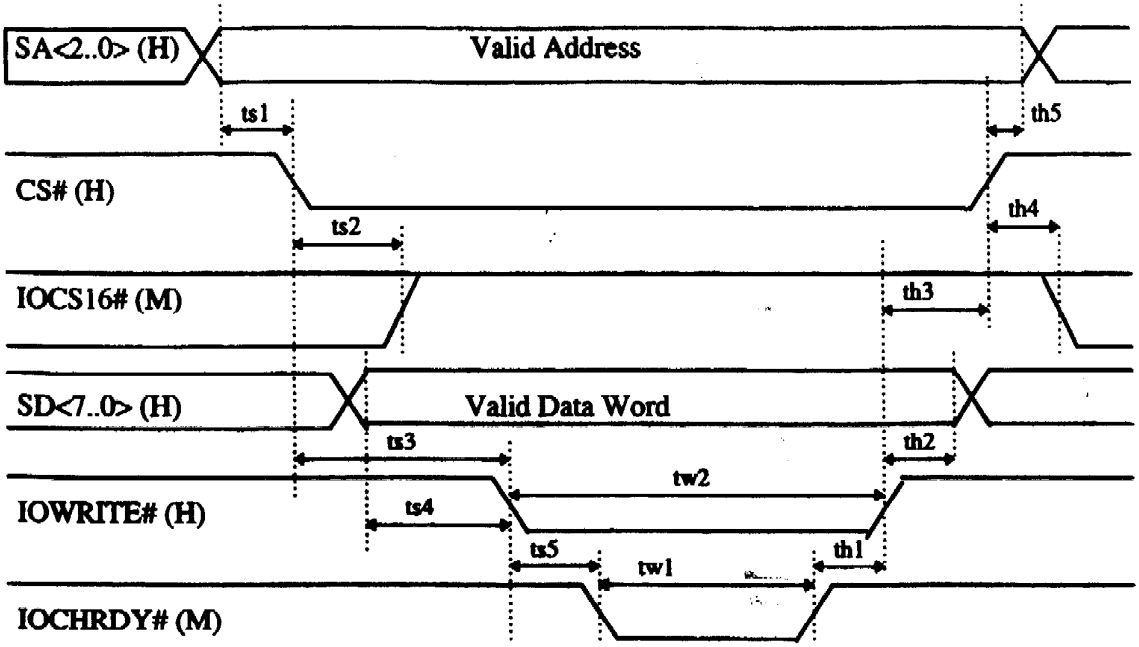
The host drives IOWRITE# high with the timing dependent upon IOCHRDY#. The data will be latched into the module's addressed I/O register on the rising edge of IOWRITE#. After meeting the required hold time, the host de-asserts the CS# signal. The module completes the operation by de-asserting IOCS16# for 16-bit operations.

Figure 1: 16-Bit Write Operation to Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOWRITE# Falling Edge	≥ 70
ts4	Setup, SD<15..0> to IOWRITE# Falling Edge	≥ 22
ts5	Setup, IOWRITE# to IOCHRDY# Falling Edge	≤ 35
tw1	Pulse Width, IOCHRDY# Asserted	≤ 4,000
tw2	Pulse Width, IOWRITE# Asserted	≥ 165
th1	Hold, IOCHRDY# to IOWRITE# Rising Edge	0
th2	Hold, SD<15..0> from IOWRITE# Rising Edge	≥ 30
th3	Hold, CS# from IOWRITE# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0

Figure 2: 8-Bit Write Operation to Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOWRITE# Falling Edge	≥ 70
ts4	Setup, SD<7..0> to IOWRITE# Falling Edge	≥ 22
ts5	Setup, IOWRITE# to IOCHRDY# Falling Edge	≤ 35
tw1	Pulse Width, IOCHRDY# Asserted	≤ 4,000
tw2	Pulse Width, IOWRITE# Asserted	≥ 165
th1	Hold, IOCHRDY# to IOWRITE# Rising Edge	≥ 0
th2	Hold, SD<7..0> from IOWRITE# Rising Edge	≥ 30
th3	Hold, CS# from IOWRITE# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0

Host Read Operation from OEM Module

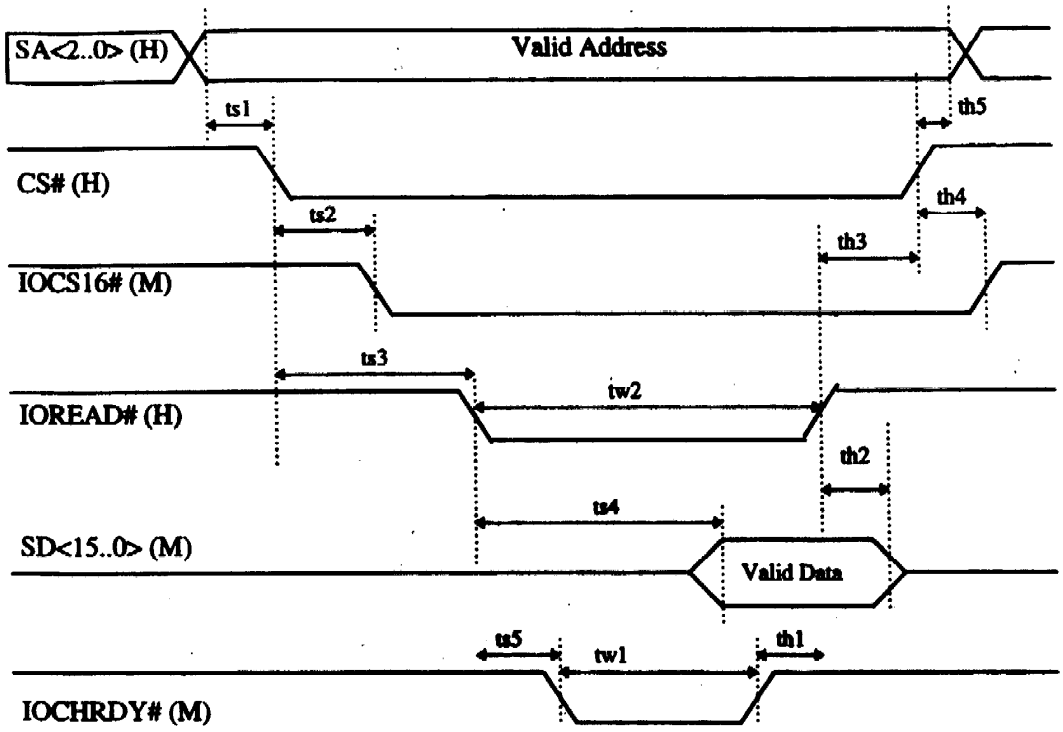
This operation occurs when the host needs to read either an 8-bit or 16-bit data word from one of the OEM module's 8 registers. The process is detailed below and shown in **Figure 3** for 16-bit transfers and **Figure 4** for 8-bit transfers. Signals controlled by the host are designated with a (H), while (M) denotes module signals.

The host applies the OEM I/O register select address bits SA<2..0> along with the Chip Select CS# to the OEM module. The module will respond by setting the IOCS16# if the address selected is a 16-bit address. If IOCS16# is not asserted then an 8-bit operation will occur. Timing of the IOCS16# signal is dependent upon both the address A<2..0> and the CS# being asserted.

The data bus, SD<15..0> for 16-bit data or SD<7..0> for 8-bit transfers is maintained in a tri-state condition by the host. The host drives IOREAD# active (to the LOW state) to set up a read from the module. The module will assert IOCHRDY# as necessary to tell the host to lengthen the IOWRITE# signal if the module can not complete the operation quickly enough. The length of the IOCHRDY# signal may vary from one write operation to another, but it will not exceed the maximum duration specified.

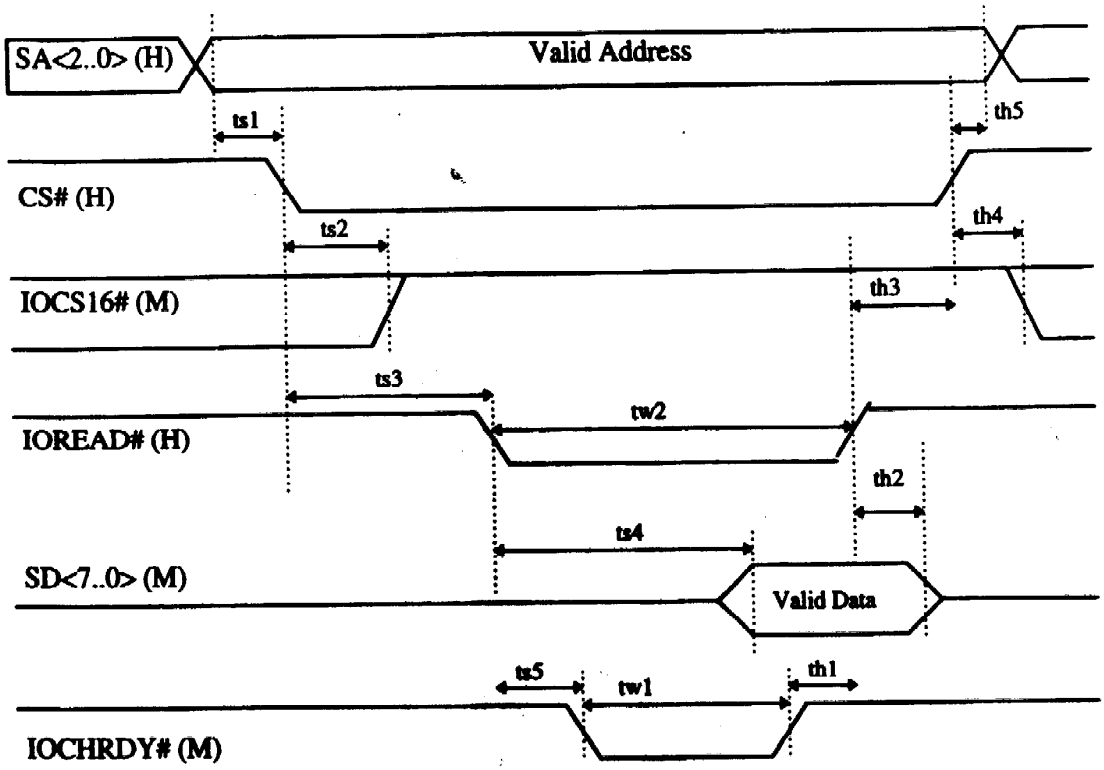
The OEM module accesses the addressed register and drives the databus with the data word from the register. The host then drives IOREAD# high with the timing dependent upon IOCHRDY#. After meeting the required hold time, the host de-asserts the CS# signal. The module completes the operation by de-asserting IOCS16# for 16-bit operations.

Figure 3: 16-Bit Read Operation from Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOREAD# Falling Edge	≥ 70
ts4	Setup, IOREAD# to Valid SD<15..0>	≤ 100
ts5	Setup, IOREAD# to IOCHRDY# Falling Edge	≤ 35
tw1	Pulse Width, IOCHRDY# Asserted	≤ 4,000
tw2	Pulse Width, IOREAD# Asserted	≥ 165
th1	Hold, IOCHRDY# to IOREAD# Rising Edge	≥ 0
th2	Hold, SD<15..0> from IOREAD# Rising Edge	≤ 30
th3	Hold, CS# from IOREAD# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0

Figure 4: 8-Bit Read Operation from Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≥ 90
ts3	Setup, CS# to IOREAD# Falling Edge	≥ 70
ts4	Setup, IOREAD# to Valid SD<7..0>	≤ 100
ts5	Setup, IOREAD# to IOCHRDY# Falling Edge	≤ 35
tw1	Pulse Width, IOCHRDY# Asserted	≤ 4,000
tw2	Pulse Width, IOREAD# Asserted	≥ 165
th1	Hold, IOCHRDY# to IOREAD# Rising Edge	≥ 0
th2	Hold, SD<7..0> from IOREAD# Rising Edge	≤ 30
th3	Hold, CS# from IOREAD# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0

VIII. PIN NUMBERS

Pin #	Lead
1	GND
2	RESERVED
3	VDD
4	RESERVED
5	VDD
6	RESERVED
7	CD_LED
8	RESERVED
9	AEN
10	TX/RX_LED
11	RSSI
12	SD14
13	SD7
14	SD13
15	SD6
16	SD12
17	SD5
18	SD11
19	SD4
20	GND
21	GND
22	SD3
23	CS#
24	SD15
25	IOREAD#
26	IOWRITE#
27	INTR
28	IOCHRDY
29	SA2
30	SA1
31	SA0
32	SD0
33	SD8
34	SD1
35	SD9
36	SD2
37	SD10
38	I/OIS16
39	VDD
40	GND

IX. SOFTWARE / NETWORKING

1. Supports peer-peer and client-server communications.
2. Proxim-supplied drivers can be configured to support IEEE 802.3, 802.2, and Ethernet frame formats.
3. Proxim-supplied drivers ODI v2.0, NDIS 2.01, 3.0, and 3.1 interfaces support most NetWare, TCP/IP, and Microsoft networking implementations according to the table below. Drivers are available from Proxim in object code form, or may be licensed from Proxim in source code form.
4. The C-LLD is Proxim's "C" source code version of the Low-Level Driver code (C_LLD). It is a set of functions that enables faster development of radio-frequency applications by OEMs integrating Proxim's RangeLAN2 products into platforms not supported by the drivers above. The C_LLD enables all the features of Proxim's sophisticated RangeLAN2 implementation, including transparent roaming, advanced power management, and automatic fragmentation. It is licensed in "C" source code that can be ported to many environments.

Typically, Proxim drivers are used in the following environments:

DOS & AT-bus compatible systems	ODI Driver	NDIS v2.0 Driver	NDIS v3.0 Driver	NDIS v3.1 Driver
Windows for Workgroups		X		
Windows 95				X
Windows-NT				X
Novell NetWare 3.1x	X			
Novell NetWare 4.x	X			
Novell Personal NetWare	X			
FTP PC/TCP 4.0		X	X	
NetManage Chameleon		X	X	

Non-DOS or Non-AT Bus compatible	C_LLD source code, ported by the OEM to the target platform

X. POWER

1. Input Voltage: 4.75V - 5.25V
2. Ripple: < 100 mV peak-peak
3. Input Current: See modes below.

- RX: 150 mA typical when receiver is active. Receiver is active when the unit is not transmitting and not in sleep or doze modes.

- TX: 300 mA typical, 350 mA absolute maximum when actively transmitting. Transmitter duty cycle is dependent on traffic load.

- Doze: 5 mA typical (average value). The 6330 automatically enters the Doze state when there has been no traffic for a configurable time period (driver default is 30 seconds). In this mode the PC Card minimizes power usage and remains synchronized to the master. It can therefore receive directed messages from the master or transmit packets to the master with minimal start-up or synchronization latency.

- Sleep: <2 mA typical. This state is entered when communication is lost with either the Master or the host and a configurable time period expires. In this state the 6330 can neither send nor transmit frames, but is awakened if an interrupt is sent to the card.

XI. ENVIRONMENTAL

1. Temperature Range: Operation: -20°C to +60°C
   Storage: -50 °C to +85°C
2. Humidity: 10% to 90%
3. Vibration: 5 to 200 Hz, 1.0G constant level,
   all directions (unpackaged, non-operational)
4. Shock: 30 G, 11ms, half sine (unpackaged, non-operational)
5. MTBF: Calculated at > 100,000 hours

XII. WARRANTY

Proxim warrants the 6330-series Products to be free of defects in materials and workmanship for a period of One Year from date of purchase. Proxim will either replace in kind or repair the product, at Proxim's discretion.

XIII. LABELING AND PACKAGING

Proxim will apply one label to each unit which will include the Proxim Product Number and Proxim Serial Number (barcoded together in 3 of 9 format), the datecode representing the date of manufacture or shipment, and an optional OEM code (up to nine digits). Proxim also supplies a label indicating the hardware base (Japan or ETSI/FCC) and the country code setting.

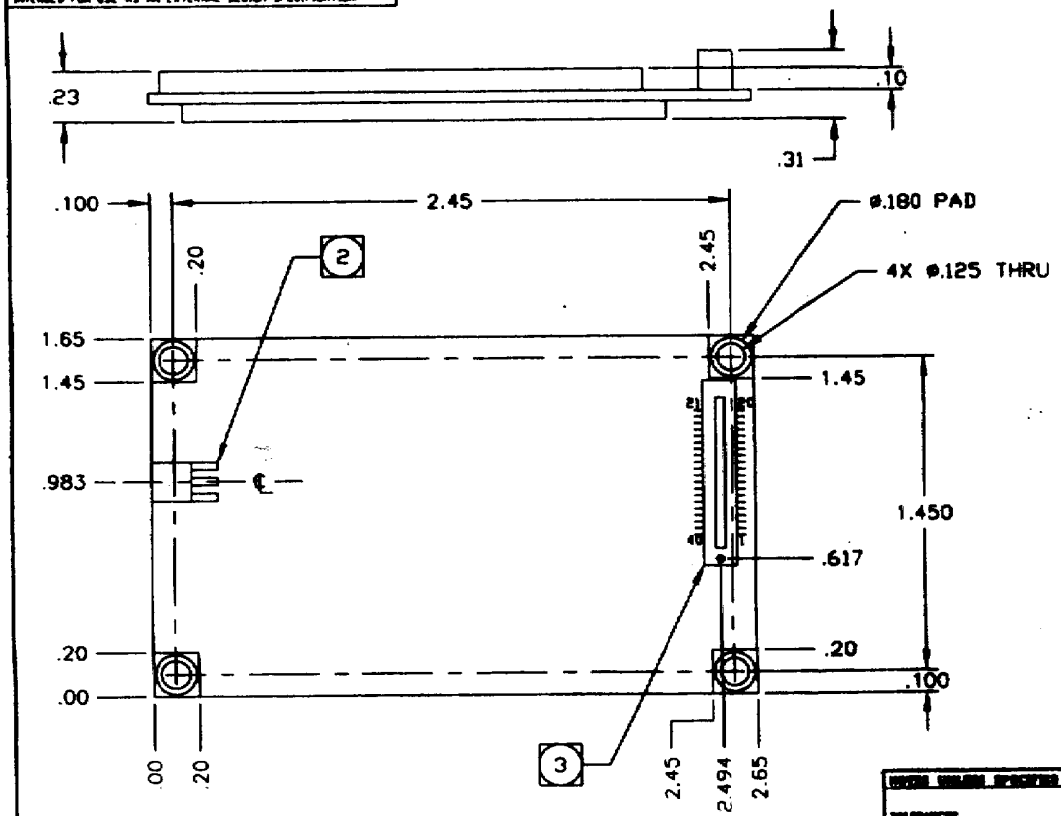
Upon written customer request, Proxim is able to apply a 2 inch by 4 inch label on the outside of each shipping carton which can include any or all of the customer's Part Number, the Quantity of units in the carton, and a barcode in 3 of 9 format of the customer's Part Number, in a mutually-agreeable format.

The product will be shipped egg-crated in bulk packaging. All shipping containers meet ITSA-1A specification for shipping US domestic and ISTA-2A for shipping internationally.

XIV. REFERENCES

Outline Drawing:	7370.0012
Design Guide:	7360.0082
Product Serial Number label:	2460.0530 (label specification)

REVISION					
LTR	ECO	DATE		BY	APPR
01	--	--	INITIAL RELEASE	WF	
02	--	9/27/96	REVISED PER 8000.0093 PCB LAYOUT	WF	
03	P1150	2-26-97	INITIAL RELEASE	BB	BB



NOTE: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: FR-4 OR EQUIVALENT EPOXY RESIN, 1/2 OZ COPPER CLAD .048±.005 THICK.
2. 82-MMCX, JACK, EDGE M.T. TO BE FLUSH WITH PCB EDGE ±.005. THIS APPLIES TO 0.983 LOCATION DIMENSION.
3. AMP #177986-1, 40-PIN CONNECTOR .8MM PITCH.

PRELIMINARY

UNLESS OTHERWISE SPECIFIED
TOLERANCES
.XX+/- .01 ANGULAR
.XXX+/- .005 +/-
BREAK ALL SHARP EDGES APPROX. .010
MACH. SURFACES
DIMENSIONS APPLY AFTER PLATING

DRAWN	Wm FOSTER	9/27/96
DESIGN	A. N. YAZAR	9/27/96
MATERIAL	1	
FINISH		
CHECKED AND APPROVED		

proxim

TITLE: OUTLINE, PCA, BOARD, M-ISA

SIZE	DWG NO.	REV.
B	7370.0012	03
SCALE 2:1	FILE NAME 73700012	SHEET 1 OF 1