6. 6307 MINI-ISA DESIGN-IN CARD

The RangeLAN2 Mini-ISA OEM Module is an integrated hardware/software package that allows developers to easily incorporate sophisticated wireless LAN networking capabilities into their products. It is especially well suited for integration into portable computer platforms for mobile data applications.

The RangeLAN2 Mini-ISA OEM Module includes a 2.4 GHz frequency hopping spread spectrum radio and network controller in a compact single-piece package optimized for mobility, performance, and range. It offers sophisticated wireless networking features, such as roaming, power management and synchronization. It supports industry standard interfaces to assure quick and inexpensive integration, and provides interoperable communications with all RangeLAN2 and Wireless LAN Interoperability Forum devices.

6.1 Introduction

This section details the specific issues related to the Mini-ISA OEM modules. There are two variations of the Mini-ISA OEM module, each of which provides a unique set of interface connectors. Other than the interface connectors, the two modules share common specifications. The 6302 OEM module utilizes an AMP connector for the 50-pin digital interface, while the 6303 utilizes a vertical Berg connector. The different connectors provide a choice in module installation, as discussed in Section 6.6.2.

6.2 Data Sheets

Included at the end of Section 6 are the data sheets for the Mini-ISA OEM modules.

6.3 Interface Description

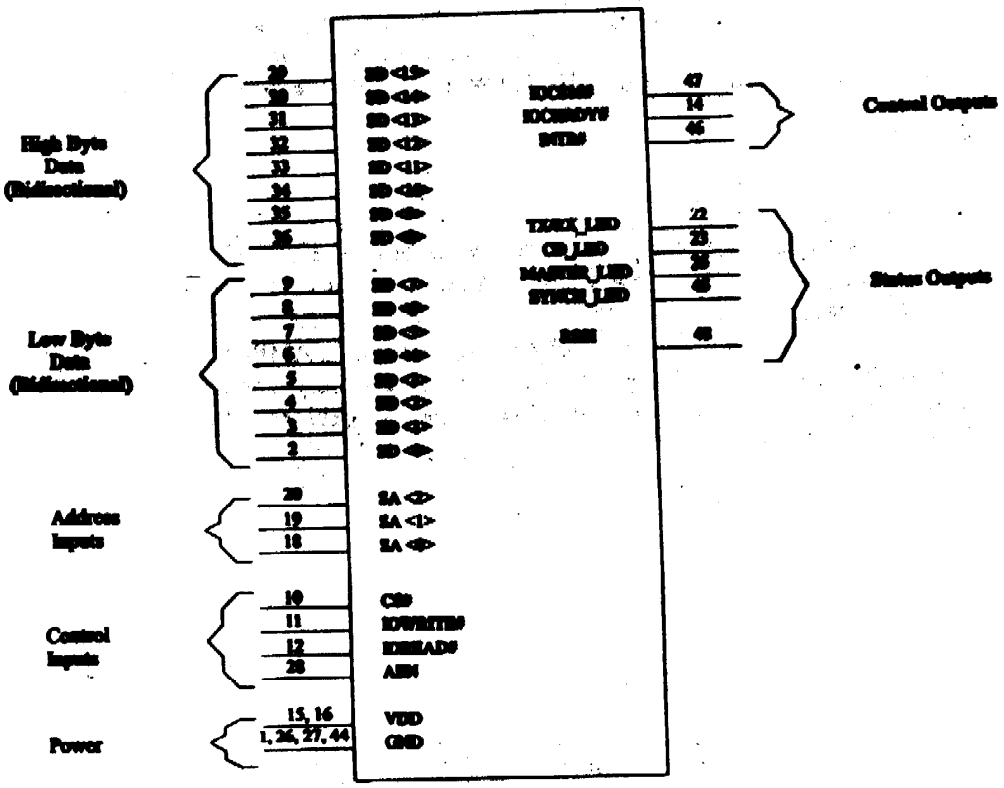
The Mini ISA OEM Module provides a 50 pin connector to the host for passing power, control, and data signals to the module, as shown in Figure 6-1. The module has been designed to interface to the host as an PC/ISA memory mapped I/O device. The module requires a minimal set of signals to operate, including data bus, chip select, address bus, and read / write strobes. Section 6.3.1 details the inputs and outputs for the module. The module defaults to a 16-bit data bus, but will also operate as an 8-bit device with 8-bit hosts, as discussed in Section 6.4.

The chip select signal, CS#, is used to decode addresses destined for the OEM module. The module requires an address space of 8 I/O registers, that can be located on any 8 byte boundary decoded with the CS# signal. The 3-bit address bus is used to identify the specific I/O register. The Mini-ISA uses only 5 I/O registers and all of them can be

specified using an even address value (SA<0> = 0). More detail information of these registers are described in **Section 12.4.**

The module supports both normal writes and read accesses. Each type of access is described in the following paragraphs. The OEM module does not support DMA transfers.

Figure 6-1: 6302 Mini ISA OEM Module Interface Connector



OUTPUT SIGNALS		
Pin #	**Pin Name**	**Description**
23	CD_LED	This active high output status signal is used to indicate that the module is receiving a RangeLAN2 signal. This signal can be used to drive an external LED.
46	INTR#	This is the interrupt signal from the module. This signal is ISA bus compatible. It is active low and is an inverted pulse approximately 1ms in duration. It is used to interrupt the host computer when the module requires servicing.
14	IOCHRDY#	This active low signal is used to lengthen an IOREAD# or IOWRITE# signal when the module can not respond quickly enough. This signal will not be held low for longer than 2 uSec, and is an open drain output capable of sinking 24 mA of current.
47	IOCS16#	This active low signal is used to indicate that the I/O address being selected by SA<2..0> and CS# is a 16-bit address. This signal will not be active in 8-bit configurations. This signal is an open drain output that is capable of sinking 24 mA.
25	MASTER_LED	This active high output status signal is used to indicate that the module is acting as a Master station. This signal can be used to drive an external LED.
45	SYNCH_LED	This active high output status signal is used to indicate that the module is synchronized to a Master station. This signal can be used to drive an external LED.
48	RSSI	This high impedance Received Signal Strength Indication signal should be left unconnected if not being used. In most applications, this signal is digitized internally to the module and a digital value is available to the host with the packet that the measurement corresponds to.
22	TX/RX_LED	This active high output status signal is used to indicate that the module is in transmit mode. This signal can be used to drive an external LED.

POWER SIGNALS		
Pin #	**Pin Name**	**Description**
15, 16	VDD	These power inputs are tied together on the module and supply all of the power to the module. Input voltage range: 4.75V to 5.25V. Input current depends on function: RX Mode: 175 mA typical TX Mode: 350 mA typical Doze Mode: 20 mA (average) Sleep Mode: 2 mA typical
1, 26, 27,44	GND	Power returns

6.3.2 Interrupts and I/O Ports

The drivers for the Mini-ISA OEM modules supports the following ISA Bus specification interrupts (IRQ3, IRQ4, IRQ5, IRQ7, IRQ10, IRQ12 and IRQ15). A single interrupt output signal is provided by the OEM module, and must be connected to the corresponding interrupt line on the platform's interface bus. For example, the default interrupt for the standard Mini-ISA driver is IRQ15. The Mini-ISA interface board is configured to connect the PC ISA bus IRQ15 to the OEM module's INTR# interrupt output. This allows the interrupt of the OEM module to be interrupted as IRQ15 by the PC and driver.

The Mini-ISA OEM module requires an address space of 8 consecutive bytes that is considered to be an I/O port to an XT or AT compatible platform. The drivers for the Mini-ISA OEM module support the following starting addresses for I/O: 100, 120, 140, 218, 270, 280, 290, 298, 2A0, 2A8, 2E0, 300, 310, 358, 360, and 368. The platform must decode the selected I/O port range and provide a chip select (CS#) to the OEM module. The driver must be configured for the selected I/O port range also.

6.4 8-Bit vs. 16-Bit Data Operation

Both 8-bit and 16-bit data operations are supported. The OEM module can be configured for the desired operation through the driver, by specifying Byte (8-bit) or Word (16-bit) operation. The standard drivers supplied with the module automatically determine whether the host operates in 8-bit or 16-bit modes. When the driver is loaded by the host, the driver automatically performs a test to determine the mode. A 16-bit transfer to the OEM module is first attempted. If the transfer between the driver and the OEM module is successful, 16-bit mode will be used. If the driver was not able to successfully write and subsequently read back from the upper byte of the data word, then 8-bit mode will be used. In either mode, SA<2..0> = 0H is used to access the I/O data register(s).

6.5 Read and Write Operations

This section describes the process for reading and writing to the OEM module. Both operations are performed as I/O Accesses by the host. Differences between 8-bit transfers and 16-bit transfers are discussed. These read and write operations are consistent with the ISA bus specification.

6.5.1 Host Write Operation to Mini-ISA Module

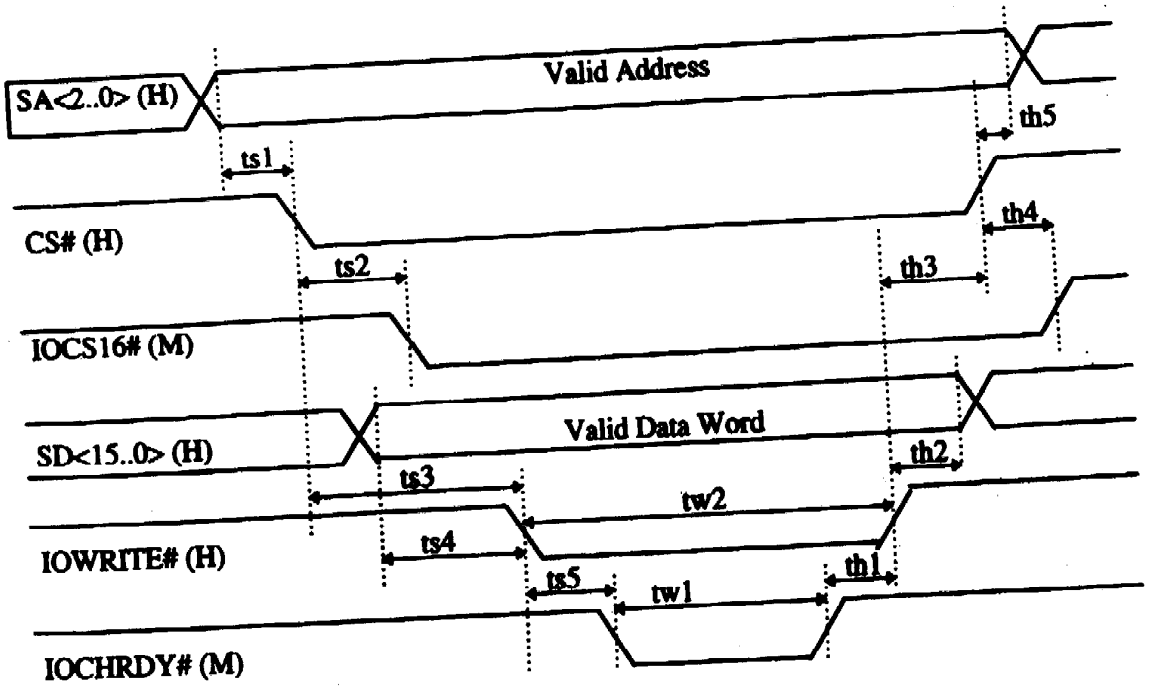
This operation occurs when the host needs to write either an 8-bit or 16-bit data word to the Mini-ISA OEM module to one of it's 8 registers. The process is detailed below and shown in **Figure 6-2** for 16-bit transfers and **Figure 6-3** for 8-bit transfers. Signals controlled by the host are designated with a (H), while (M) denotes module signals.

The host applies the OEM I/O register select address bits SA<2..0> along with the Chip Select CS# to the OEM module. The module will respond by setting the IOCS16# if the address selected is a 16-bit address. If IOCS16# is not asserted then an 8-bit operation will occur. Timing of the IOCS16# signal is dependent upon both the address A<2..0> and the CS# being asserted.

The host places the data word on to the databus, either SD<15..0> for 16-bit data or SD<7..0> for 8-bit. The host also drives IOWRITE# active (to the LOW state) to set up a write to the module. The module will assert IOCHRDY# as necessary to tell the host to lengthen the IOWRITE# signal if the module can not complete the operation quickly enough. The length of the IOCHRDY# signal may vary from one write operation to another, but it will not exceed the maximum duration specified.

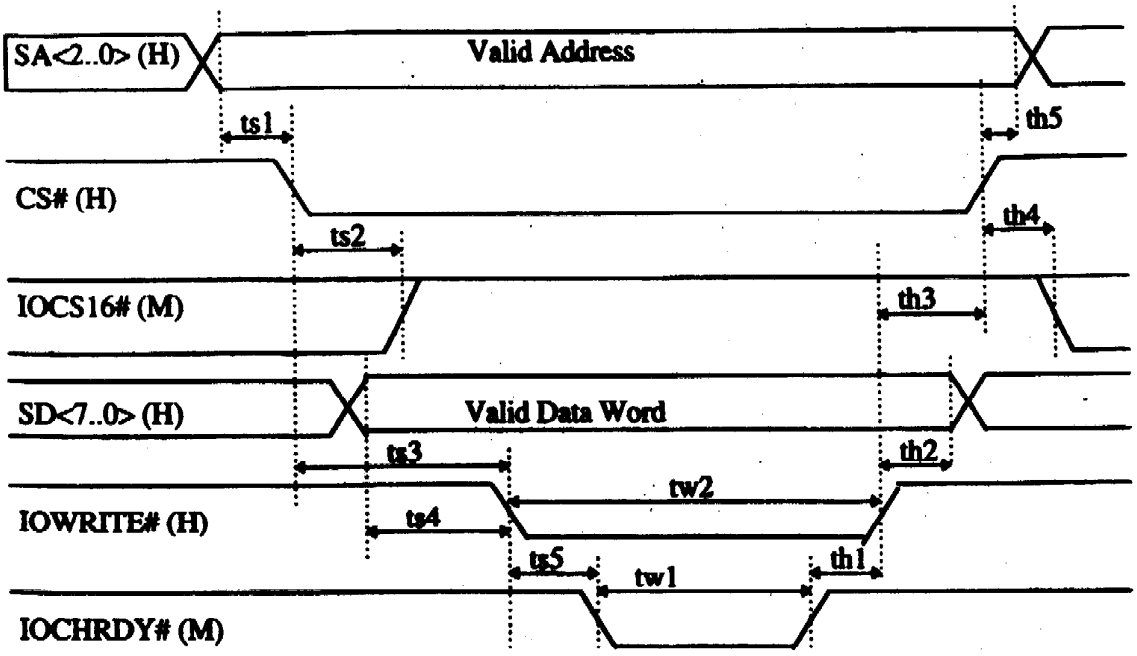
The host drives IOWRITE# high with the timing dependent upon IOCHRDY#. The data will be latched into the module's addressed I/O register on the rising edge of IOWRITE#. After meeting the required hold time, the host de-asserts the CS# signal. The module completes the operation by de-asserting IOCS16# for 16-bit operations.

Figure 6-2: 16-Bit Write Operation to Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOWRITE# Falling Edge	≥ 91
ts4	Setup, SD<15..0> to IOWRITE# Falling Edge	≥ 22
ts5	Setup, IOWRITE# to IOCHRDY# Falling Edge	≤ 44
tw1	Pulse Width, IOCHRDY# Asserted	≤ 15,600
tw2	Pulse Width, IOWRITE# Asserted	≥ 176
th1	Hold, IOCHRDY# to IOWRITE# Rising Edge	TCLK
th2	Hold, SD<15..0> from IOWRITE# Rising Edge	≥ 32
th3	Hold, CS# from IOWRITE# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0
TCLK	Clock Period, System Bus Clock	125 to 167

Figure 6-3: 8-Bit Write Operation to Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOWRITE# Falling Edge	≥ 91
ts4	Setup, SD<7..0> to IOWRITE# Falling Edge	≥ 22
ts5	Setup, IOWRITE# to IOCHRDY# Falling Edge	≤ 44
tw1	Pulse Width, IOCHRDY# Asserted	≤ 15,600
tw2	Pulse Width, IOWRITE# Asserted	≥ 176
th1	Hold, IOCHRDY# to IOWRITE# Rising Edge	TCLK
th2	Hold, SD<7..0> from IOWRITE# Rising Edge	≥ 32
th3	Hold, CS# from IOWRITE# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0
TCLK	Clock Period, System Bus Clock	125 to 167

6.5.2 Host Read Operation from Mini-ISA Module

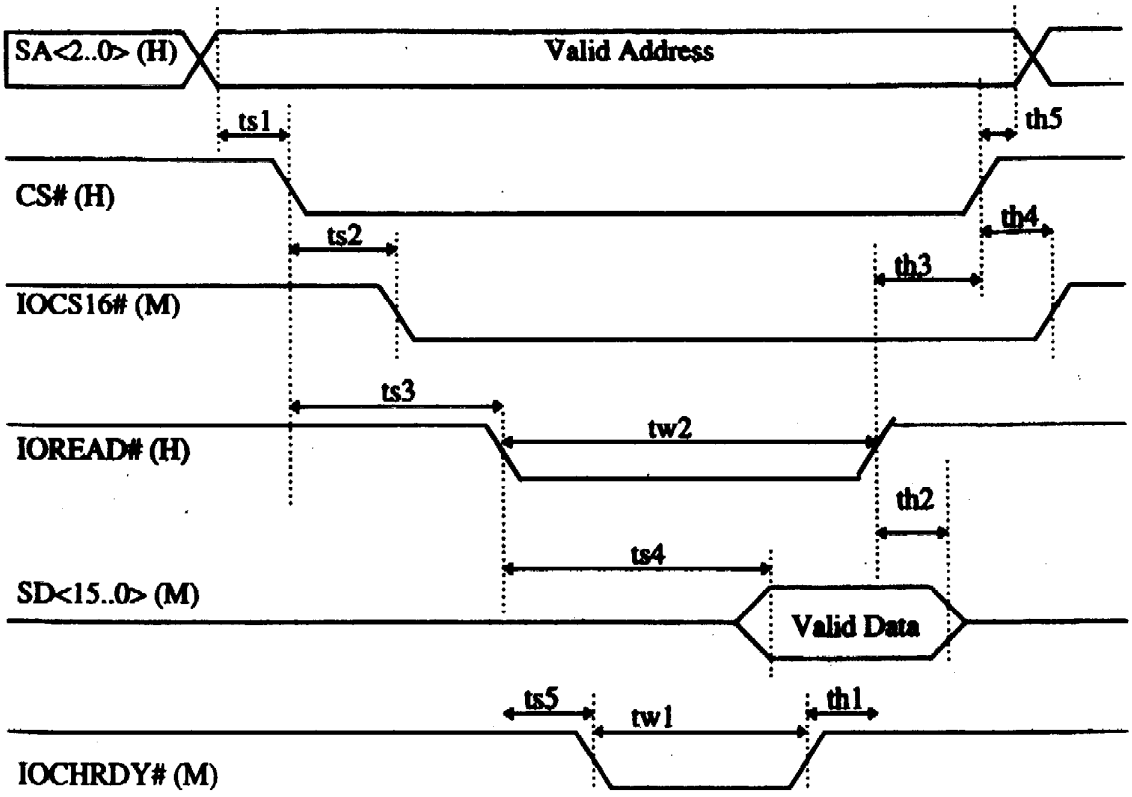
This operation occurs when the host needs to read either an 8-bit or 16-bit data word from one of the OEM module's 8 registers. The process is detailed below and shown in **Figure 6-4** for 16-bit transfers and **Figure 6-5** for 8-bit transfers. Signals controlled by the host are designated with a (H), while (M) denotes module signals.

The host applies the OEM I/O register select address bits SA<2..0> along with the Chip Select CS# to the OEM module. The module will respond by setting the IOCS16# if the address selected is a 16-bit address. If IOCS16# is not asserted then an 8-bit operation will occur. Timing of the IOCS16# signal is dependent upon both the address A<2..0> and the CS# being asserted.

The data bus, SD<15..0> for 16-bit data or SD<7..0> for 8-bit transfers is maintained in a tri-state condition by the host. The host drives IOREAD# active (to the LOW state) to set up a read from the module. The module will assert IOCHRDY# as necessary to tell the host to lengthen the IOWRITE# signal if the module can not complete the operation quickly enough. The length of the IOCHRDY# signal may vary from one write operation to another, but it will not exceed the maximum duration specified.

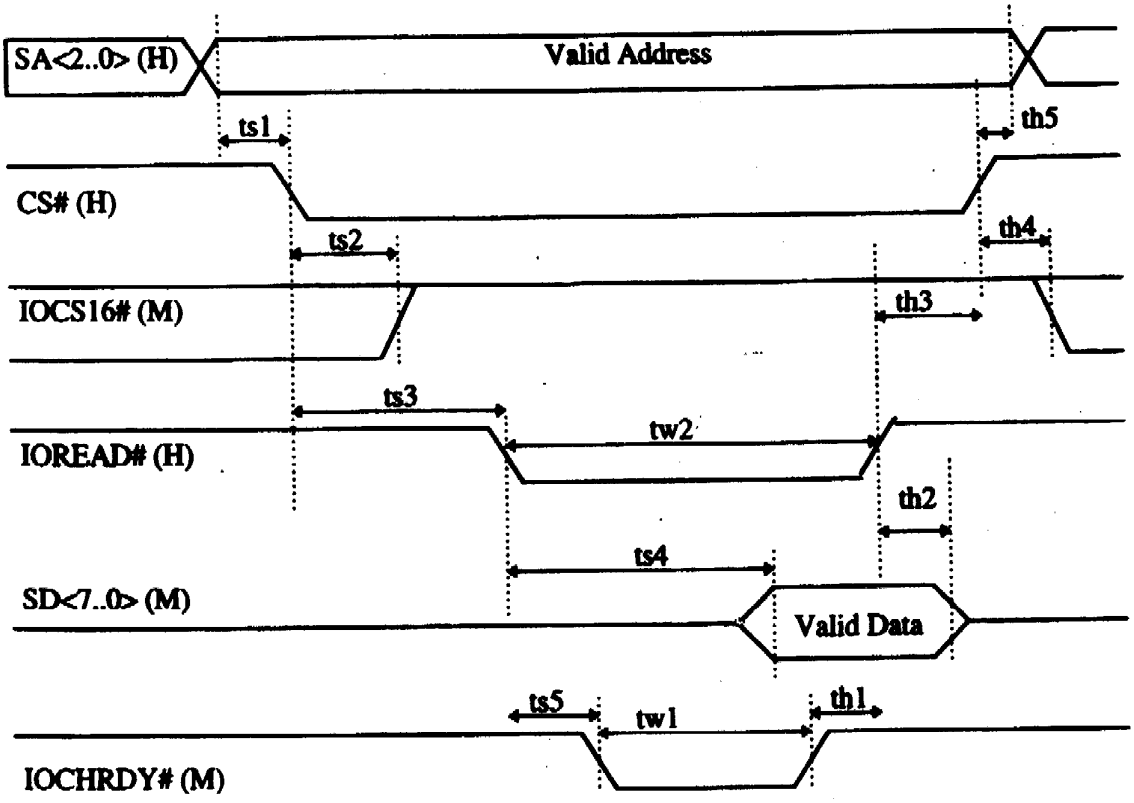
The OEM module accesses the addressed register and drives the databus with the data word from the register. The host then drives IOREAD# high with the timing dependent upon IOCHRDY#. After meeting the required hold time, the host de-asserts the CS# signal. The module completes the operation by de-asserting IOCS16# for 16-bit operations.

Figure 6-4: 16-Bit Read Operation from Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOREAD# Falling Edge	≥ 91
ts4	Setup, IOREAD# to Valid SD<15..0>	≤ 110
ts5	Setup, IOREAD# to IOCHRDY# Falling Edge	≤ 44
tw1	Pulse Width, IOCHRDY# Asserted	≤ 15,600
tw2	Pulse Width, IOREAD# Asserted	≥ 176
th1	Hold, IOCHRDY# to IOREAD# Rising Edge	TCLK
th2	Hold, SD<15..0> from IOREAD# Rising Edge	≤ 30
th3	Hold, CS# from IOREAD# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0
TCLK	Clock Period, System Bus Clock	125 to 167

Figure 6-5: 8-Bit Read Operation from Module



Timing Parameter	Description	Value (nSec)
ts1	Setup, SA<2..0> to CS#	≥ 0
ts2	Setup, CS# to IOCS16# Falling Edge	≤ 90
ts3	Setup, CS# to IOREAD# Falling Edge	≥ 91
ts4	Setup, IOREAD# to Valid SD<7..0>	≤ 110
ts5	Setup, IOREAD# to IOCHRDY# Falling Edge	≤ 44
tw1	Pulse Width, IOCHRDY# Asserted	≤ 15,600
tw2	Pulse Width, IOREAD# Asserted	≥ 176
th1	Hold, IOCHRDY# to IOREAD# Rising Edge	TCLK
th2	Hold, SD<7..0> from IOREAD# Rising Edge	≤ 30
th3	Hold, CS# from IOREAD# Rising Edge	≥ 11
th4	Hold, IOCS16# from CS#	≥ 0
th5	Hold, SA<2..0> from CS#	≥ 0
TCLK	Clock Period, System Bus Clock	125 to 167

6.6 Mechanical Issues

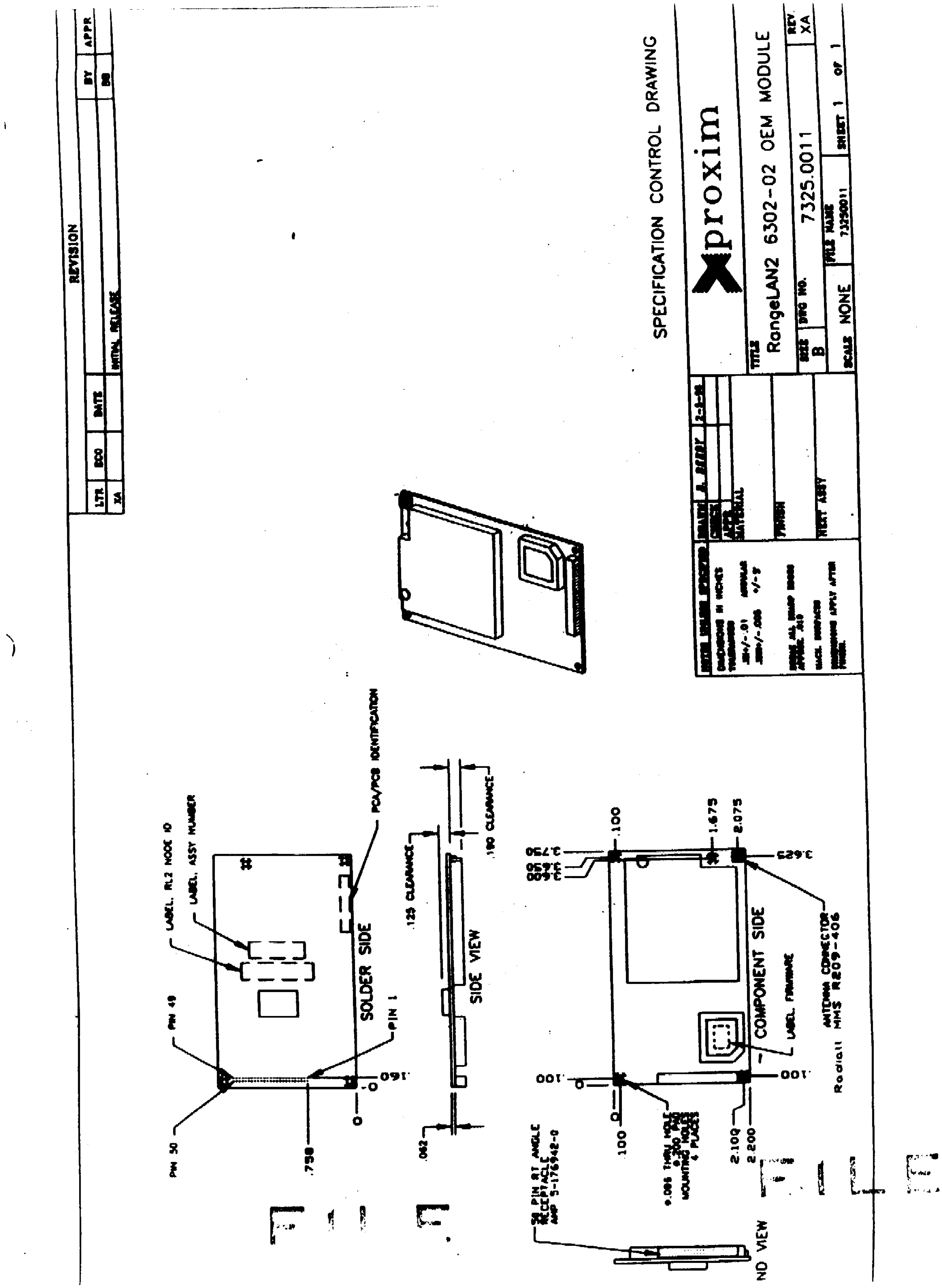
The OEM module has four mounting holes that are used for installing the module to the host with stand-offs. **Sections 9.4 and 9.5** provide guidelines about the positioning of the OEM module relative to the enclosure and other components.

6.6.1 Outline Drawing and Dimensions

The Mini-ISA module outline drawings are included in the following pages.

Insert 6-1: 6302/6303 Mini-ISA OEM Module Drawing

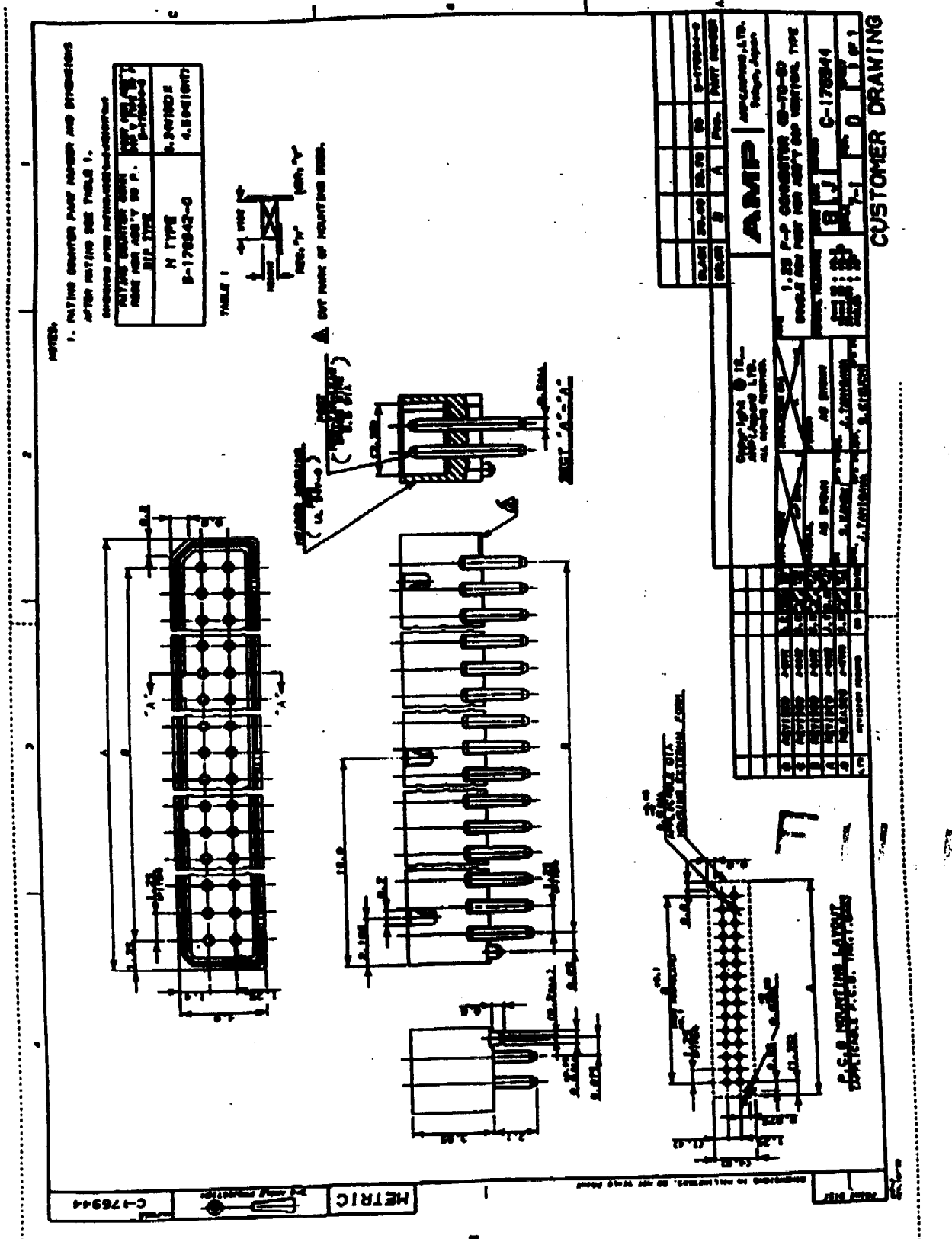
The drawing of 6302/6303 Mini-ISA OEM Modules is included in the following two pages.


SPECIFICATION CONTROL DRAWING
proxim
RangeLAN2 6302-02 OEM MODULE
7325.0011
REVISION
INITIAL RELEASE
SIZE B
SCALE NONE
SHEET 1 of 1
REV XA
SOLDER SIDE
SIDE VIEW
COMPONENT SIDE
END VIEW
LABEL, RL2 NODE ID
LABEL, ASSY NUMBER
PCA/PCB IDENTIFICATION
PIN 49
PIN 50
PIN 1
.125 CLEARANCE
.190 CLEARANCE
LABEL, FIRMWARE
ANTENNA CONNECTOR
Radiall MMS R209-406
50 PIN RT ANGLE RECEPTACLE
AMP 5-176942-0

Insert 6-2: Drawing, AMP S-176942 / S-176943 / S-176944 Connectors

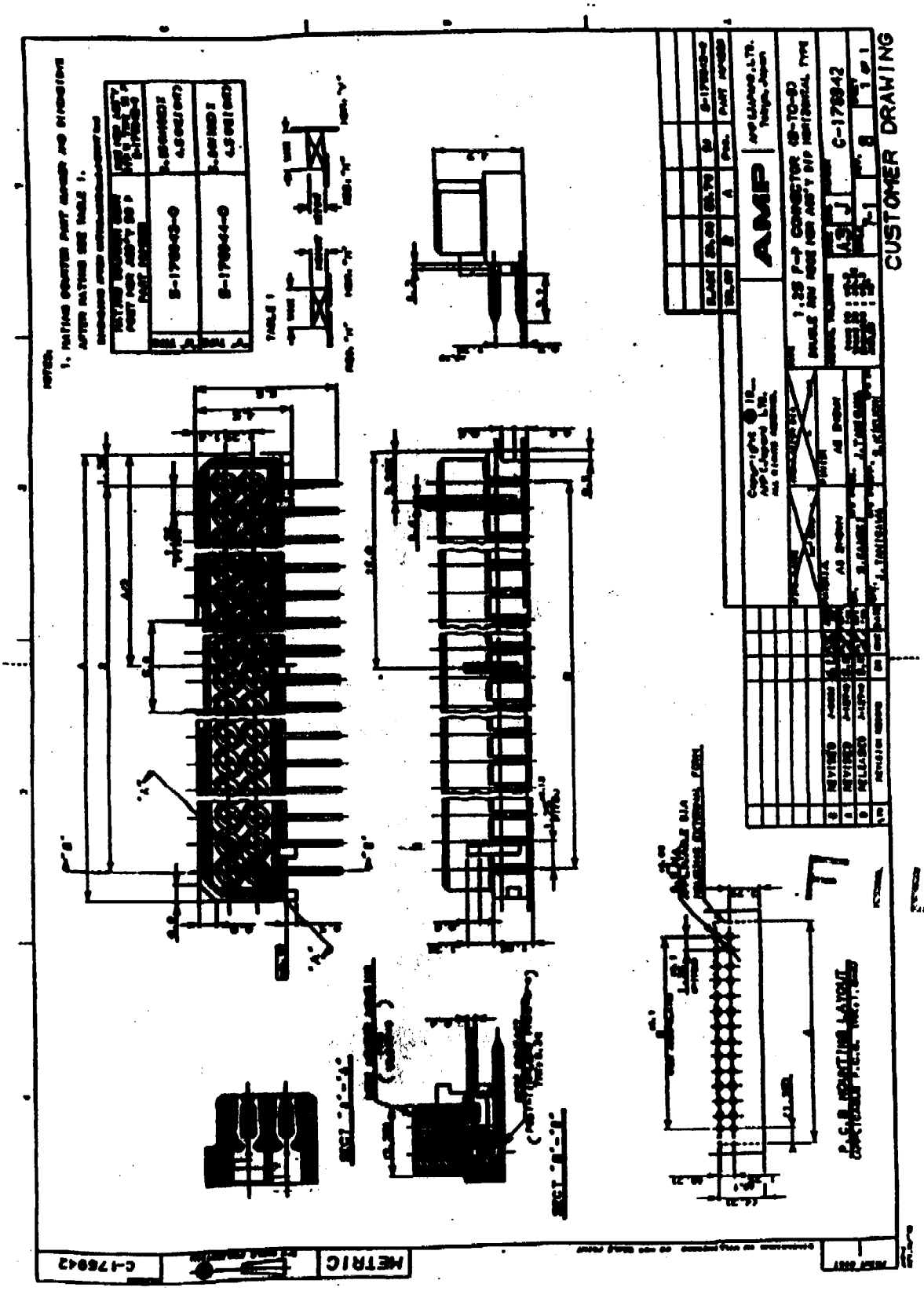
The drawing of the AMP connectors are included in the following pages.

AMP Connector Datasheet, Perpendicular Mating Connector # C-176944



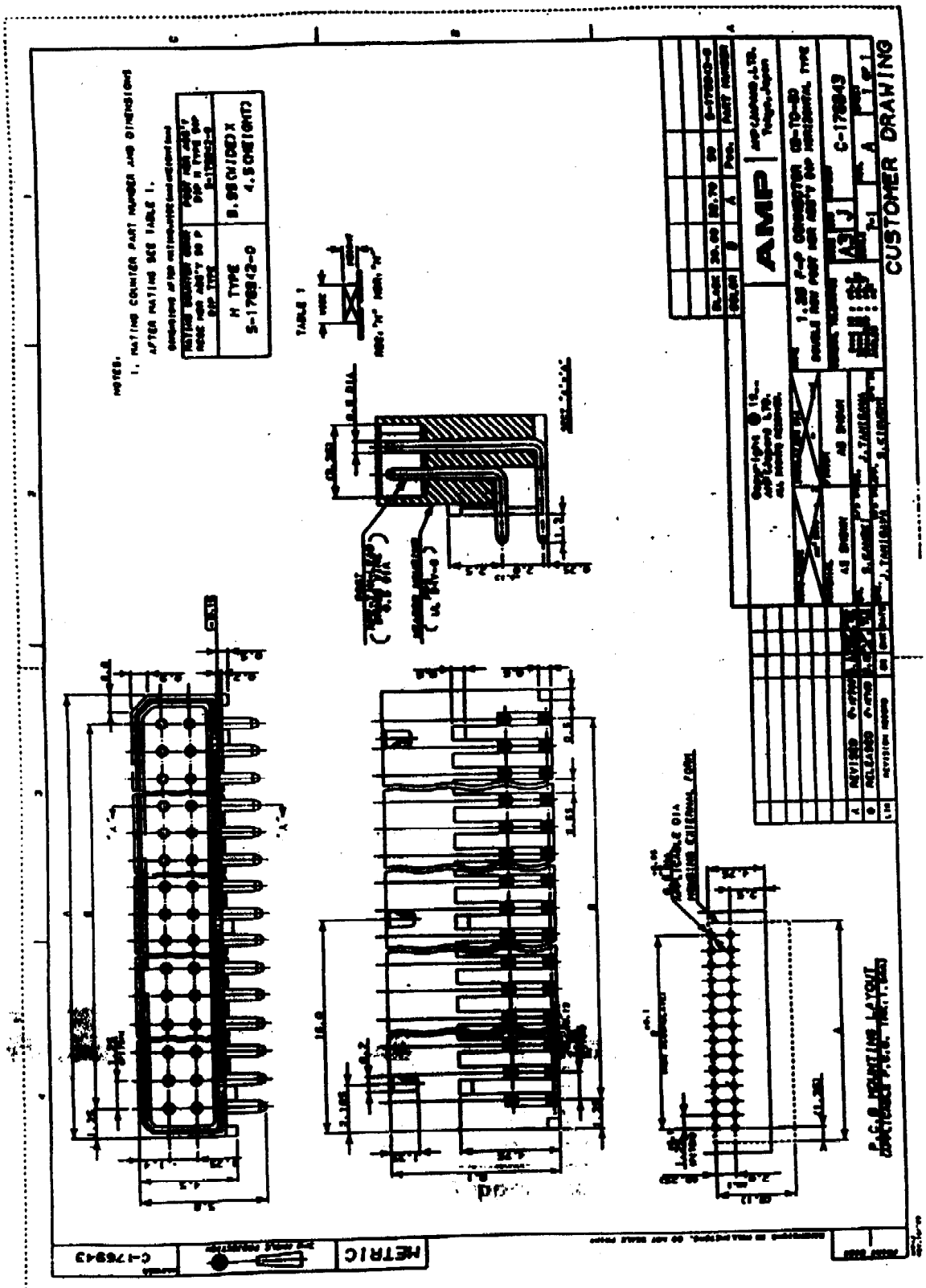
FILE

AMP Connector Datasheet, OEM Module Connector, #C-176942



FILE

AMP Connector Datasheet, Parallel Mating Connector #C-176943



Insert 6-3: Data sheet, Berg (87011-625) Connector

The data sheet of the Berg connector is included in the following pages.

FOR MORE DETAILED PRODUCT INFORMATION, OR FOR THE LOCATION NEAREST YOU, CONTACT ONE OF THE REGIONAL HEADQUARTERS LISTED BELOW.

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Fax: 91-22-2852823

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Fax: 91-812-342500

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Republic of China
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Fax: 886-3-462-0676

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1-800-237-2374 (U.S.A. & CANADA) or 717-938-7212

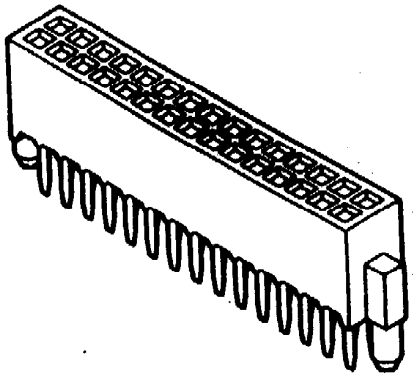
BERG™
ELECTRONICS

FILE

PCB Mounted Receptacle Assemblies

High-Density, Through-Mount, Vertical

1.27 × 1.27 mm (0.050 x 0.050 in.) Centerlines



Rib-Cage™ II Through-Mount Receptacle Assemblies

Features

- High-density, [illegible] mm (0.050 in.) centerline system [illegible] occupies only one-eighth the [illegible] of 2.54 mm (0.100 in.) centerlines.
- Available in double [illegible] vertical assemblies.
- Sizes in increments [illegible] from 10 to 100 positions.
- Compatible with vapor [illegible] and infrared reflow soldering [illegible] processes.
- Contacts are selectively [illegible] with gold in the contact area [illegible] and on the solder tails.
- Unique design of beryllium-copper receptacle provides 100 grams normal force and 1.14 mm (0.0[illegible]in.) wipe to ensure reliable interconnection after repeated [illegible]ing cycles.
- Connectors are also available with side-key polarization.
- Available with hold-downs and locators, which are highly recommended to maintain proper alignment of the connector and PCB.
- Standoffs prevent entrapment of cleaning solutions.

Mating Data

[illegible]pprovals and [illegible]rtifications

File no. E88906

File no. LR46823

Tech[illegible] Data

Materials

Housing ..... d polyphenyl[illegible] (PPS), UL 94 V

Color ..... Brown

Temper[illegible]e ..... -55°C to +130°C

- Applicable soldering processes ..... Wave

- Contact ..... Beryllium-copper

Plating

- Finish

Contact ar[illegible] ..... 0[illegible].30 µin.) min gold

Solder tail ..... 2.54[illegible] µin.) min tin-lead

Electrical Performa[illegible]

- Insul[illegible]on resista[illegible] ..... 50,000 MΩ min initial

With[illegible]ding volt[illegible] ..... 800 V ac

ma[illegible]ating ..... mp dc (30°C temperature rise)

- Contact resistance ..... 7[illegible] mΩ max initial, 25 mΩ max after environmental test

Mechanical Performa[illegible]

- Mating force ..... [illegible] (4.0 ozf) max per contact
- Unmating force ..... [illegible]0 (0.25 ozf) min per contact
- Durability (mating cy[illegible] ..... 200 min

Packaging

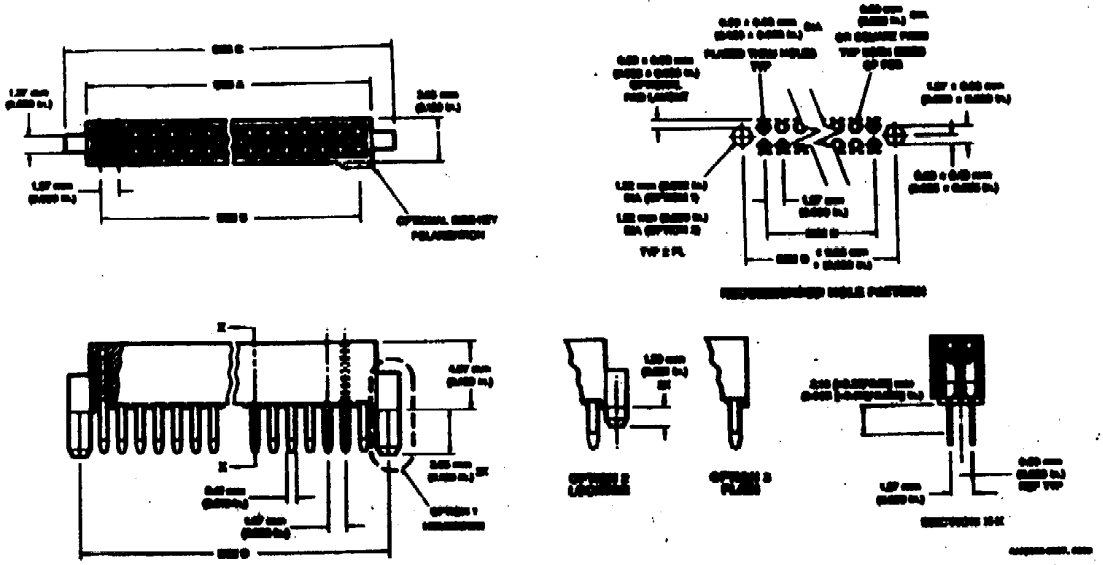
- Antistatic tubes

FILE

Berg Connector, OEM Module Connector, #87011-625

Description

High-Density, Through-Mount, Vertical Receptacle Assemblies
1.27 × 1.27 mm (0.050 × 0.050 in.) Centerlines



Ordering Data

Base number specifies through-mount receptacle assembly configuration: □□□□□-6XX

Dash number specifies contact finish [6 = 0.76 µm (30 µin.) gold] and number of positions per row (5 through 50 in increments of 5).

87815 = nonpolarized with hold-downs
87472 = side-key polarization with hold-downs
87013 = nonpolarized with locators
87014 = side-key polarization with locators
87011 = nonpolarized
87012 = side-key polarization

Dash Number	Size	Dimensions							
		A		B		C		D	
		mm	in.	mm	in.	mm	in.	mm	in.
						(applicable to options 1 and 2 only)			
605	2 × 5	6.756	0.266	5.08	0.200	9.398	0.370	8.128	0.320
610	2 × 10	13.106	0.516	11.43	0.450	15.748	0.620	14.478	0.570
615	2 × 15	19.456	0.766	17.78	0.700	22.098	0.870	20.828	0.820
[redacted]									
635	2 × 35	44.806	1.766	43.18	1.700	47.498	1.870	46.228	1.820
640	2 × 40	51.206	2.016	49.53	1.950	53.848	2.120	52.578	2.070
645	2 × 45	57.906	2.266	55.88	2.200	60.198	2.370	58.928	2.320
650	2 × 50	63.906	2.516	62.23	2.450	66.548	2.620	65.278	2.570

Customer Support Materials

Description	Order No.
Customer Product Drawings	By Base No.
Product Specifications	BUS-12-087
Application Drawing	TA-801
Application Specification	BUS-20-052
Product Samples	By Part No.

Insert 6-4: 6302/6303 Mini-ISA OEM Module Technical Information

The technical information of 6302/6303 Mini-ISA module is included in the following pages.

RangeLAN2 6300 OEM Module Technical Information

proxim

GENERAL

1. Typical system range: up to 500 feet in offices and up to 1000 feet in open spaces*. Range will vary depending on a number of factors including antenna design, board integration and the physical environment between RangeLAN2/OEM equipped units
2. Frequency range: 2.4 - 2.4835 GHz for U.S., 2.471 - 2.497 GHz for Japan, varies for other countries
3. Data rate: 1.6 Mbps (main), 800 Kbps (backoff)
4. Modulation type: 4FSK (main), BFSK (backoff)
5. Regulations compliant:
   FCC Parts 15.209 and 15.247 compliant
   ETSI Parts ETS 300 328
   MKK-Characteristic Test Method for Radio Equipment - Part 2
   *Caller ID is enabled on JP units.
6. Certification is the responsibility of the OEM

TRANSMITTER

1. Output power: +20 dBm (max.) EIRP with 2 dBi gain antenna
2. Channel spacing: 1 MHz
3. Output spectrum:
   ±0.5 MHz: <-20 dBc
   ±2.0 MHz: <-50 dBc typical
4. Spurious Emissions:
   Harmonics: <-50 dBm
   Other (>5 MHz from f_0): <-50 dBm

RECEIVER

1. Sensitivity:
   at 1.6 Mbps: -77 dBm typical
   at 800 Kbps: -85 dBm typical
2. Maximum input power:
   Performance range: <-5 dBm
   Survivability range: +5 dBm
3. Channel rejection:
   ±2 MHz: -45 dBc
   ±4 MHz: -50 dBc

FREQUENCY GENERATION

1. Frequencies/sequence (hops): 79-U.S., 43-ETSI, 23-Japan
2. Frequency stability: 50 ppm
3. Orthogonal hopping channels: 15

ELECTRICAL

1. 50-pin interface based on standard ISA pins, most signals map directly from ISA
2. A device must be added to decode Chip Select from ISA address lines
3. Single interrupt line may be mapped to any IRQ

The following is a list of the signals on the 50-pin interface:

Pin#	Signal	I= Input, O = Output
1	GND	I
2-9	SD0-7	I/O
10	CS#	I
11	IOWRITE	I
12	IOREAD	I
13	Not used	
14	IOCHRDY	O
15	VDD	Power Input
16	VDD	Power Input
17	Not used	
18	SA0	I
19	SA1	I
20	SA2	I
21	Not used	
22	TX/RX LED	O
23	CD_LED	O
24	Not used	
25	Master_LED	O
26	GND	Power Input
27	GND	Power Input
28	AEN	I
29-36	SD15-SD8	
37-43	Not used	
44	GND	Power Input
45	Synch_LED	O
46	INTR	O
47	I/OIS16	O
48	RSSI	
49-50	Not used	

SOFTWARE/DRIVERS

1. Proxim-designed MAC layer supports IEEE 802.3 frame format
2. ODI (Novell)/NDIS (Microsoft) interfaces
3. Netware 3.1.X/4.X NOS support
4. Personal Netware NOS support
5. Windows 95 and Windows NT NOS support
6. Microsoft Windows for Workgroups NOS support
7. Other drivers and interfacing options are also available

RANGELAN2 6300 OEM Module
Technical Information

proxim

POWER

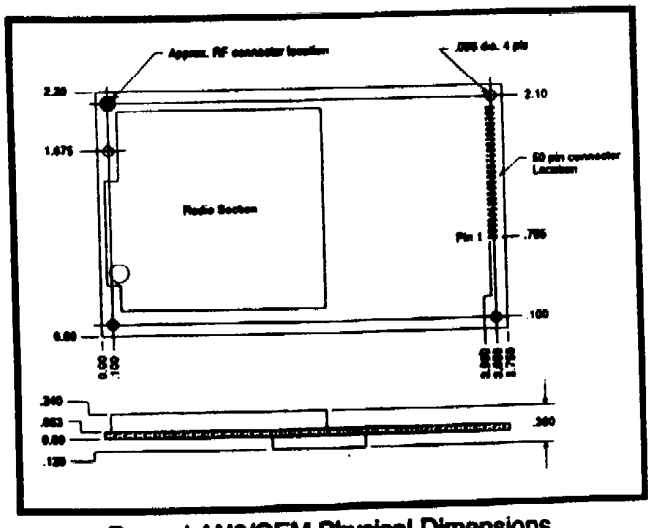
1. Input voltage: 4.75V - 5.25V
2. Input current:
   - RX: 175 mA typical
   - TX: 350 mA typical
   - Sleep: 2 mA typical
   - Snooze: 20 mA typical (average value)

ENVIRONMENTAL

1. Temperature range:
   - Operation: -20°C to +60°C
   - Storage: -50°C to +85°C
2. Humidity: 10% to 90%
3. Vibration: .27G (5 to 500 Hz)
4. Shock: 10 G, or 6 foot drop
5. MTBF: 100,000 hours

MECHANICAL

1. Dimension: 2.20 inches x 3.75 inches x .4 inches
2. Weight: <60 gram
3. Interface connector: Amp 5-176942-0 or Berg 87400-125. Can be stacked, perpendicular or end-to-end fashion.
4. Antenna connector: Radiall MMS plug receptacle (part number R 209406).



RANGELAN2/OEM Physical Dimensions
(nominal)

DESIGN KIT

Available for $4995 to Qualified OEMs:

1. 6300 Series OEM Module (Specify: FCC, ETSI, or Japan platform)
2. Half-sized ISA board maps ISA pins to 50-pin connector on OEM Module
3. RangeLAN2 7100 ISA product for test bed
4. OEM Module test antenna with Radiall connector
5. Standard ODI and NDIS drivers for x86 host platforms to drive OEM module
6. Radiall to SMA cable assembly to allow connection of standard SMA connector for antenna of desired
7. Developer Design Guide which contains confidential technical information for qualified OEMs performing design-in of RangeLAN2 6300 OEM Module

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