Harmony 7630 Open Air Compact Flash™ Card Technical Description

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PRODUCT:

The product is a FHSS WLAN adapter operating in the 2.4-2.4835 GHz band with a nominal TX output power of 100mW. It is an enclosed circuit board assembly with a 50-pin data / power connector and a coaxial antenna connector.

USER CONNECTIONS:

Data and power are provided through the 50-pin connector. A unique antenna connector is provided for attaching the antenna to the adapter.

INTERNAL CLOCK AND RF OSCILLATOR FREQUENCIES:

Processor ASIC	24 MHz, 32 kHz
RF synthesizer	reference 4MHz
	TX frequency 1201-1240MHz, 500kHz steps
	RX frequency 1145.75-1184.75MHz, 500kHz steps
transmit LO, transmit and receive range	2402-2480MHz, 1MHz steps
receive LO	2291.5-2369.5MHz, 1MHz steps
receive IF	110.5MHz, 1MHz BW

SIGNAL FLOW:

Data is transferred through the 50-pin connector to the processor. The processor ASIC also contains the baseband radio functions, A/D and D/A converters, transceiver control functions and memory interface.

In transmit, the synthesizer tunes from 1201 to 1240MHz in 500kHz steps. It is part of an integrated 2.4GHz transceiver IC, using an external VCO and buffer, loop, and modulation filters. The reference for the synthesizer is a 4 MHz processor ASIC output derived from the 24 MHz oscillator. The VCO is directly FM modulated with –20dB BW of less than 1MHz. The transceiver IC doubles the modulated external VCO and sends the signal to a bandpass filter, power amplifier, transmit / receive switch, lowpass filter, and antenna connector.

In receive, the synthesizer tunes from 1145.75 to 1184.75MHz in 500kHz steps. The receive signal path is from the antenna connector, through the lowpass filter and transmit / receive switch shared with the transmitter, an LNA, an image reject filter, and to the integrated transceiver IC. It is mixed down to IF by the receive LO which is generated inside the transceiver IC by doubling the VCO output. The IF output of the mixer goes off chip for bandpass filtering, back on for additional amplification, off again for more filtering and then back on chip for limiting and FM quadrature demodulation. The demodulated signal is amplified and filtered at baseband before being converted to a bit stream in the processor ASIC.

There are two shielded areas. The VCO and buffer are under one shield, and the balance of the RF is under the other shield. RF filtering is distributed at each stage with final TX filtering between the transmit/receive switch and the antenna.