Harmony 8570 Access Point Technical Description
Document # 610.00xx

PRODUCT:
The product is a WLAN adapter operating in the 5.15 – 5.35 GHz band with a maximum TX output power of 50mW. It is a small desktop box with associated wall plug mounted 12VDC power supply, dual external antennas and a 10/100baseT port for connection to standard wired LAN. The peak gain for each antenna is 6dBi. Refer to the manual for MPE statement. This device can either be stand alone connected to an RJ-45 LAN hub port, or be connected to the RJ-45 port of a computing device.

USER CONNECTIONS:
There is a single RJ-45 connector supplied for the single 10/100baseT port. The LED next to the RJ-45 changes colors to indicate the different connection speeds and blinks to indicate Ethernet activity.

The 12VDC power is connected via a 2.5mm coaxial power connector.

TEST CONNECTIONS:
There are two 50 ohm RF ports on the PCA, one for each of the two antenna connections. Each antenna is terminated with a Radiall UMP2.0 snap-on plug. A slide-on version of the plug can be used during FCC certification for conducted measurements.

ACCESSORIES:
Proxim P/N 4000.0007 wall mounted unregulated power supply, 100-120V/50-60Hz input, 12V 1A nominal output. Proxim P/N 4000.0030 universal power supply, 100-240V/47-63Hz, 0.8A input, 12V, 1.5A nominal output.

Proxim P/N 6001.0124 unshielded twisted pair RJ-45 cable assembly.

INTERNAL CLOCK AND RF OSCILLATOR FREQUENCIES:

Processor ASIC	33MHz
Ethernet controller	25MHz
RF synthesizer	PLL frequencies of 40, 80, or 160MHz derived from a 32 MHz oscillator
TX and RX frequencies	5180-5320MHz, 20MHz steps
LO Leakage	4144-4256MHz
Mixer Product	6216-6384MHz
Baseband bandwidth	20MHz

SIGNAL FLOW:
The memory and Ethernet controller communicate with the processor IC. The MAC/baseband processor integrates the media access control (MAC), the baseband radio functions, A/D and D/A converters, transceiver control functions and a PCI/Cardbus interface.

The Ethernet controller and processor ASIC each support their own on board clock oscillators at 25 and multiples of 33MHz to include 100MHz and 200MHz.

In transmit, the synthesizer tunes to one of the TX frequencies listed above. Data is initiated at the Ethernet interface. The Ethernet controller processes serial data to the SDRAM which is then processed by the internal PCI controller within the processor IC to the MAC/baseband processor. Current outputs from the DAC of the MAC/baseband processor are low-pass filtered through the external reconstruction filter. The I and Q signals are converted to RF thru a dual-conversion architecture, from baseband to IF and from IF to RF signals. These signals are driven off-chip through a power amplifier, through the antenna switch, and to the antenna connector.

In receive, the synthesizer tunes to one of the RX frequencies listed above. The receive signal path is from the antenna connector, through the antenna switch, a band pass filter, an LNA, a receive balun, and to the integrated transceiver IC. Inside the transceiver IC, the RF mixer converts the output of the on-chip LNA to an intermediate frequency. The IF mixer converts this signal down to baseband I and Q signals. The I and Q signals are low-pass filtered by the external channel select filters, and amplified by a baseband PGA controlled by digital logic. The baseband signals continue through external anti-alias filters before being sent to the ADC of the MAC/baseband processor. Data at the PCI interface of the MAC/baseband processor is processed by the PCI controller within the processor IC to SDRAM which is then processed by the Ethernet controller to serial data to be sent to the Ethernet interface.