DESCRIPTIVE INFORMATION

FCC FILING FOR SC4812ET @1.9 GHz CDMA BTS

The Information in this exhibit is in accordance with the FCC Rules and Regulations, Vol. II, Part 2, Subpart J. Sections 2.983 through 2.999 are addressed.

Section 2.983 (a) **Name of Applicant and Manufacturer:** MOTOROLA

Section 2.983 (b) **Identification of Equipment:** IHET6YZ1

Section 2.983 (c) **Quantity Production:** Quantity Production is Planned.

Section 2.983 (d) **Technical Description**

This Transmitter is intended for use in the Public Cellular Radio Telecommunications Service and is designed in compliance with the FCC Rules and Regulations Title 47, Part 24(E).This transmitter is capable of spread spectrum (CDMA) operation, and allows up to 64 Walsh codes to support Pilot, Sync, Paging and Traffic channels.

(1) **Types of Emissions**

This equipment will be capable of operation using wide band spread spectrum techniques employing Direct Sequence Code Division Multiple Access (DS-CDMA) digital communication techniques.

For this transmitter, the emission designator is 1M25F9W (per FCC Part 2.201, subpart C).

(2) **Frequency Range**

This transmitter operates within the 1930 to 1990 MHz Band (per FCC Part 24). This base station will support CDMA operations on channel numbers 25 through 1175 (1931.25 MHz - 1988.75 MHz).

(3) **Range of Operating Power**

The rated maximum average power out of the SC4812ET @1.9 GHz CDMA BTS is 40 W (46.0 dBm). However, in CDMA the actual power output is based on the number of traffic channels in operation. The minimum power occurs when only a pilot signal is present. The maximum power occurs when a pilot along with synchronization, paging, and traffic channels are present. For a typical system setup, the theoretical difference between minimum power and maximum power is 8dB. The output power is variable in 0.25 dB steps. The range is 12 dB.

(3) **Range of Operating Power (cont.)**

In addition, the dynamics of a CDMA system allow for what is called "cell breathing". This allows an operator to vary the range of a cell by controlling the power of the pilot signal.

(4) **Maximum Power Limits**

The peak output power of a base station transmitter may not exceed 100 Watts as defined in Part 24.232

(5) **Applied voltages and currents into the final transistor elements of the transmitter output:**

In the CDMA system, the applied voltages and currents into the final transistor elements SRF7042X4 for 40 W output:

Drain	27.7 VDC
Drain Current	1.0 AMPS x 3
Gate Voltage	4 VDC

(6) **Function of Each Active Device**

Refer to the Operational Description Exhibit.

(7) **Complete Circuit Diagrams**

Refer to the Schematics Exhibit.

(8) **Instruction/Installation Manual**

Refer to the Installation Manual Exhibit.

(9) **Tune-Up/Optimization Procedure**

Refer to the Users Manual Exhibit.

(10) Means for Frequency Stabilization

Refer to Section F of the Test Report Exhibit.

The Clock Synchronization Module (CSM/CSM2) provides clock and time signals for an SC4812ET @1.9 GHz CDMA BTS. In addition, it provides the primary source, a 3 MHz clock, for the transmit synthesizer in the Broadband Transceiver. The CSM/CSM2 relies on a GPS receiver, either riding piggyback onto the CSM/CSM2 card or remotely located in an integrated package with the GPS antenna as the primary time reference for the ovenized oscillator. Two types of redundancy are provided:

1) Dual CSM/CSM2 cards provide redundancy in case of primary CSM/CSM2 failure.

2) Redundancy is also provided by either a High Stability Oscillator (HSO) or a Low Frequency Reference (LFR), such as a Loran C receiver, residing in a separate slot. The HSO is provided in case of GPS system failure.

The CSM/CSM2 uses the received signals as a reference to provide the required clock for the site. The CSM/CSM2 distributes CDMA time, a 19.6608 MHz clock, and a two second synchronization pulse every even second of universal time to the CDMA Clock Distribution (CCD) Cards .

The CSM/CSM2 is also responsible for configuration and management of the GPS and LFR systems. CSM/CSM2 software determines on a site basis what the GPS and LFR configurations should be. For future Commercial CDMA systems, GPS and LFR configuration information could optionally be downloaded to the CSM/CSM2 from the GLI2. The CSM/CSM2 is managed by the GLI2.

The High Stability Oscillator (HSO) or Low Frequency Time Reference (LFR) is used to provide a stable time reference in case of a GPS system failure or shutdown. The output of the LFR card is routed to the CSM/CSM2 cards, which derive the appropriate time references for the RF Cabinet. The current LFR is a LoranC receiver. In areas where LoranC is unavailable, the HSO may be used.

(11) Means for Attenuation of Spurious Emissions

Refer to Section C of the Test Report Exhibit.

Bandpass filters are employed in the transmit RF circuit to attenuate far out spurious emissions. The filter used here is of an air dielectric cavity resonator type.

The baseband employs a discrete L-C 7-pole elliptic filter. This filter is used to attenuate sideband noise and close in spurious emissions.

In addition, suppression of spurious radiation is obtained by proper shielding techniques.

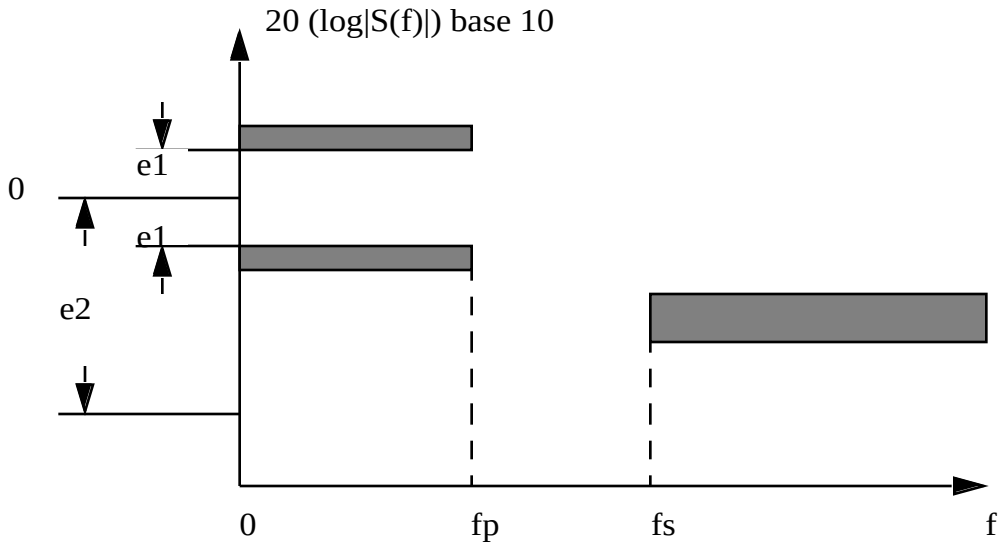
Means for Limiting Modulation

Refer to Sections B and F of the Test Report Exhibit.

In a CDMA system, the input signal (voice for example) is sampled and coded in a vocoder. This signal is then spread to 1.23 MHz by a pseudo-random spreading code. This spreading code sets the bandwidth of the spread-spectrum signal. If more than one signal is in operation (i.e. more than one voice channel), then the two signals are simply layered one atop the other within the 1.23 MHz band. So, to some extent, the bandwidth of the transmitted signal is limited by the chip rate of the PN spreading code.

Primary limiting of the CDMA signal bandwidth is accomplished by the use of a programmable digital limiter and Finite Impulse Response (FIR) filters in the BBX2. The digital limiter prevents occasional large peaks and thus avoids wrap-around error that would occur. The FIR filters are 13 Tap and run with four sets of coefficients at a 4X rate, thus being equivalent to a 48-tap linear FIR filter. Output I and Q data streams from the filters are guaranteed to be 45 dBc below the carrier at 885 kHz offset. Further filtering of the analog wave is accomplished through the use of a 7-pole elliptic filter in the BBX2. A more detailed description of the FIR filter response is given In the following graph.

The baseband filters have a linear phase. In addition, they have a frequency response S(f) that satisfies the limits shown in the figure below. The normalized frequency response of the filter shall be contained within plus or minus error (e1) in the passband and shall be less than or equal to error (e2) in the stop band (f>fs). The numerical values for the parameters are e1=1.5dB, e2=-40dB, fp=590kHz, and fs=740kHz.



BASEBAND FILTERS FREQUENCY RESPONSE LIMITS

Means for Limiting Power

The power output will be controlled by the Multi-Channel CDMA (MCC) card and the Base Band Transceiver II (BBX2). The Base Band Transceiver card (BBX2) has an automatic gain control around the transmitter lineup to maintain an output power that is within ±1dB of the input power plus required gain on the BBX2.

(12) Description of Digital Modulation Techniques

Refer to Section B of the Test Report Exhibit.

The Code Division Multiple Access (CDMA) system uses only a digital transmission mode for both the voice and data transmission. The voice vocoder rate is variable and ranges from 0.8 to 8.6 KBPS in a Rate Set 1 system, and from 1.05 to 13.35 KBPS in a Rate Set 2 system. The exact data rate chosen is based on the voice activity factor. Regardless of vocoder rate and system type, Rate Set 1 or 2, the modulation symbol rate is always 19.2 KBPS into the block interleaver and walsh function modulator on all paging and traffic channels. Encoding at 9600 bps results in a set forward traffic channel power, and at a sub-rate of 4800 bps approximately half of the forward power is effectively reduced.

The CDMA waveform is a combination of frequency division, code division, and orthogonal signal multiple access techniques. Frequency division is employed by dividing the available spectrum into nominal 1.25 MHz bandwidth channels. Code division is employed by "mixing" the data with a pseudorandom noise binary code at a rate of 1.2288 MHz. This spreads the signal over a 1.23 MHz bandwidth.

The spread signal is then encoded into two parallel bit streams referred to as I(t) and Q(t). At any time t, the vector form of I(t) and Q(t) forms a vector which can be plotted as a constellation on a graph whose abscissa and ordinate axes are scaled in terms of the magnitude of I(t) and Q(t) respectively.
Only four differential changes between any two sequential vectors are permitted. The digitally encoded I and Q waveforms from the pilot, paging, synchronizing, and traffic signals are then digitally combined and digitally filtered. These signals are then passed through a Digital to Analog converter and filtered using a 7-pole Elliptic filter with a 3 dB cutoff frequency of 630 Khz. This encoding scheme is referred to as Binary Phase Shift Keying (BPSK). These I(t) and Q(t) signals are then applied to the modulator.

Section 2.983 (e) **Standard Test Conditions**

The following conditions and procedures were followed during testing of this transmitter:

Room Temperature	+ 25 ˚C
Room Humidity	50%
DC Supply Voltage	+27 VDC (Nominal)

Prior to testing, the unit was tuned up according to the Manufacturer's Alignment Procedure. All data presented represents the worst case parameter being measured. All test data required by sections 2.985 through 2.997 can be found in Section A through F of the Test Report Exhibit.

Section 2.983 (f) **Equipment Identification**

A drawing of the equipment identification nameplate appears in the ID Label/Location Info Exhibit.

Section 2.983 (g) **Photographs**

The photographs showing external construction are in the External Photos Exhibit. The photographs showing internal construction are in the Internal Photos Exhibit.

Section 2.983 **Description of Various RF Cabinet Configurations**

The 1.9 GHz SC4812ET BTS consists of an RF Cabinet that is an outdoor, weatherized version of the 1.9 GHz SC4812T. The cabinet is powered by 27 VDC and each cabinet has the capability to support up to 4 carriers at 3 sector or 2 carriers at 6 sector. Customers may provide their own source of AC/DC rectified power or, an optional outdoor, weatherized power cabinet that provides AC/DC rectified power an battery back-up is also available. An air to air heat exchanger is used for cooling each cabinet, except in the LPA area which uses blower fans.

The RF Cabinet contains one Combined CDMA Channel Processing (C-CCP) shelf, capable of supporting up to 12 MCCx24 cards. The MCC provides signal processing functions necessary to implement various channel functions specified in the CDMA Common Air Interface specification. Channel types include sync channels, paging channels, access channels, and traffic channels. The pilot Channel is implemented on the BBX2. The MCC converts between CDMA STRAU traffic and control format and CDMA baseband format. RX inputs from the BBX2 to the MCC consist of I and Q signals from the main & diversity receive antennas. Each of the 13 BBX2 cards has its own common connection to all MCC cards. A single TX output per MCC per sector is routed to the proper BBX2. The C-CCP shelf supports up to 4 dedicated CDMA carriers at 1 to 3 sectors or up to 2 dedicated CDMA carriers at 6 sectors The C-CCP also contains control, clock, and alarm functions as required.

A fully loaded RF Cabinet supports one complete C-CCP shelf. Up to four (4) CDMA Carriers for 3 sectors and up to two carriers for 6 sectors will provide transmission. Again, the RF Cabinet is configurable in an omni, three-sector, or six-sector arrangement.

Section 2.983 **Use with Various Power Supplies**

The RF Cabinet can accommodate a DC input voltage of +27VDC. Polarity changes are accommodated in the power distribution area by feeding straight through or crossing over the primary input voltage. Circuit breakers are provided for each feed to the C-CCP shelf in the RF Cabinet. Additionally, circuit breakers are provided for fans and other components requiring direct primary input voltage.

Three Power Supply Cards installed in the C-CCP Shelf convert the input DC voltage to the necessary voltages required to power the cards in the shelf.

The power supply cards are in a N+1 redundant, load sharing configuration. This means all supplies are on line at all times. Two supplies have the capacity to power an entire shelf. With this scheme, one supply is not designated as primary or redundant, all are on line and circuitry between the supplies assures load sharing equality to within approximately 15%. Each supply has an LED to alarm a detected failure.

Section 2.987(d) Measurements Required: **Modulation Characteristics**

Refer to Section B of the Test Report Exhibit. Waveform Quality (ρ)

DEFINITION

Transmit waveform quality is the normalized correlated power between the actual waveform and the ideal waveform. The range of values for the transmit waveform quality is from 1.0, a perfect CDMA waveform, to 0.0, a non-CDMA signal. As an example, a base station with a -0.4 dB degradation in its transmit waveform would have a quality (ρ) of 10^(-0.4/10) = 0.912.

MINIMUM STANDARD

The minimum waveform quality figure for a spread-spectrum CDMA signal is -0.4 dB or 0.912 as measured with a Rho meter.

METHOD OF MEASUREMENT

Set the pilot level to 20% of the CDMA Avg. power, and transmit the pilot signal only. Connect the Rho meter directly to the transmit port. On the CDMA Rho Meter, disable the RF generator and set the tuning mode to manual. Enter the base station's RF transmit frequency and set the input attenuation to hold. Set the input attenuation to 20 dB. Now, set the DSP Analyzer test mode to continuous and chose the Rho measurement as the measurement type. Set the channel to forward and choose amplitude middle as the trigger qualifier. Set the gain to 0 dB. Set the reference frequency to 19.6608 MHz. Select internal to lock-on to the CDMA time base reference. Read the measured value for Rho on the Rho meter.

Section 2.989(c) Measurement Required: **Occupied Bandwidth**

Refer to Section E of the Test Report Exhibit.

DEFINITION

The measured spectral width of an emission. The measurement determines occupied bandwidth as the difference between upper and lower frequencies where 0.5% of the emission power is above the upper frequency and 0.5% of the emission power is below the lower frequency.

Data to show the bandwidth occupied by this transmitter and output power is presented in the form of Channel Power Measurement plots from a spectrum analyzer. The Channel Power Measurement divides the Channel Power Bandwidth into increments (defined by the Resolution Bandwidth Setting selected), then sums the energy contained in each of those increments to provide an integrated measurement of the power in the Channel Power Bandwidth.

METHOD OF MEASUREMENT

Connect a spectrum analyzer to the RF Cabinet RF Transmit Port. Set the CDMA signal power to maximum. Setup the spectrum analyzer to make the following integrated Channel Power Measurements:

1. Channel Power Measurement of the CDMA Carrier Centered at 1931.25 (Ch. 25)

Channel Power Bandwidth: 1.25 MHz

Resolution Bandwidth: 30 KHz

2. Channel Power Measurement of the CDMA Carrier Centered at 1988.75 (Ch. 1175).

Channel Power Bandwidth: 1.25 MHz

Resolution Bandwidth: 30 KHz

Record the Channel Power Measurements.

Repeat the procedure with the CDMA signal power set to Minimum level.

Section 2.991 Measurement Required: **Spurious & Harmonic Emissions at the Antenna Terminals**

Refer to Section D of the Test Report Exhibit.

DEFINITION

Conducted spurious emissions are emissions at the antenna terminals on a frequency or frequencies that are outside the authorized bandwidth of the transmitter. Reduction in the level of these spurious emissions will not affect the quality of the information being transmitted.

MINIMUM STANDARD

Per CFR 47 Part 24.238 the minimum standards for Transmit Port Conducted Spurious Emissions are as follows:

Section 24.238 (a) Emission Limits

On any frequency outside a licensee's frequency block, the power of any emission shall be attenuated below the transmitter power (P) by at least 43+10 log (P) dB.

METHOD OF MEASUREMENT

Connect a spectrum analyzer to the RF Cabinet RF Transmit Port. Measure the power level at the carrier frequency. Now, sweep the spectrum analyzer over a frequency range from 1MHz to tenth harmonic of the carrier frequency, recording all spurious emissions.

Section 2.993 Measurement Required: **Field Strength of Spurious & Harmonic Radiation**

Refer to Section C of the Test Report Exhibit.

DEFINITION

Radiated spurious and harmonic emissions are emissions from the equipment when loaded into a non-radiating load on a frequency or frequencies that are outside an occupied band sufficient to assure transmission of information with required quality for the class of communications desired. The reduction in the level of these spurious emissions will not affect the quality of the information being transmitted.

MINIMUM STANDARD

The magnitude of each spurious and harmonic emission that can be detected when the equipment is operated under the conditions specified in the alignment procedure, shall not be less than 43 + 10*log(mean output power in Watts) dB below the mean power output.

Necessary measurements were made at Motorola Inc., located at 5555 N. Beach Street, Fort Worth, Texas 76137 or at the radiation test facility located at 1605 Liberty School Rd., Azle, TX 76020.

INSTALLATION OF EQUIPMENT

The equipment under test is placed on a turntable, connected to a dummy RF load, and placed in normal operation. A receiving antenna located 3 meters from the turntable picks up any signal radiated from the transmitter and its operating accessories. The antenna is adjustable in height from 1 to 4 meters and can be horizontally or vertically polarized.

METHOD OF MEASUREMENT

The equipment is adjusted to obtain peak readings of received signals wherever they occur in the spectrum by:

1. Rotating the transmitter under test.

2. Adjusting the antenna height.

The testing procedure is repeated for both horizontal and vertical polarization of the receiving antenna. Relative signal strength is indicated on meters built into the receiver. To obtain an actual radiated signal strength, the meter reading is adjusted to correct for all affecting factors, such as antenna gain, RF gain, and cable loss. A table of correction factors vs. frequency is then used to convert a signal level measured at the receiver to the value that would be measured at the device (assuming an isotropic radiator).

Section 2.995 Measurement Required: **Frequency Stability**

Refer to Section F of the Test Report Exhibit.

DEFINITION

The carrier frequency stability is the ability of the transmitter to maintain an assigned carrier frequency.

MINIMUM STANDARD

The frequency stability shall be sufficient to ensure that the fundamental emission stays within the authorized frequency block (per CFR47 Part 24.235).

METHOD OF MEASUREMENT

Frequency measurements shall be made at the extremes of the temperature range -30 to 50 degrees Celsius and at intervals of not more than 10 degrees throughout the range. A period of time sufficient to stabilize all of the components in the equipment shall be allowed prior to each frequency measurement. Only the portion or portions of the transmitter containing the frequency determining and stabilizing circuitry need to be subjected to the temperature variation test.

Summary of Active Devices

APPLICANT: MOTOROLA **TRANSMITTER TYPE: IHET6YZ1**

Multicoupler Preselector Card (MPC6)

Device Type	Component Description	Operating Frequencies
MMPT3906LT1	Transistor PNP 40V 2A	D.C.
MMBT3904LT1	Transistor NPN 40V 2A	D.C.
MC33164D-5R2	IC Undervolt Sensing Ckt, Motorola	D.C.
MMSZ6685T	Zener Diode 3.9V 500mV, Motorola	D.C.
MMBD6050LT1	Diode 70V, 5A, Motorola	D.C.
HSMP-3800-L31	RF PIN Diode	1850-1910 MHz
PALCE22VIOH-15JC/4	IC Programmable Logic Device	D.C.
BRPG1204W-TR	Bicolor LED 70mA 2.5V	D.C.
BCW69	Transistor PNP	D.C.
CFK-0301	RF FET	1850-1910 MHz
MGA-82563	IC RF Amplifier	1850-1910 MHz
SNA-486	IC RF Amplifier	1850-1910 MHz
MMBZV6ALT1	Dual Diode Common Anode 5.6V	D.C.
MC33060ADR2	PWM Control Circuit	D.C.
MTD2955ET4	Power MOSFET Pch 60V, 12A	D.C.
MBRD340T4	Rectifier Schottky, 3A, 40V	D.C.
MC33182DR2	Low Pwr Dual Op-Amp	D.C
P6SMB12CAT3	12V Transient Suppressor	D.C.

Multicoupler Preselector Card (MPC6)
(continued)

Device Type	Component Description	Operating Frequencies
MMBD7000	Zener Diode	D.C.
RELAY_G6S_2G_DC12	DPDT 12V Relay	D.C.
MBRS140T3	Schottky Rectifier40V 1A	D.C.
LT1054IS	IC Voltage Converter with Regulator	D.C.
LM317	Adj. Voltage Regulator 500mA	D.C.
X9241	IC CMOS Quad EEPOT	D.C.
MC3303DR2	IC Gen Purpose Quad Op-Amp	D.C.
X2502D	IC EPROM 256x8	D.C.

Group Line Interface II (GLI2)

Device Type	Component Description	Operating Frequencies
MB3240T10TBDG60	DRAM 4Mx32 DIMM	40 MHz
VSA51015	32.768MHz PLL-VCXO	32.768 MHz
SG-636PCE	40MHz OSC	40 MHz
MAX732CWE	FLASH PWR SUPPLY	170 kHz
I74F776A	FUTURE BUS RX	2.048 MHz
I74F777A	FUTURE BUS TX	2.048 MHz
LTC1435CS	SWITCHER IC	230 kHz
MPC860MHzP40	MICROPROCESSOR	40MHz
MC10ELT21	PECL	3 MHz
MPC946FAR2	CLOCK DIST IC	40 MHz, 20 MHz
MC68160CFB	EEST	20 MHz
MC34058FTA	RS485 XCVR	4.096 MHz
MC74LCX16244DTR2	BUFFERS	2.048 MHz
SX05TR009ZQ01	PPC ASIC	40MHz
MT9082AP	TSI DIGITAL SWITCH	8.192 MHz
PEB2254H-V13	E1/T1 FRAMER/LIU/HDLC	8.192, 12.352 MHz, 16.384 MHz
OR2C26A-3PS208-DB	LUCENT FPGA	8.192, 16.384 MHz 20 MHz
W42C70-01G	ZERO DELAY BUFFER	16 MHz
MAX250ESD	RS232 XCVR	9600 - 19.2K BPS
MAX251ESD	9600 - 19.2K BPS	RS232 XCVR

Broadband Tranceiver Card (BBX2)
(1.9GHZ BBX2 STLG4011AA)

Digital Module

Device Type	Component Description	Operating Frequencies
XC5210	Xilinx FPGA	20 MHz
		19.6608 MHz
		1 MHz
74LCX574	Octal FlipFlop	19.6608 MHz
BRPG1204W-TR	Red/Green LED	0 - 2 Hz
MMBT3904LT1	NPN Transistor	DC
		0 - 2 Hz
74ACT02	Quad 2In NOR	20 MHz
AD9762	12Bit DAC	4.9152 MHz
AD826AR	Dual Op Amp	0 - 630 KHz
MC79M05BDTRK	5V Linear Regulator	DC
MC33269DT_3.3	3.3V Linear Regulator	DC
MC33161	Univ Voltage Ref	DC
MMSZ5237BT1	8.2V Zener Diode	DC
MC33063AD	DC to DC Converter	45 KHz
MMDF2P02HDR2	Dual P-channel FET	45 KHz
MBRS340T3	3.0A Schottky Diode	45 KHz
MC10ELT21D	PECL to TTL Converter	3 MHz
MC10H641	Octal ECL to TTL Clk Distibutor	19.6608 MHz
MC10EL16D	ECL Buffer	19.6608 MHz
MC10EL58	PECL Buffer	19.6608 MHz
MMBT3906LT1	PNP Transistor	19.6608 MHz

Broadband Tranceiver Card (BBX2)
(1.9 GHz BBX2 STLG4011AA)
(continued)

Digital Module cont.

Device Type	Component Description	Operating Frequencies
74ABT125D	BiCMOS Hex Tri-state Buffer	DC
		0.5 Hz
		4.096 MHz
ISPLSI2032	Lattice CPLD	.5Hz
		3 MHz
		19.6608 MHz
		50 MHz
SG615HC	50 MHz Crystal Oscillator	50 MHz
74HC4066	Analog Mux	3 MHz
74ACT08	Quad 2In And	DC
		20 MHz
74LCX244	Octal Tri-State Buffer	4.096 MHz
		100Hz
MBR0530T1	0.5A Schottky Diode	100Hz
MC68EN360ZP	QUICC	20 MHz
DS1232S	Reset/Watchdog	2 Hz
HSM636	20 MHz Crystal Oscillator	20 MHz
28F800CV	FLASH	20 MHz
MCM518160	DRAM	20 MHz

Broadband Tranceiver Card (BBX2)
(1.9GHZ BBX2 STLG4011AA)
(continued)

Device Type	Component Description	Operating Frequencies
SX02RH029DH01	DTC ASIC	0.5 Hz
		19.6608 MHz
		20 MHz
IDT74FCT162500ATPV	18Bit Transceiver	19.6608 MHz
MMBD7000LT1	Dual Diode	DC
LT1081IS	RS-232 Transceiver	9.6 KHz
MMSZ5243BT1	Dual 13V Zener Diode	DC

ADC Module

Device Type	Component Description	Operating Frequencies
AD9059	8 Bit ADC	9.8304 MHz
		0 - 630 KHz
MMBD201LT1	30V Hot Carrier Diode	DC

RF Control Module

Device Type	Component Description	Operating Frequencies
MMBD201LT1	30V Hot Carrier Diode	DC
AD680AR	2.5VDC Reference	DC
TLC5620	Serial Quad DAC	DC
MC145041	11in Serial ADC	0 - 630 KHz
		1 MHz

Multiple Channel CDMA (MCC-24E) Card: Issue O

Device Type	Component Description	Operating Frequencies	
SG636PH-50MHz	XTAL OSC	X2	50 MHz
SG636PFT-20MHz	XTAL OSC	X1, X3	20 MHz
MTD20N03NDLT4	N Ch FET 30V, 20A	Q1, Q2	~275 kHz
MMBT3904LT1	NPN Trans 40V .2A	Q3, Q4	DC
MBRS140T3	Schottky Diode 1A, 40V	D1, D2	~275 KHz
SY38157JU02	EMAXX-II ASIC	U100,101,200,201	19.6608 MHz
		U300,301,400,401	19.6608 MHz
		U500,501,600,601	19.6608 MHz
LTC1435CS	Switching Regulator	U38	~275 kHz
XC5204-6FQ160C	4K Gate FPGA	U64	19.6608 MHz
XC5215-6FQ160C	15K Gate FPGA	U67	4.096 MHz
XC9572-7PQ100C	1.6K Gate ISP EPLD	U8,U16	~8 MHz
XC9572-10PQ100C	1.6K Gate ISP EPLD	U50,U51	~22 MHz
DS1705ESA	Reset Controller	U3,U21,U44-U49	DC
74LCX16500MEAX	18Bit Trans Latch	U53,U54,U58,U59	19.6608 MHz
74LCX16501MEAX	18Bit Trans Latch	U63,U65,U68,U90	19.6608 MHz
MC68EN360ZP25	Comm uP with Ethernet 25 MHz	U27	
DSP56167FV60	Digital Signal Processor	U104,U204,U304	44 MHz
		U404,U504,U604	44 MHz
74ACT00D	NAND Quad 2 Input	U10	DC
74ACT02D	NOR Quad 2 Input	U17	DC
74ACT08D	AND Quad 2 Input	U2,U39,U40,U41	DC
74ACT14D	Hex Schimitt Trig	U20,U22	DC
74ACT32D	OR Quad 2 Input	U56	DC
74ACT74D	Dual FF	U1,U35,U36,U37	DC
74ACT574DW	Oct D Flip/Flop	U52	DC
74ACT541DW	Oct 3ST Line DRVR/CVR	U57	DC
74ACT05D	Hex Inverter w/Opn DRN	U13	DC

Multiple Channel CDMA (MCC-24E) Card: Issue O

(continued)

Device Type	Component Description		Operating Frequencies
MC10H641FN	PDECL-TTL 1:9 Clk Drvr	U60	19.6608 MHz
MC10EL16D	PDECL Receiver	U81,U83	19.6608 MHz
MC10EL58D	PDECL 2:1 Mux.	U82	19.6608 MHz
MC100ELT23D	PDECL to TTL Translator	U80	19.6608 MHz
MC88913D	Clk Driver	U26	50, 25 MHz
		U55	20, 10 MHz
74LCX244DT	Oct Line Driver	U66,U78,U88	4.096 MHz
74LCX86DT	QUAD EOR 2 Input	U69-77, U84-87	
MCM6226BJ15	SRAM 128Kx8	U102,103,202,203	22 MHz
		U302,303,402,403	22 MHz
		U502,503,602,603	22 MHz
MCM518165BT60	DRAM EDO 16Mx16	U5,U12	~8 MHz
74ABT125D	Quad Buffer	U31,61,62,79	DC
74FCT162501ATPV	18Bit Transceiver	U25,U30	~1.4 MHz
		U28,29,32,33,34,43	DC
74FCT162827BTPV	20Bit Buffer	U23,U24	~1.4 MHz
LXT907 APC	Ethernet Interface	U19	20.0 MHz
LT1081IS	RS232 XMTR RCVR	U9	~9.6 kHz
X25020	Serial 256x8 EEPROM	U18	DC
GAL26CV12C-7LJ	PAL	U89	19.6608 MHz
E28F008SC85	FLASH 1MX8	U6,U7,U14	~1.4 MHz

CDMA Clock Distribution (CCD) Module: Issue A or B

Device Type	Component Description	Operating Frequencies	
GAL22V10C-7LJ	PAL	U2	50 MHz
2520N-50MHz	XTAL OSC	X1	50 MHz
MMBT3904	NPN Transistor	Q1	DC
74ACT04D	Hex Inverter	U1	DC
MC10EL16D	PDECL Receiver	U5,U8,U9	DC
		U16	19.6608 MHz
MC10EL111FN	PDECL 1:9 Clk Driver	U13,U14,U15	19.6608 MHz
MC10EL23D	PDECL to TTL Translator	U6,U7,U10,U11	DC
		U12	19.6608 MHz
DS1232S	Micro Power Monitor	U4	DC
X25020	Serial 256x8 EEPROM	U3	DC

Clock Synchronization Module (CSM2)

Device Type	Component Description	Operating Frequencies
MJD243RL	Q13, Q11, Q10, Q9, Q8, Q1	3 MHz
MJD2955T4	Q15	D.C.
MMFT3055V	Q17, Q18	307.2 KHz
MMBT3904	Q19, Q14, Q12, Q7, Q5, Q4, Q2	D.C.
MMBT3906	Q6, Q3	D.C.
MMBT3906	Q16	307.2 KHz
74ACT14D	U1	0.5 Hz
74ACT14D	U75, U66, U65, U37	1 Hz
MC14538B	U10	D.C.
IDT71024S15TY	U82, U81, U12, U11	16 MHz
74ACT00D	U13	19.6608 MHz
74ACT00D	U60	D.C.
AM29F040	U15, U14	16 MHz
AD817AR	U16	19.6608 MHz, 3 MHz
74ACT245DW	U19, U17	1 Hz
AD9850	U18	19.6608 MHz
MC68302FC	U2	16 MHz
XC5206-160	U20	307.2 KHz, 19.6608 MHz, 10 MHz
AD7846JP	U24	1 Hz
MC10ELT21D	U25	10 MHz
MC78M12	U26, U53	D.C.
MC10E1651FN	U27	19.6608 MHz
LM317D	U28	D.C.
MC78M15CDTRK	U29	D.C.
LT1081IS	U3	130 KHz
MC79M15CDT	U30	D.C.
MC100ELT23D	U31	19.6608 MHz
MC100ELT23D	U73, U72	D.C.

Clock Synchronization Module (CSM2)

(continued)

Device Type	Component Description	Operating Frequencies
MC100ELT23D	U36, U35	19.6608 MHz
MC100ELT23D	U78, U77	3 MHz
LT1054IS	U32	25 kHz
MC10EL16D	U33	19.6608 MHz
GAL22V10B-7LJ	U34	50 MHz
74ACT74D	U38	9.8304 MHz
X25020	U4	D.C.
78ST305HC	U40	1 MHz
10H20EV8	U41	50 MHz
MC10EL07D	U49, U43	19.6608 MHz
MC10EL51D	U52, U50, U45, U44	D.C.
MC10EL51D	U55	0.5 Hz
MC10EL31D	U56, U51, U46	D.C.
75175D	U74, U59	8000 Hz
75175D	U76, U47	4800 Hz
75175D	U79	9600 Hz
MC10EL04D	U57, U48	D.C.
74ACT05D	U5	D.C.
75172BDW	U67, U54	4800 Hz
75172BDW	U71	0.5 Hz
MC10EL16D	U62, U61, U58	D.C.
MC10EL16D	U63	19.6608 MHz
MC10EL16D	U64	D.C.
DS1232S	U6	D.C.
MC10EL111FN	U68	0.5 Hz
MC10EL111FN	U69	D.C.
MC10EL111FN	U70	19.6608 MHz

Clock Synchronization Module (CSM2)

(continued)

Device Type	Component Description	Operating Frequencies
MC68681FN	U7	4 MHz, 9600 Hz
74ACT32D	U8	16 MHz
MC34025	U83	307.2 MHz
78M05	U84	D.C.
74ACT04D	U9	16 MHz
MA505-16MHz	Y1	16.0 MHz
19.6608 MHz VCXO	Y2	19.6608 MHz
SG615H-50MHz	Y3	50 MHz

Switchboard 1900 MHz (STLG4009A)

Device Type	Component Description	Operating Frequencies
MMBZ5231BL	5.1V Zener Voltage Regulator Diode	DC
MMBT3904	NPN Transist	DC
MC33161	Universal Voltage Monitor	DC
MC33063	Switching Regulator	40 kHz
MMDF2P02HD	P-Channel MOSFET	40 kHz
MBRS340T3	Schottky Power Rectifier (1A)	40 kHz
MIC2920A-5.0BS	Low-Dropout Voltage Regulator (0.4A)	DC
MIC2940A	Low-Dropout Voltage Regulator (1.25A)	DC
MIC5205-3.3BM5	Low-Dropout Voltage Regulator (150mA)	DC
MIC2941ABU	Low-Dropout Variable Voltage Regulator (200mA)	DC
MBR0530T1	Schottky Power Rectifier (0.5A)	DC
74LCX244	Low-Voltage CMOS Octal Buffer	DC
MMBD7000	Dual Switching Diode	DC
pLSI2032	Programmable Logic Device	DC
25020	Serial E^2PROM	100 kHz
74ACT04	Hex Inverter	DC
74ACT00	Hex NAND Gate	DC
BRPG1204	Red-Green LED	DC
LM2901	Quad Comparator	DC
HMC182S14	GaAs SP4T Terminated Switch	1800 - 2000 MHz
SW338	GaAs SPDT Terminated Switch	1800 - 2000 MHz
HMC183QS24	GaAs SP8T Terminated Switch	1800 - 2000 MHz
SW419	GaAs SP4T Terminated Switch	1800 - 2000 MHz
SNA-486	GaAs FET MMIC (100mA) RF Amplifier	1900 - 2000 MHz

High Stability Oscillator (HSO)

Device Type	Component Description	Operating Frequencies
SN74AC240DW	LINE DRIVER	1 HZ
X2502OS	EEPROM	9.6 kHz
DS3695AM	RS485 DRIVER	1 HZ
FE5680A	Rb MODULE	500 HZ 8.388608 MHz 38 MHz 50.255 MHz 100.51 MHz 6.8 GHZ