SPECIFICATION OF TRANSMITTER

MODEL : SYSTEM-X FLASH-5

1. FREQUNCY : 72MHZ BAND
2. FREQUNCY : fo+1KHZ +/- 300HZ at CENTER X-TAL & 9.6VOLT
   fo+1KHZ +/- 1KHZ at USEABLE X-TAL & NICID BATTERY
3. MODULATION : FM NEG 2.8KHZ+/-0.3KHZ
4. NO OF CHANNEL : 5 CHANNEL
5. OUTPUT IMPEDANCE : WHIP ANTENNA
6. RF POWER : 300mW +/- 50mW at 9.6VOLT
7. SUPREOUS POWER : -54dB
8. RF BAND WIDTH : 55dB at +/-10KHZ
9. CURRENT DRAIN : 180mA +/- 20mA at 9.6VOLT
10. FRAME TIME : 20.7mS +/- 2mS
11. CHANNEL CENTER : 1.5mS +/- 20uS
12. REVERSE CENTER : 20uS
13. CHANNEL FLOAT TORANCE : 7uS
14. CHANNEL RETURN TORANCE : 7uS
15. RF FLOATING : 7uS
16. WORRYING LOW VOLTAGE : 9.2 VOLT
17. CHANNEL RANGE

	CH-1,2,4	CH-3	CH-5
TICK HIGH	1.88mS +/- 0.02mS	1.88mS +/- 0.02mS	1.12mS +/- 0.02mS
STICK CENTER	1.50mS +/- 0.02mS		
STICK LOW	1.12mS +/- 0.02mS	1.12mS +/- 0.02mS	1.88uS +/- 0.02mS
TRIM(TOTAL)	0.30mS +/- 0.02mS	0.20mS +/- 0.02mS	

Ordering number : EN4411

SANYO

No.4411

2SC4910

NPN Epitaxial Planar Silicon Transistor

VHF-Band Power Amp Applications

Features

- On-chip emitter ballast resistors.

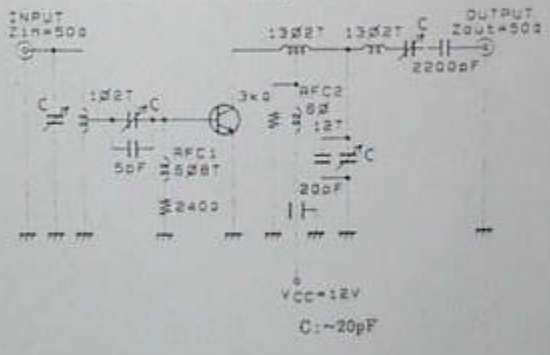
Absolute Maximum Ratings at Ta = 25°C

			unit
Collector-to-Base Voltage	V_{CBO}	38	V
Collector-to-Emitter Voltage	V_{CEO}	18	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	0.75	A
Collector Current (Pulse)	I_{CP}	1.2	A
Base Current	I_B	150	mA
Collector Dissipation	P_C	1.5	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 to +150	°C

Electrical Characteristics at Ta = 25°C

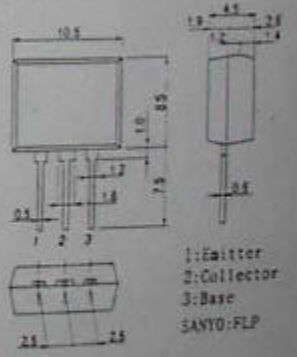
			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	V_{CB} = 30V, I_E = 0			50	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 2V, I_C = 0			50	μA
DC Current Gain	h_{FE}	V_{CE} = 10V, I_C = 200mA	20		200	
C-B Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	38			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	18			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0	3			V
Output Capacitance	Cob	V_{CB} = 10V, f = 1MHz		6	10	pF
Output Power	P_O	V_{CC} = 12V, f = 175MHz, P_{IN} = 50mW	0.7	0.9		W
Collector Efficiency	ηc	See specified Test Circuit.	55	70		%

Collector Efficiency Test Circuit

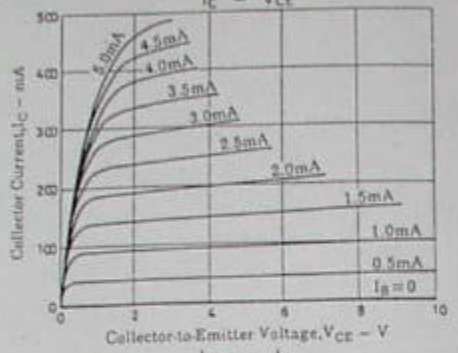


Package Dimensions 2084B

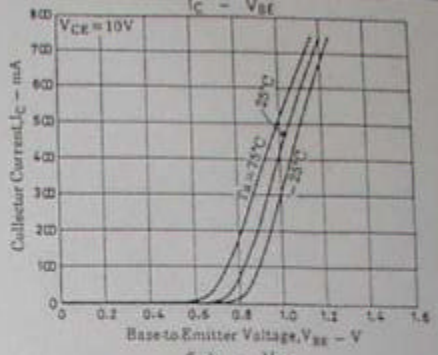
(unit:mm)



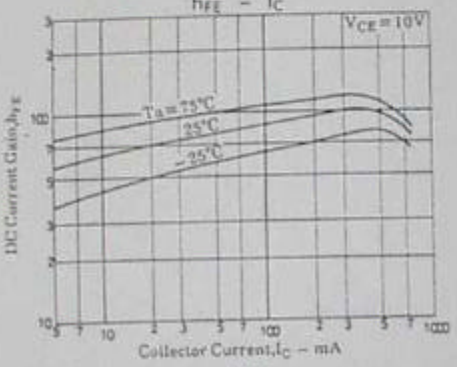
$I_C - V_{CE}$



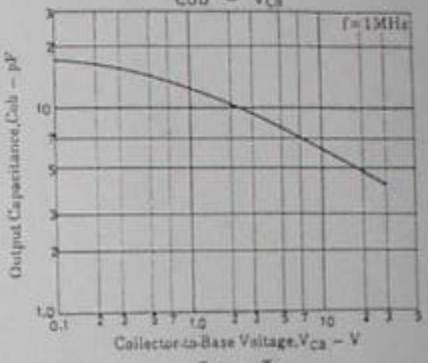
$I_C - V_{BE}$



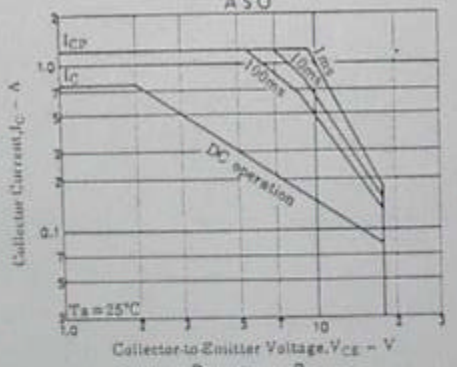
$h_{FE} - I_C$



Cob – V_{CB}

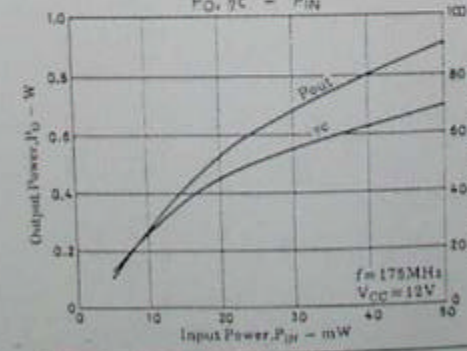


ASO

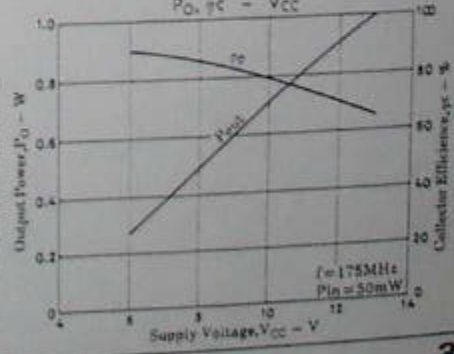


$P_C - Ta$

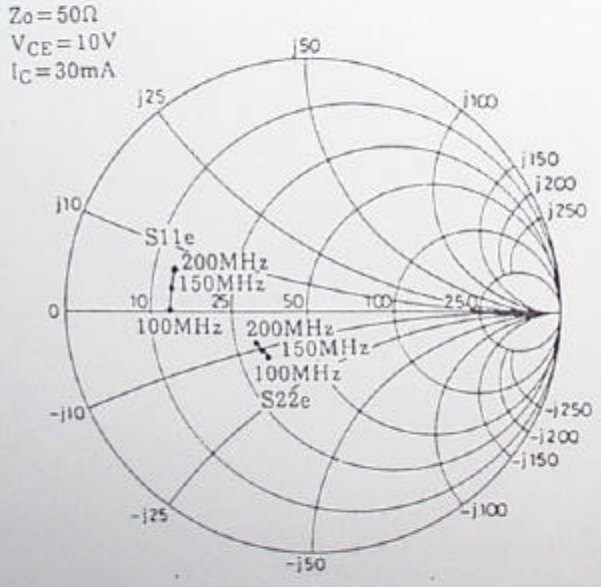
$P_O, \eta C - P_{IN}$



$P_O, \eta C - V_{CC}$



S Parameter


Zo = 50Ω
VCE = 10V
IC = 30mA
j50
j25
j100
j150
j200
j250
j10
S11e
200MHz
150MHz
100MHz
10
25
50
100
250
0
200MHz
150MHz
100MHz
S22e
-j10
-j250
-j200
-j150
-j25
-j100
-j50

KEC
KOREA ELECTRONICS CO.,LTD.

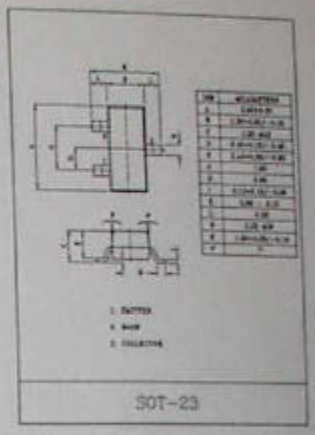
SEMICONDUCTOR
TECHNICAL DATA

KRC110S ~ KRC114S

EPITAXIAL PLANAR NPN TRANSISTOR

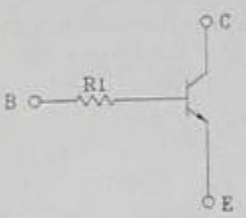
SWITCHING APPLICATION.
INTERFACE CIRCUIT AND DRIVER CIRCUIT APPLICATION.

FEATURES
- With Built-in Bias Resistors.
- Simplify Circuit Design.
- Reduce a Quantity of Parts and Manufacturing Process.



SOT-23

EQUIVALENT CIRCUIT



MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector Power Dissipation	P_C	200	mW
Junction Temperature	T_j	150	℃
Storage Temperature Range	T_{stg}	-55~150	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	V_{CB}=50V, I_E=0	-	-	100	nA
Emitter Cut-off Current		I_{EBO}	V_{EB}=5V, I_C=0	-	-	100	nA
DC Current Gain		h_{FE}	V_{CE}=5V, I_C=1mA	120	-	-	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=10mA, I_B=0.5mA	-	0.1	0.3	V
Transition Frequency		f_T *	V_{CE}=10V, I_C=5mA	-	250	-	MHz
Input Resistor	KRC110S	R_1		-	4.7	-	kΩ
	KRC111S			-	10	-	
	KRC112S			-	100	-	
	KRC113S			-	22	-	
	KRC114S			-	47	-	

Note : * Characteristic of Transistor Only

MARK SPEC

TYPE	KRC110S	KRC111S	KRC112S	KRC113S	KRC114S
MARK	NK	NM	NN	NO	NP

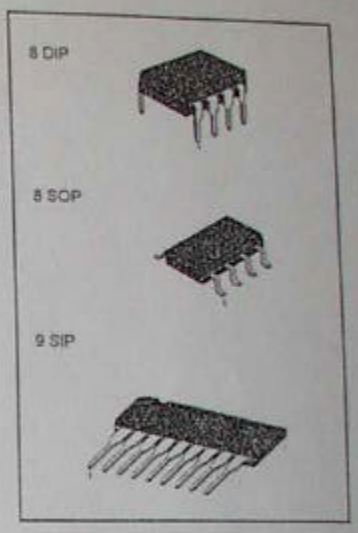
1994. 3. 22 Revision No : 0 KEC

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC			SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Switching Time	Rise Time	KRC110S	t_r	V_O=5V V_{IN}=5V R_L=1kΩ	-	0.025	-	μS
		KRC111S			-	0.03	-	
		KRC112S			-	0.3	-	
		KRC113S			-	0.06	-	
		KRC114S			-	0.11		
	Storage Time	KRC110S	t_{stg}		-	3.0	-	
		KRC111S			-	2.0	-	
		KRC112S			-	6.0	-	
		KRC113S			-	4.0	-	
		KRC114S			-	5.0	-	
	Fall Time	KRC110S	t_f		-	0.2	-	
		KRC111S			-	0.12	-	
		KRC112S			-	2.0	-	
		KRC113S			-	0.9	-	
		KRC114S			-	1.4	-	

DUAL OPERATIONAL AMPLIFIERS

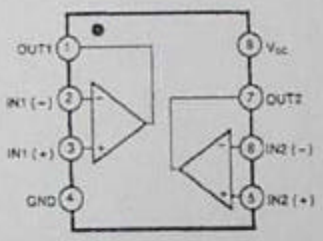
The KA258 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.
Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power Supply voltage.
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power Supply systems.

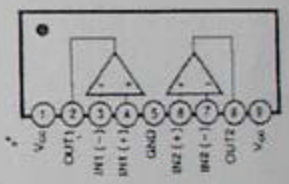


FEATURES

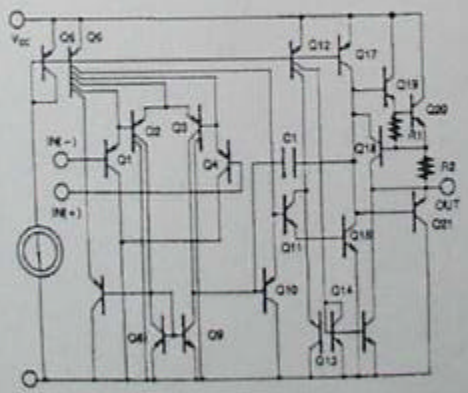
- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: KA258/A, KA358/A: 3V~32V
  (or ±1.5V~i6V)
  KA2004: 3V~26V (or ±1.5V II3V)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to Vcc - 1.5V DC
- Power drain suitable for battery operation.

BLOCK DIAGRAM





SCHEMATIC DIAGRAM (One section only)



ORDERING INFORMATION

Device	Package	Operating Temperature
KA358 KA358A	8 DIP	0 ~ + 70℃
KA358S KA358AS	9 SIP	
KA358D KA358AD	8 SOP	
KA258 KA258A	8 DIP	-25 ~ + 85℃
KA258S KA258AS	9 SIP	
KA258D KA258AD	8 SOP	
KA2904	8 DIP	-40 ~ + 85℃
KA2904S	9 SIP	
KA2904D	8 SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	KA258/KA258A	KA358/KA358A	KA2904	Unit
Supply Voltage	V_{CC}	± 16 or 32	± 16 or 32	± 13or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	± 32	± 32	± 26	V
Input Voltage	V_I	-0.3 to +32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND ($V_{CC} \leq V$, T_A = 25℃(One Amp))		Continuous	Continuous	Continuous	
Operating Temperature Range	T_{OPR}	-25 ~ + 85	0 ~ + 70	-40 ~ + 85	℃
Storage Temperature Range	T_{STG}	-65 ~ + 150	-65 ~ + 150	-65 ~ + 150	℃

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, T = 25℃, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA258			KA358			KA2904			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} -1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω			2.9	5.0		2.9	7.0		2.9	7.0	mV
Input Offset Current	I_{IO}				3	30		5	50		5	50	nA
Input Bias Current	I_{BIAS}				45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V (KA2904, V_{CC} = 26V)		0		Vcc -1.5	0		Vcc -1.5	0		Vcc -1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V (KA2902, V_{CC} = 26V)			0.8	2.0		0.8	2.0		0.8	2.0	mA
		R_L = ∞ ,over full temperature range			0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, $R_L \geq 2K\Omega$ $V_{O(P)}$ = 1V to 11V		*50	100		25	100		25	100		V/mV
Output Voltage Swing	V_{OPH}	V_{CC} = 30V	R_L = 2KΩ	26			26			22			V
	V_{OPH}	V_{CC} = 26V for 2904	R_L = 10KΩ	27	28		27	28		23	24		V
	V_{OPL}	V_{CC} = 5V, $R_L \geq 10K\Omega$			5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	80		50	80		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120			120		dB
Short Circuit to GND	I_{SC}				40	60		40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		10	30		10	30		10	30		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V		10	15		10	15		10	15		mA
		$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 200mA		12	100		12	100					μA
Differential Input Voltage	$V_{I(DIFF)}$					Vcc			Vcc			Vcc	V

ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, V_{EE}=GND, unless otherwise specified)
The following specification apply over the range of - 25℃ ≤ T_A ≤ + 85℃ for the KA258; and the 0℃ ≤ T_A ≤ + 70℃ for the KA358; and the -40℃ ≤ T_A ≤ +85℃ for the KA2904

Characteristic	Symbol	Test Conditions	KA258			KA358			KA2904			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω			7.0			9.0			10.0	mV
Input Offset Voltage Drift	V_{IO}	R_S = 0Ω		7.0			7.0			7.0		μV/℃
Input Offset Current	I_{IO}				100			150		45	200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$			10			10			10		pA/℃
Input Bias Current	I_{BIAS}			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V (KA2904,V_{CC} = 26V)	0		Vcc -2.0	0		Vcc -2.0	0		Vcc -2.0	V
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L ≥ 2.0KΩ $V_{O(P)}$ = 1V to 11V	25			15			15			V/mV
Output Voltage Swing	V_{OPH}	V_{CC} = 30V R_L = 2KΩ	26			26			26			V
		V_{CC} = 26V for 2904 R_L = 10KΩ	27	28		27	28		27	28		V
	V_{OL}	V_{CC} = 5V, R_L ≥ 10KΩ		5	20		5	20		5	100	mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30		10	30		10	30		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V	5	8		5	9		5	9		mA
Differential Input Voltage	$V_{I(DIFF)}$				Vcc			Vcc			Vcc	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE}=GND, T_A=25℃, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA258A			KA358A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} - 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω		1.0	3.0		2.0	3.0	mV
Input Offset Current	I_{IO}			2	15		5	30	nA
Input Bias Current	I_{BIAS}			40	80		45	100	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V		0.8	2.0		0.8	2.0	mA
		RL = ∞, over full temperature range		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L ≥ 2KΩ V_O = 1V to 11V	50	100		25	100		V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V, R_L = 2KΩ	26			26			V
		V_{CC} = 26V for 2904, R_L = 10KΩ	27	28		27	28		V
	V_{OL}	V_{CC} = 5V, R_L ≥ 10KΩ		5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I_{SC}			40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	20	30		20	30		mA
	I_{SINK}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	15		10	15		mA
		$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V $V_{O(P)}$ = 200mV	12	100		12	100		μA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)

The following specification apply over the range of -25℃ ≤ T_A ≤ +85℃ for the KA258A, and the 0℃ ≤ T_A ≤ +70℃ for the KA358A

Characteristic	Symbol	Test Conditions	KA258A			KA358A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω			4.0			5.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$			7.0	15		7.0	20	μV/℃
Input Offset Current	I_{IO}				30			75	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$			10	200		10	300	pA/℃
Input Bias Current	I_{BIAS}			40	100		40	200	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2KΩ	26			26			V
		V_{CC} = 30V, R_L = 10KΩ	27	28		27	28		V
	$V_{O(L)}$	V_{CC} = 5V, R_L ≥ 10KΩ		5	20		5	20	mV
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L ≥ 2.0KΩ $V_{O(P)}$ = 1V to 11V	25			15			V/mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30		10	30		mA
	I_{SINK}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	5	9		5	9		mA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}	V

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

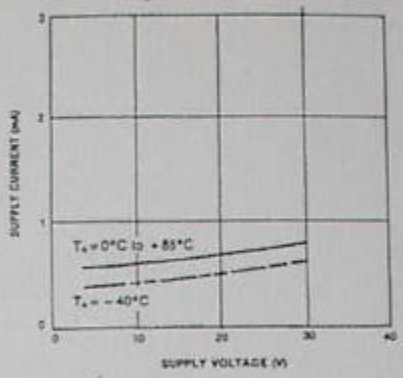


Fig. 2 VOLTAGE GAIN

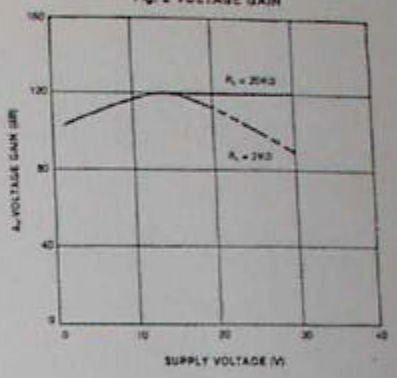


Fig. 3 OPEN LOOP FREQUENCY RESPONSE

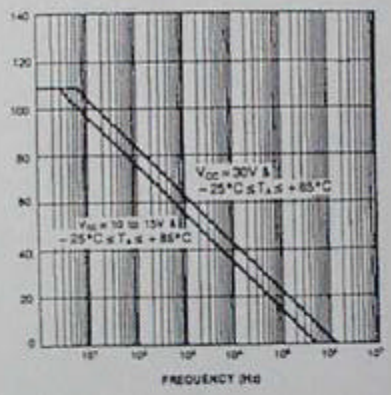


Fig. 4 LARGE SIGNAL FREQUENCY

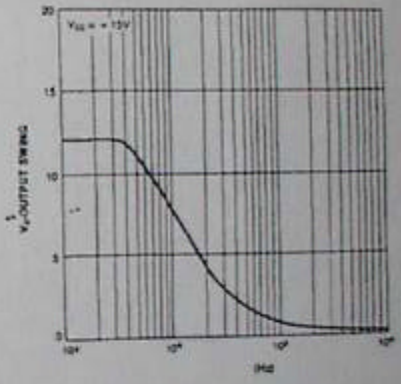


Fig. 5 OUTPUT CHARACTERISTICS
CURRENT SOURCING

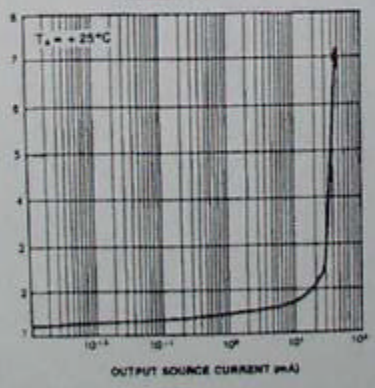


Fig. 6 OUTPUT CHARACTERISTICS
CURRENT SINKING

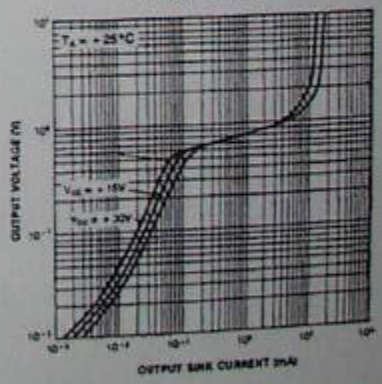


Fig. 7 INPUT VOLTAGE RANGE

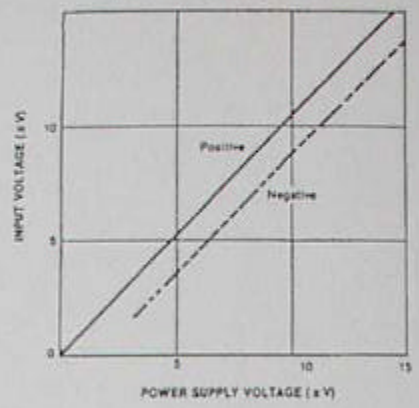


Fig. 8 COMMON-MODE REJECTION RATIO

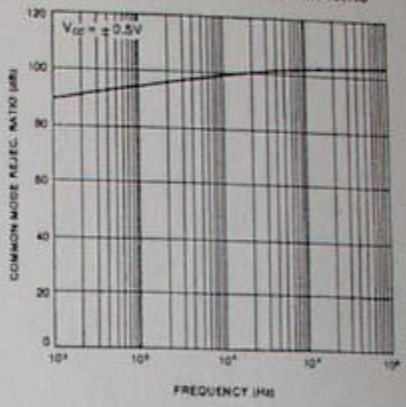


Fig. 9 CURRENT LIMITING

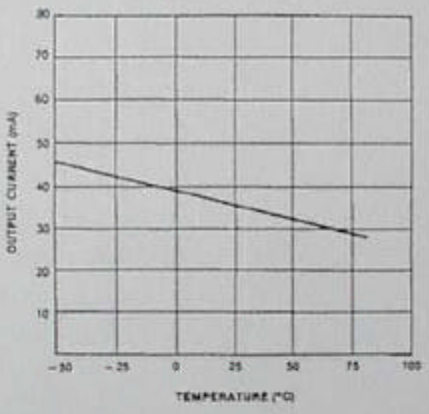


Fig. 10 INPUT CURRENT

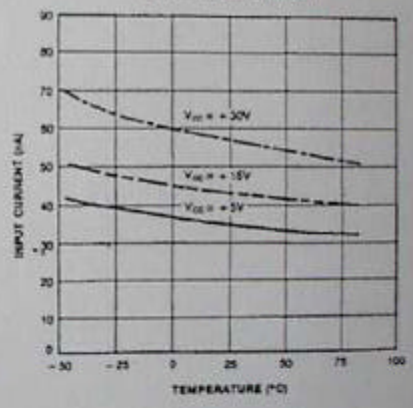


Fig. 11 VOLTAGE FOLLOWER PULSE RESPONSE

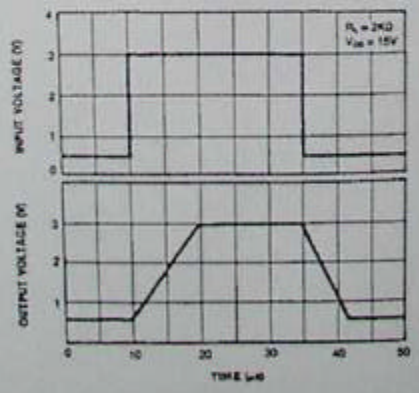
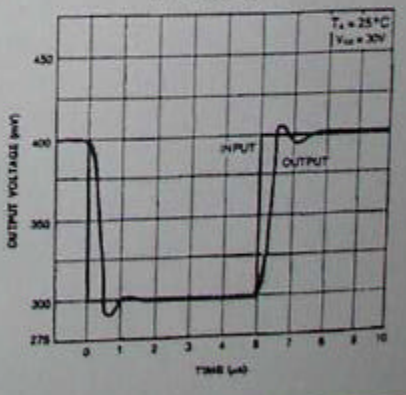


Fig. 12 VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



OKI semiconductor

MSM65512/65P512

OKI ORIGINAL HIGH PERFORMANCE CMOS 8 BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

MSM65512 is a high-performance 8-bit single-chip controller that employs Oki's original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65512 is capable of high-speed processing, and includes 8 Kbytes of program memory, 256 bytes of data memory, timers and serial ports on chip. Also available is the MSM65P512, which replaces the on-chip program memory with one-time PROM.

OPERATING RANGE

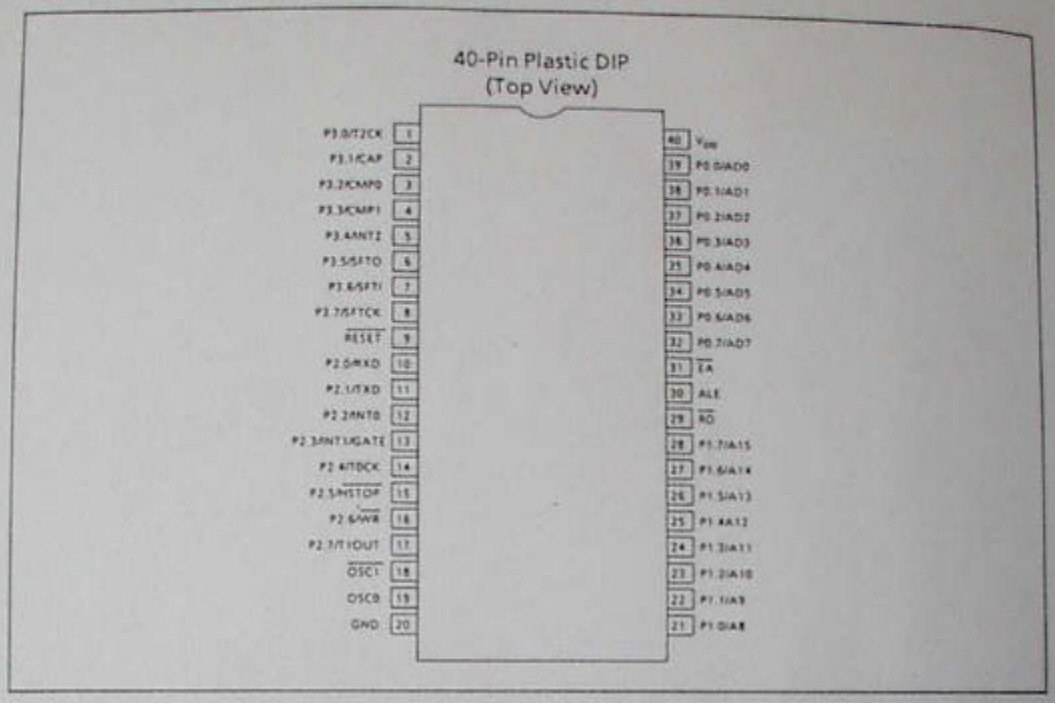
- Operating Frequency : DC ~ 10 MHz
- Operating Voltage : 4.5 ~ 5.5 V
- Operating Temperature : -40 ~ 85°C (MSM65512)

FEATURES

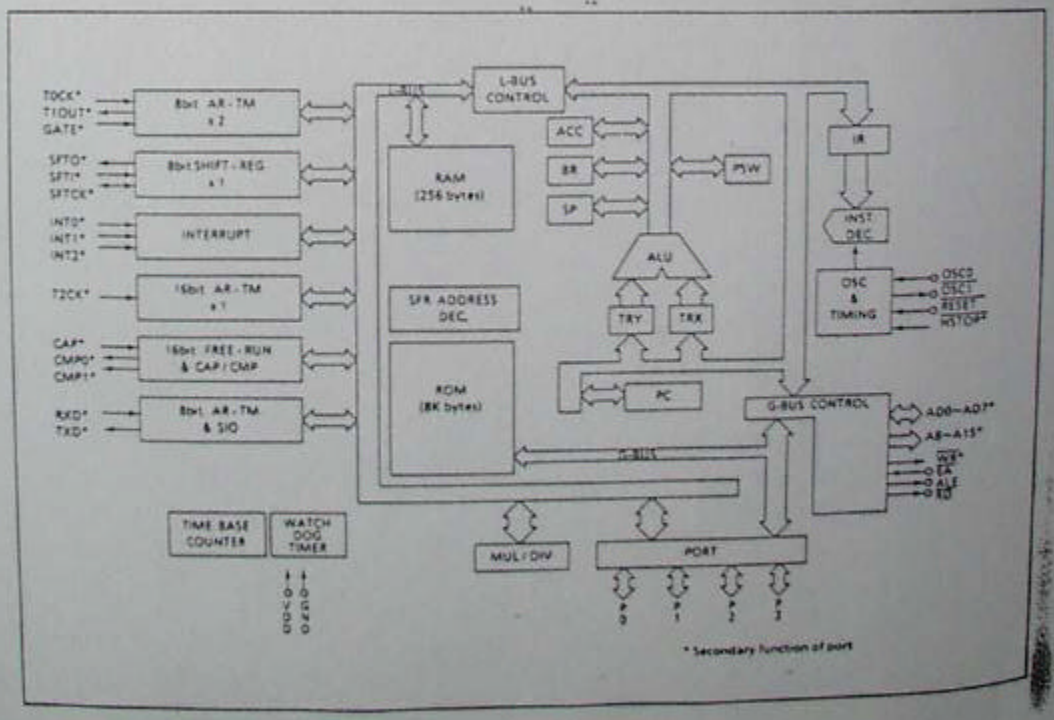
- Memory Space : 64 Kbytes
  - On-Chip Program Memory : 8 Kbytes
  - On-Chip Data Memory : 256 bytes
- Minimum Instruction Execution Cycle: 400nS @ 10 MHz
- Powerful instruction set:
  - 83 basic instructions
  - 8/16-bit operation instructions
  - Bit manipulation instructions
  - Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions
  - 16 ← 8 x 8
  - 16 ← 16/8, 8 ← 16 mod 8
- I/O ports: 8-bit x 4
- Timers
  - 8-bit auto-reload timer x 2
  - 16-bit auto-reload timer x 1
  - Watchdog timer x 1
- Counters
  - Time base counter x 1
  - 16-bit free-running counter x 1
- Capture input: 1 channel
- Compare output: 2 channels
- Serial ports
  - Shift register x 1
  - Serial port with baud rate generator (UART/synchronous) x 1
- External interrupts: 3
- Interrupt factors: 15
- Package:
  - 40 pin plastic DIP (DIP40-P-600)
  - 44 pin plastic QFP (T.B.D)
  - 44 pin PLCC (QFJ44-P-S650)
  - 64 pin plastic QFP (T.B.D)

- Specifications are subject to change without notice.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



3-Wire Serial CMOS E^2PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 V (V_{CC} = 4.5 V to 5.5 V)
  - 3.0 V (V_{CC} = 2.7 V to 5.5 V)
  - 2.5 V (V_{CC} = 2.5 V to 5.5 V)
  - 2.0 V (V_{CC} = 1.8 V to 5.5 V)
- User Selectable Internal Organization
  - 1K: 128 x 8 or 64 x 16
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- Three-Wire Serial Interface
- Self-Timed Write Cycle (10 ms Max)
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- Eight-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages

Description

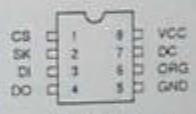
The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial E^2PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of eight bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/57/66 is available in space saving eight-pin PDIP and eight-pin JEDEC and EIAJ SOIC packages.

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

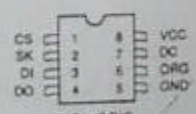
Atmel's E^2PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT93C46/56/57/66 is available in 5.0 V ± 10%, 2.7 V to 5.5 V, 2.5 V to 5.5 V, and 1.8 V to 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect

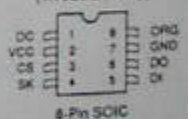


8-Pin PDIP



8-Pin SOIC

Rotated (R)
(1K JEDEC Only)



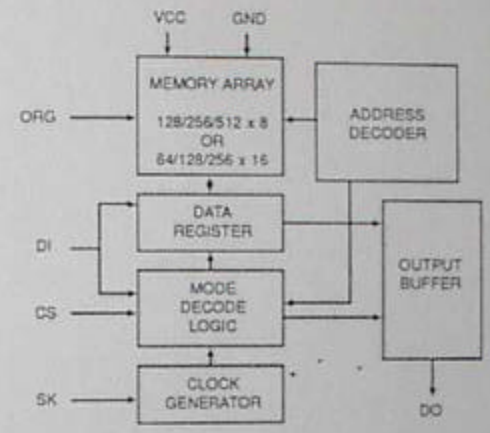
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

LOW FREQUENCY AMPLIFIER

- Complement to KSC1623
- Collector-Base Voltage V_{CBO}= -60V

SOT-23

1. Base 2. Emitter 3. Collector

ABSOLUTE MAXIMUM RATINGS (T_A=25℃)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-60	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-100	mA
Collector Dissipation	P_C	150	mW
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ 150	℃

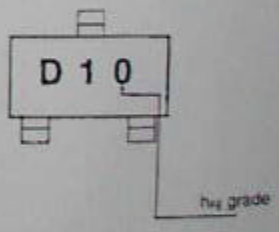
ELECTRICAL CHARACTERISTICS (T_A=25℃)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector Cut-off Current	I_{CBO}	V_{CB}= -60V, I_E=0			-0.1	μA
Emitter Cut-off Current	I_{EBO}	V_{EB}= -5V, I_C=0			-0.1	μA
DC Current Gain	h_{FE}	V_{CE}= -6V, I_C= -1mA	90	200	600	
Collector-Emitter Saturation Voltage	V_{CE} (sat)	I_C= -100mA, I_B= -10mA		-0.18	-0.3	V
Base-Emitter On Voltage	V_{BE} (on)	I_C= -1mA, V_{CE}= -6V	-0.55	-0.62	-0.65	V
Current-Gain-Bandwidth Product	f_T	I_C= -10mA, V_{CE}= -6V		180		MHz
Output Capacitance	C_{OB}	V_{CB}= -10V, I_E=0 f=1MHz		4.5		pF

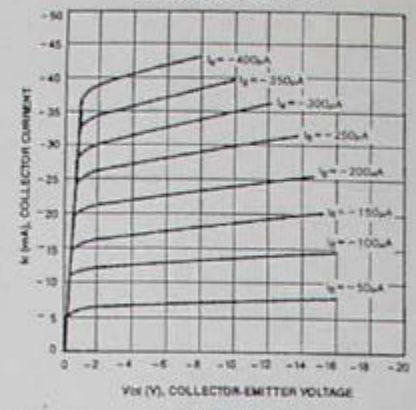
h_{FE} CLASSIFICATION

Classification	O	Y	G	L
h_{FE}	90-180	135-270	200-400	300-600

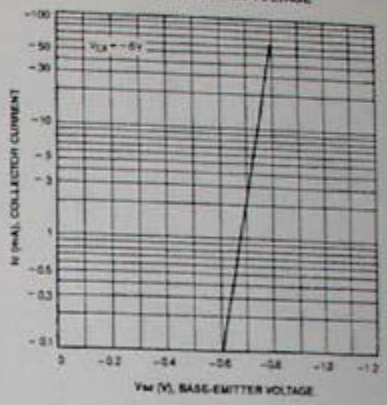
Marking



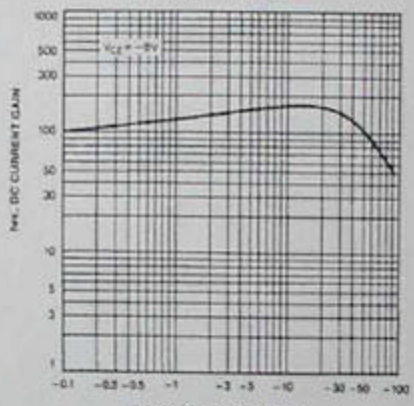
STATIC CHARACTERISTIC



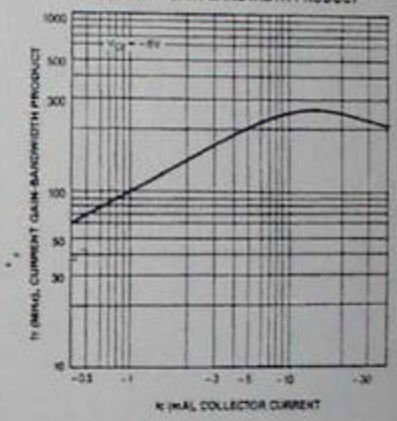
BASE-EMITTER ON VOLTAGE



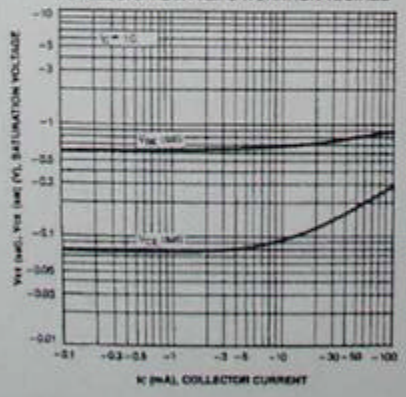
DC CURRENT GAIN



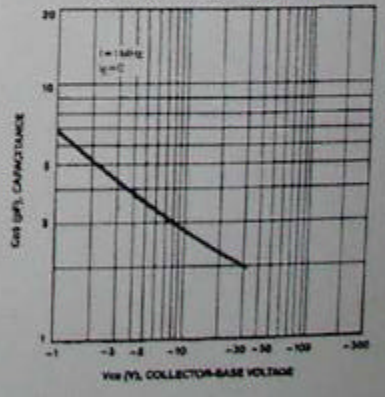
CURRENT GAIN-BANDWIDTH PRODUCT



BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



COLLECTOR OUTPUT CAPACITANCE



GD4051B

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 4051B is an 8-Channel Analog Multiplexer/Demultiplexer with three Address Inputs (A_0–A_2), an active LOW Enable Input ($\overline{E}$), eight independent Inputs/Outputs (Y_0–Y_7) and a Common Input/Output (Z).

The 4051B contains eight bidirectional analog switches, each with one side connected to an independent Input/Output (Y_0–Y_7) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance, ON state) by the three Address Inputs (A_0–A_2). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

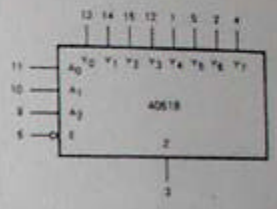
V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0–A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0–Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER
- COMMON ENABLE INPUT (ACTIVE LOW)

PIN NAMES

Y_0–Y_7	Independent Inputs/Outputs
A_0–A_2	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Common Input/Output

LOGIC SYMBOL



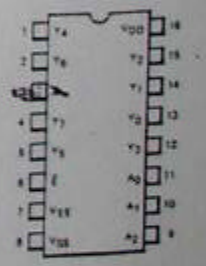
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

TRUTH TABLE

INPUTS				CHANNELS							
$\overline{E}$	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

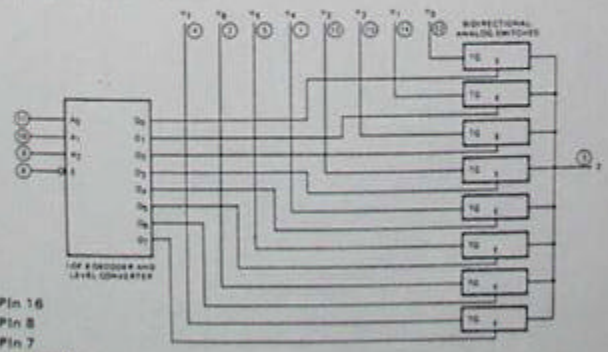
L = LOW Level
H = HIGH Level
X = Don't Care

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram as the Dual In-line Package.

4051B FUNCTIONAL LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	V_{is} = V_{DD} to V_{EE} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	E = V_{DD} V_{SS} = V_{DD}/2 V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						E = V_{SS} = V_{DD}/2 V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	μA	MIN, 25°C	V_{SS} = V_{EE} All inputs at V_{DD} or V_{EE}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		25			10			6		ns	C_L = 50 pF, R_L = 200 kΩ
t_{PHL}	Input to Output		10			6			4			$\overline{E}$ = V_{SS} = V_{EE},
t_{PLH}	Propagation Delay,		170			95			80		ns	A_n or V_{is} = V_{DD} or V_{EE}
t_{PHL}	Address to Output		210			125			95			Note 5
t_{PZL}	Output Enable Time		185			95			75		ns	C_L = 50 pF, R_L = 1 kΩ
t_{PZH}			205			105			85			E or A_n = V_{SS} = V_{EE}
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	V_{is} = V_{DD} or V_{EE}
t_{PHZ}			1240			1120			1070			Note 5
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ V_{SS} = $V_{DD}/2$, $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) p-p f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) p-p at -40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) p-p V_{SS} = $V_{DD}/2$ 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS} R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD}/2$.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns, R_L = 10 kΩ.
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 4, 5, 12, 13, 14, or 15 the voltage drop across the bidirectional switch must not exceed 0.5 V at T_A ≤ 25°C, or 0.3 V at T_A > 25°C. No V_{DD} current will flow through R_L if the switch current flows into terminal 3.

GD4066B

QUAD BILATERAL SWITCHES

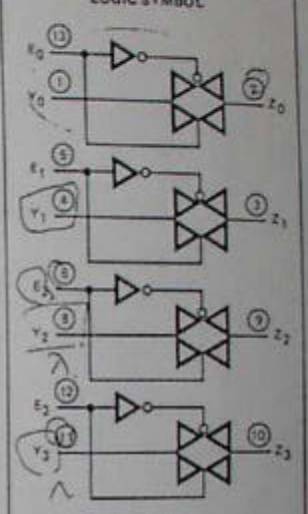
DESCRIPTION — The 4066B has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- DIGITAL OR ANALOG SIGNAL SWITCHING
- INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)

PIN NAMES

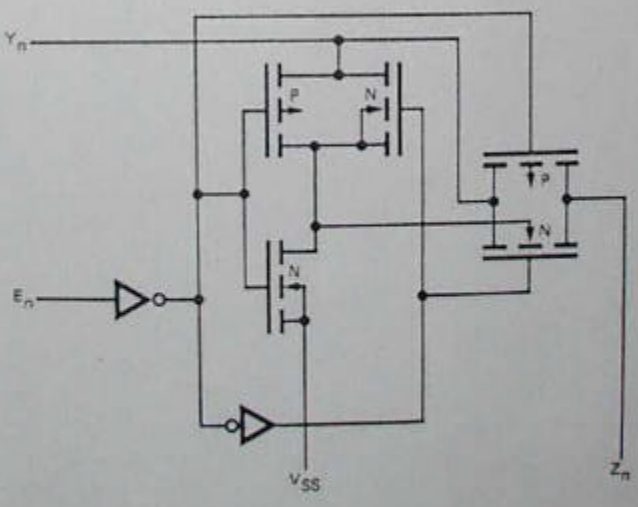
E_0–E_3	Enable Inputs
Y_0–Y_3	Input/Output Terminals
Z_0–Z_3	Input/Output Terminals

LOGIC SYMBOL

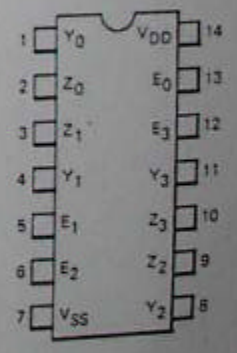


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A 4066B)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250	Ω	MIN	E_n = V_{DD} R_L = 10 kΩ to $V_{DD}/2$ V_{is} = V_{DD} to V_{SS}
				270	1000		120	500		80	280		25°C	
				330	1090		170	520		130	300		MAX	
		XM		160	850		85	400		60	220	Ω	MIN.	
				270	1000		120	500		80	280		25°C	
				360	1150		190	550		145	320		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	E_n = V_{DD} R_L = 10 kΩ to $V_{DD}/2$ V_{is} = V_{DD} or V_{SS}
I_Z	OFF State Leakage Current	XC									±300	nA	MIN, 25°C	E_n = V_{SS} V_{is} = V_{DD} or V_{SS} V_{os} = V_{SS} or V_{DD}
											±1000		MAX	
		XM									±100		MIN, 25°C	
											±1000		MAX	
I_{DD}	Quiescent Power Supply Dissipation	XC			1			2			4	µA	MIN, 25°C	All inputs at V_{DD} or V_{SS}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	µA	MIN, 25°C	
					7.5			15			30		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8	45 45		3 4	30 30		2 2	20 20	ns	C_L = 50 pF, R_L = 200 Ω to V_{SS} Input Transition Times ≤ 20 ns E_n = V_{DD} V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32	125 125		16 16	60 60		13 13	50 50	ns	C_L = 50 pF, R_L = 1 kΩ to V_{SS} or V_{DD} E_n = V_{DD} (square wave) Input Transition Times ≤ 20 ns V_{is} = V_{DD} or V_{SS}
t_{PLZ} t_{PHZ}	Output Disable Time		360 360			380 380			400 400		ns	
	Distortion, Sine Wave Response		0.4			0.4			0.4		%	R_L = 10 kΩ Input Frequency = 1 kHz E_n = V_{DD} V_{is} = V_{DD}/2 (sine wave) p-p
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ E_A = V_{DD}, E_B = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} [V_{os} (B)/V_{is} (A)] = -50 dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ≤ 20 ns $R_{L(OUT)}$ = 1 kΩ $R_{L(IN)}$ = 50 Ω E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ, E_n = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					40		[4]	[4]		MHz	R_L = 1 kΩ V_{is} = V_{DD}/2 (sine wave) p-p E_n = V_{DD}, 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB
f_{MAX}	Enable Input Frequency (Note 4)					10					MHz	C_L = 50 pF, R_L = 1 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{os} = V_{is}/2 at DC V_{is} = V_{DD}
C_{is}	Input Switch Capacitance					4					pF	V_{DD} = 10 V E_n = V_{SS} V_{is} = Open 100 kHz or 1 MHz Bridge
C_{os}	Output Switch Capacitance					4					pF	
C_{ios}	Feedthrough Switch Capacitance					0.2					pF	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11 the voltage drop across the bidirectional switch must not exceed 0.8 V at $T_A \leq 25°C$, or 0.3 V at $T_A > 25°C$. No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.